Best Case Analysis

Asian IBIS Summit
Tokyo, Japan
November 12, 2018

Shinichi Maeda
KEI Systems
E-mail: KEI-Systems@jcom.home.ne.jp
Outline

• Typical Case? / Worst Case?
• Characteristics of IC
• New Feature of Future IO Device
• What is Best Case Analysis?
• How to Execute Best Case Analysis?
• IBIS-AMI
Typ/Min/Max

- IBIS Model has three cases
- Typ/Min/Max

[Model Spec]
<table>
<thead>
<tr>
<th>Subparameter</th>
<th>typ</th>
<th>min</th>
<th>max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thresholds</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vinh</td>
<td>3.5</td>
<td>3.15</td>
<td>3.85</td>
</tr>
<tr>
<td>Vinl</td>
<td>1.5</td>
<td>1.35</td>
<td>1.65</td>
</tr>
</tbody>
</table>

[Pulldown]
<table>
<thead>
<tr>
<th>Voltage</th>
<th>I(typ)</th>
<th>I(min)</th>
<th>I(max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>−5.0V</td>
<td>−40.0m</td>
<td>−34.0m</td>
<td>−45.0m</td>
</tr>
<tr>
<td>−4.0V</td>
<td>−39.0m</td>
<td>−33.0m</td>
<td>−43.0m</td>
</tr>
</tbody>
</table>

[Falling Waveform]
<table>
<thead>
<tr>
<th>Time</th>
<th>V(typ)</th>
<th>V(min)</th>
<th>V(max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0000s</td>
<td>5.0000V</td>
<td>4.5000V</td>
<td>5.5000V</td>
</tr>
<tr>
<td>0.2000ns</td>
<td>4.7470V</td>
<td>4.4695V</td>
<td>4.8815V</td>
</tr>
</tbody>
</table>

IBIS Specification Version 6.1

KEI Systems
• I-V, V-T
Typ vs. Corner

- Max
- Typ
- Min

- Model
  - DDR4 2400, DQ
Characteristics of IC

- The Characteristics of IC has variation
  - The variation is normally distributed
- Variation of Lots, Within Wafer variation, Within Chip variation
Tolerance of IC Characteristics

- Driver: Slow - Fast
- Receiver: Slow - Fast

Where is Actual IC?
DDR has Variation of I/O

- DDR4 Driver: 34 ohm, 40 ohm, 48 ohm
  - Pull-up: 3 Models are overlapped
DDR Driver’s/Receiver’s Characteristics

- Driver Impedance
- ODT
- The Variation are overlapped
Coming Device Becomes Faster

- Over 1 GHz Design is really difficult
- Can not pass the Worst-Case Analysis
- Does Design based Typical-Case Analysis can use for Sign-Off?
- Multi Characteristics Drivers/Receivers to select according to PCB design
- Analog filter to make better signal quality
- Already implemented for DDR5, PCIe and more
New Feature of Future IO Device

• Training
  • Execute Initial Stage
    • 1. Driver: Send Test Pattern Data
    • 2. Receiver: Send Back Received Data
    • 3. Driver: Set Difficult Driver/Receiver Characteristics
  • Back to Step 1
• Already Implemented
  • DDR4/DDR5
  • PCI Express/USB 3~, High-Speed Serial
Training/Setting

- DDR4 Initialize/Wait

Power ON

Initialization

ZQ Calibration

MPSM

IVREFDQ, RTT, Etc

MPR, Write Leveling Vref, DQ training

ZQCS, ZQCL

Read/Write Mode

KEI Systems
What is Best Case Analysis?

- Training Feature selects Best combination of Driver/Receiver
  - Best sets of each PCB
  - Variation of Each IC’s Characteristics
- PCB works in Best Case
- Simulation can not simulate Best Case
  - Mode has only Max/Typ/Min case
  - Can not simulate include the variation of each IC
How to Execute Best Case Analysis?

• If simulation result has no error, actual PCB should work well
• IBIS Model supports “Model Selector”
• IBIS-AMI

• In DDR4 Simulation, It should be executed manually
  • 1. Use Low (34 ohm) Driver/Middle ODT (60 ohm) Models and Typ case simulation
  • 2. If result is OK, it’s OK.
      If result is NG, change the model and re-simulate
      (It’s necessary to judge which is better Faster/Slower)
### IBIS Model

- Easy (Accustomed) to use
- Good tools (Viewer, Editor)
- [Model selector] (Simulator’s Issue)

- Can not support Analog Filter

```plaintext
<table>
<thead>
<tr>
<th>[Model Selector]</th>
<th>Progbuffer1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>OUT_2</td>
<td>2 mA buffer without slew rate control</td>
</tr>
<tr>
<td>OUT_4</td>
<td>4 mA buffer without slew rate control</td>
</tr>
<tr>
<td>OUT_6</td>
<td>6 mA buffer without slew rate control</td>
</tr>
<tr>
<td>OUT_4S</td>
<td>4 mA buffer with slew rate control</td>
</tr>
<tr>
<td>OUT_6S</td>
<td>6 mA buffer with slew rate control</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>[Model Selector]</th>
<th>Progbuffer2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>OUT_2</td>
<td>2 mA buffer without slew rate control</td>
</tr>
<tr>
<td>OUT_6</td>
<td>6 mA buffer without slew rate control</td>
</tr>
<tr>
<td>OUT_6S</td>
<td>6 mA buffer with slew rate control</td>
</tr>
<tr>
<td>OUT_8S</td>
<td>8 mA buffer with slew rate control</td>
</tr>
<tr>
<td>OUT_10S</td>
<td>10 mA buffer with slew rate control</td>
</tr>
</tbody>
</table>
```
IBIS-AMI

- Good (Best) way
  - Maybe Implemented Best Case Analysis, already
    - Simulation for PCI Express

- Can not review/evaluate the Model
  - No Viewer, Editor
Conclusion

• IC’s Training Feature is very useful to make easy PCB Design
• It’s the good idea to expand implementation for not only DDR4/DDR5, PCIe but also other fast signals
• “Best Case Analysis” is enough for Training Devices
  • Actual PCB should have better result than Simulation
• Both IBIS Model and IBIS-AMI can support “Best Case Analysis” without any enhancement
Reference

• Masuko, Maeda “Embedded DDR4 Design Simulation” 2016 Asian IBIS Summit, Tokyo
• Maeda “DDR System Simulation: What Issue to Simulate” 2017 Asian IBIS Summit, Tokyo