Best Case Analysis

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Outline

- Typical Case? / Worst Case?
- Characteristics of IC
- New Feature of Future IO Device
- What is Best Case Analysis?
- How to Execute Best Case Analysis?
- IBIS-AMI

Typ/Min/Max

- IBIS Model has three cases
- Typ/Min/Max

```
[Model Spec]
|   Subparameter          typ        min        max
| Thresholds
|
Vinh                      3.5        3.15       3.85     | 70% of Vcc
Vinl                      1.5        1.35       1.65     | 30% of Vcc
```

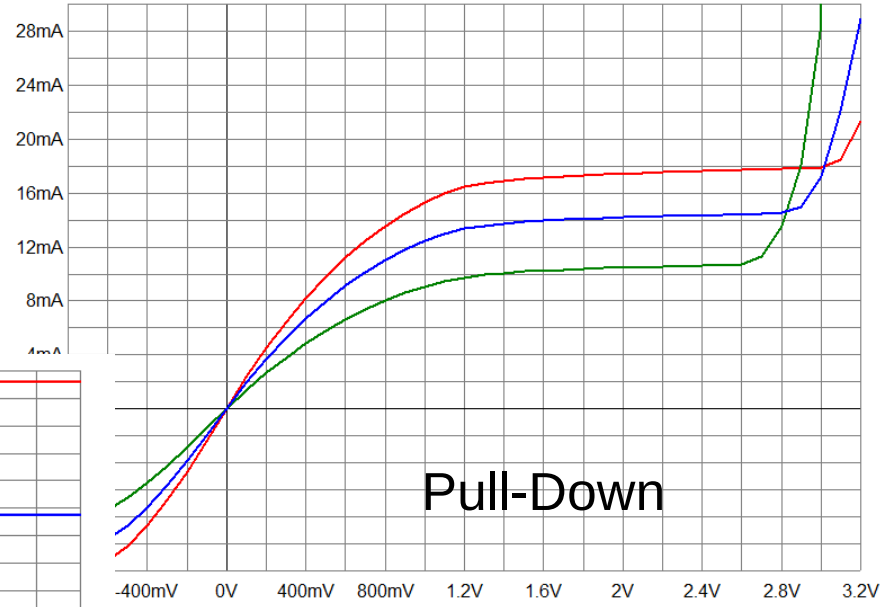
```
[Pulldown]
|  Voltage    I(typ)     I(min)     I(max)
|
    -5.0V     -40.0m     -34.0m     -45.0m
    -4.0V     -39.0m     -33.0m     -43.0m
```

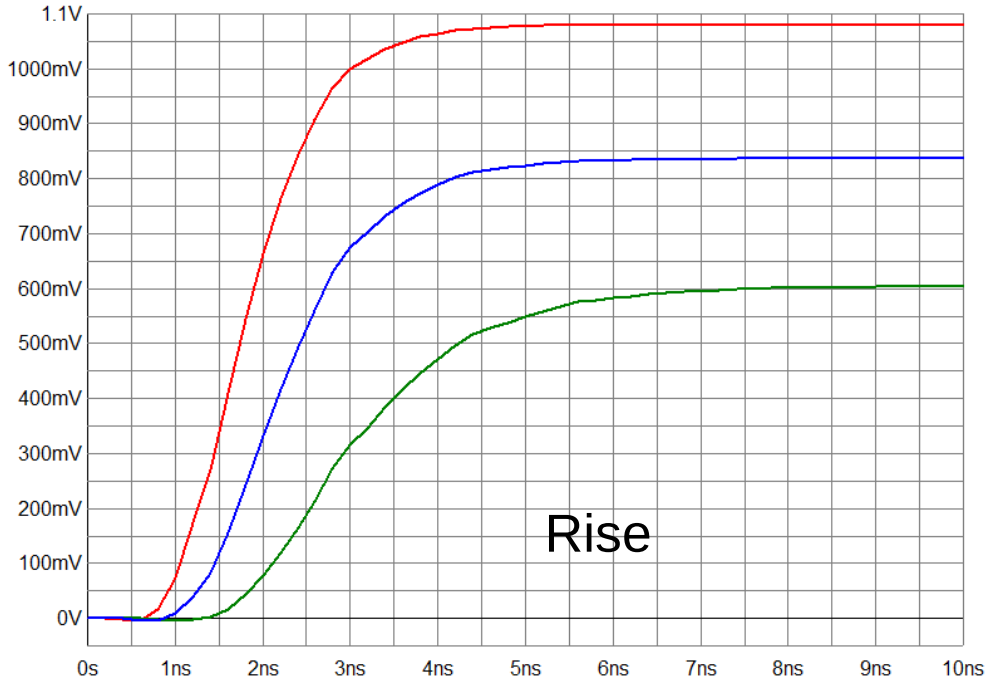
```
[Falling Waveform]
R_fixture = 50
V_fixture = 5.5
V_fixture_min = 4.5
V_fixture_max = 5.5
| Time          V(typ)          V(min)          V(max)
   0.0000s       5.0000V         4.5000V         5.5000V
   0.2000ns      4.7470V         4.4695V         4.8815V
```

IBIS Specification Version 6.1

Typ/Min/Max

- I-V, V-T

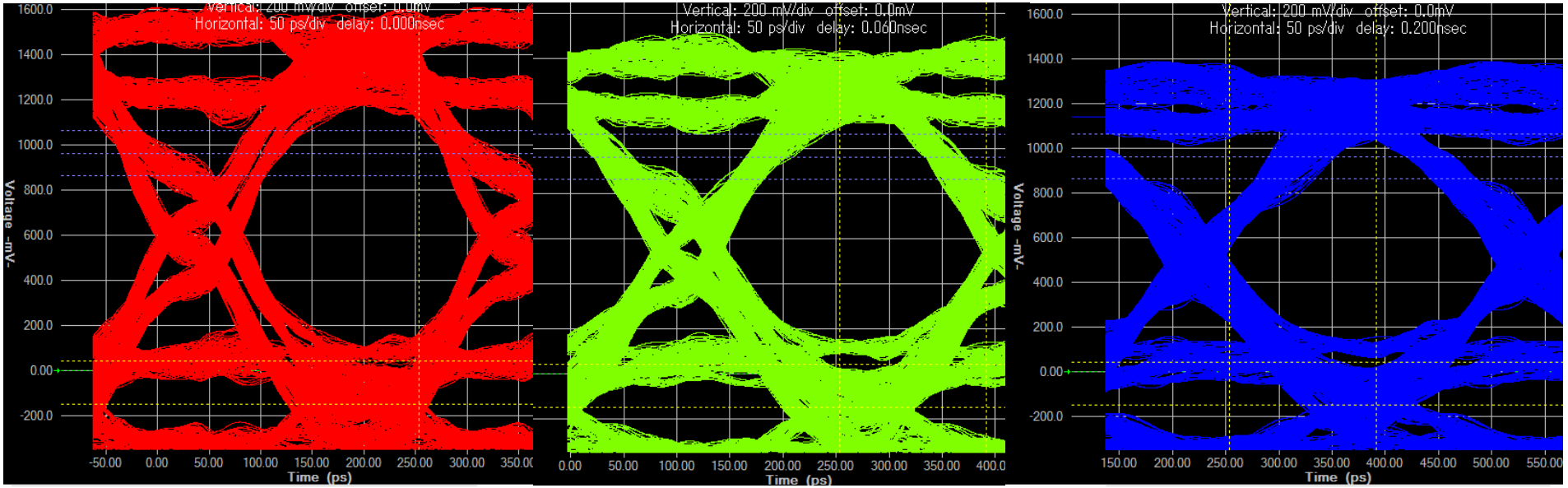




Typ
Min
Max

Typ vs. Corner

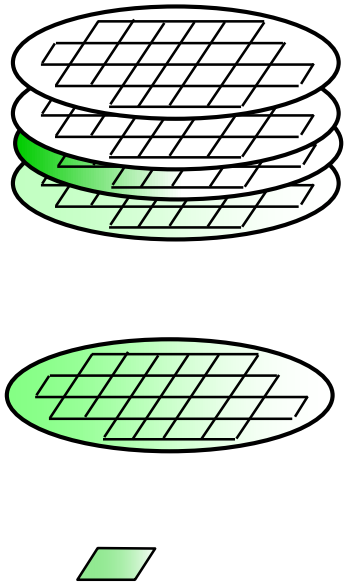
- Max Typ Min

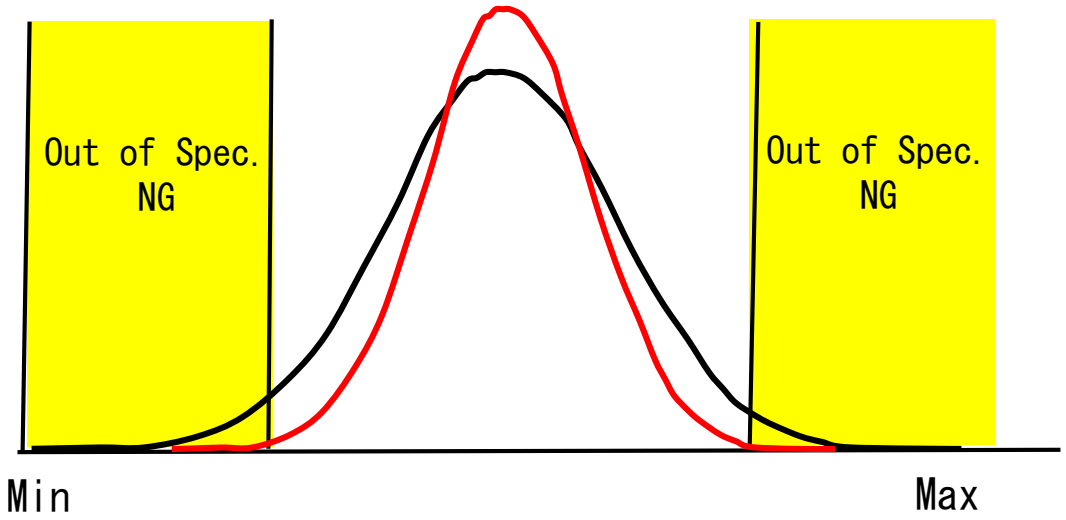


- Model
  - DDR4 2400, DQ

Characteristics of IC

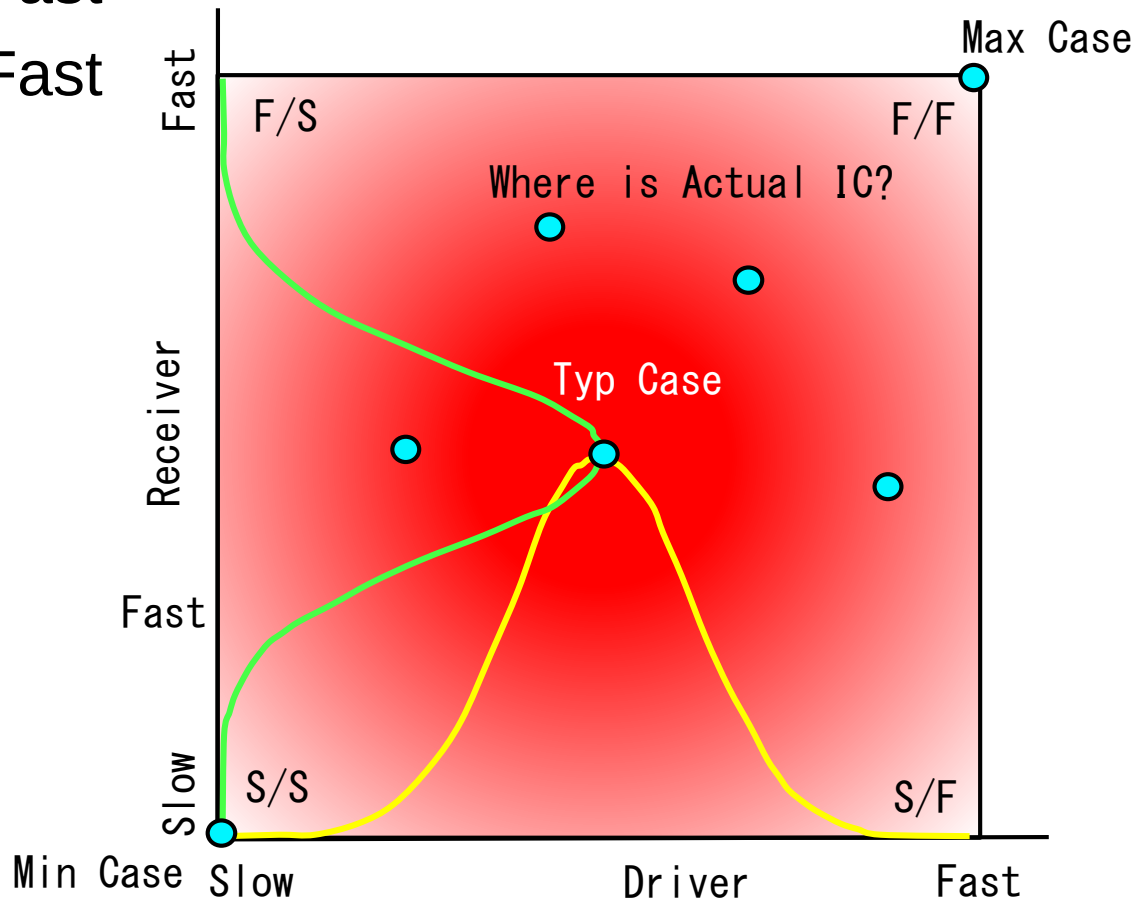
- The Characteristics of IC has variation
  - The variation is normally distributed
- Variation of Lots, Within Wafer variation, Within Chip variation





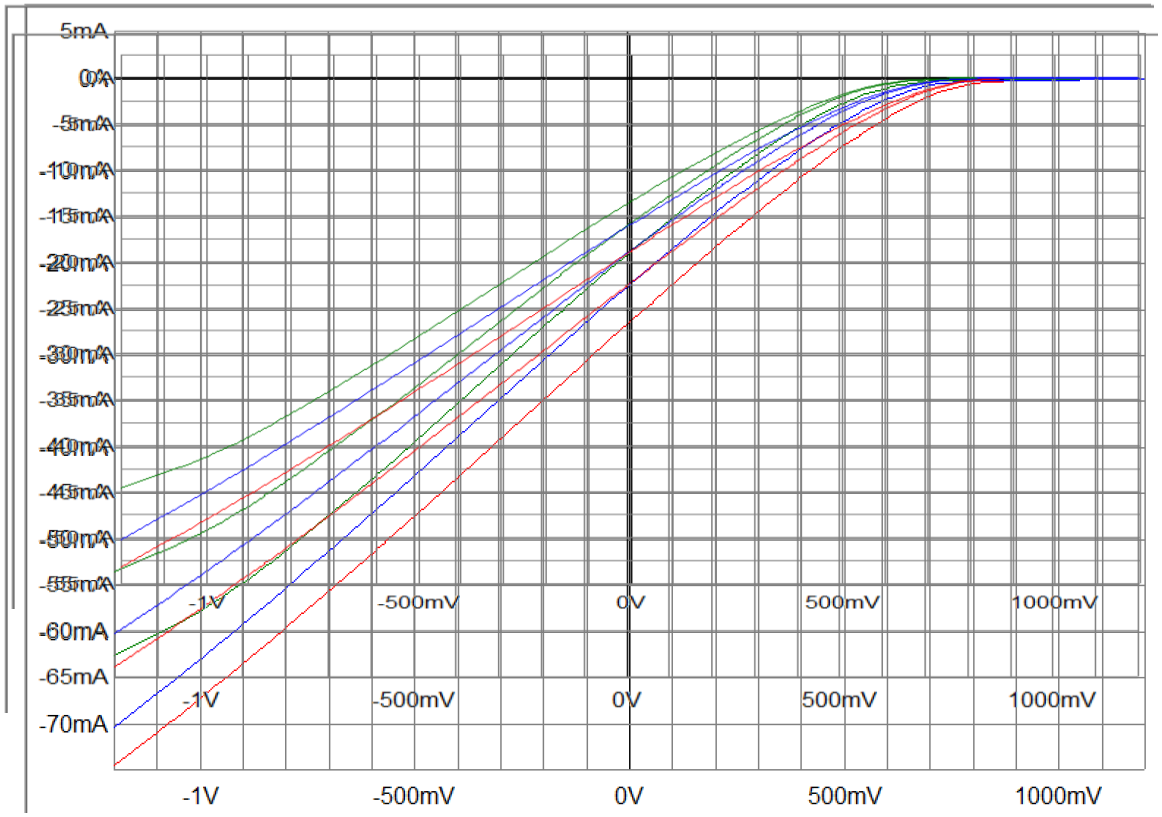
Tolerance of IC Characteristics

- Driver: Slow - Fast
- Receiver: Slow - Fast



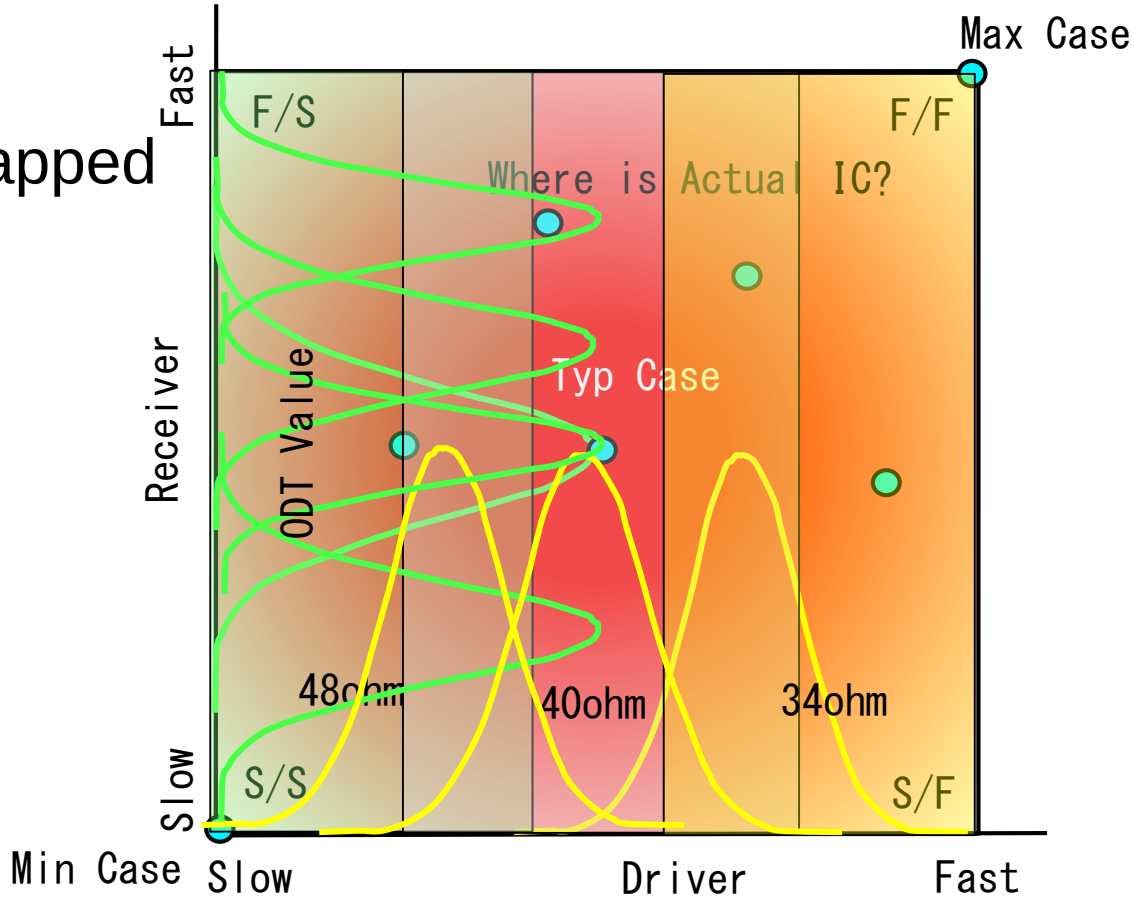
DDR has Variation of I/O

- DDR4 Driver: 34 ohm, 40 ohm, 48 ohm
  - Pull-up : 3 Models are overlapped



DDR Driver's/Receiver's Characteristics

- Driver Impedance
- ODT
- The Variation are overlapped



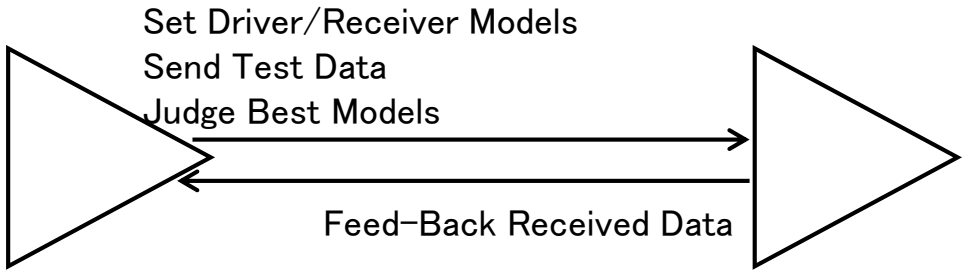
Coming Device Becomes Faster

- Over 1 GHz Design is really difficult
- Can not pass the Worst-Case Analysis
- Does Design based Typical-Case Analysis can use for Sign-Off?
- Multi Characteristics Drivers/Receivers to select according to PCB design
- Analog filter to make better signal quality

- Already implemented for DDR5, PCIe and more

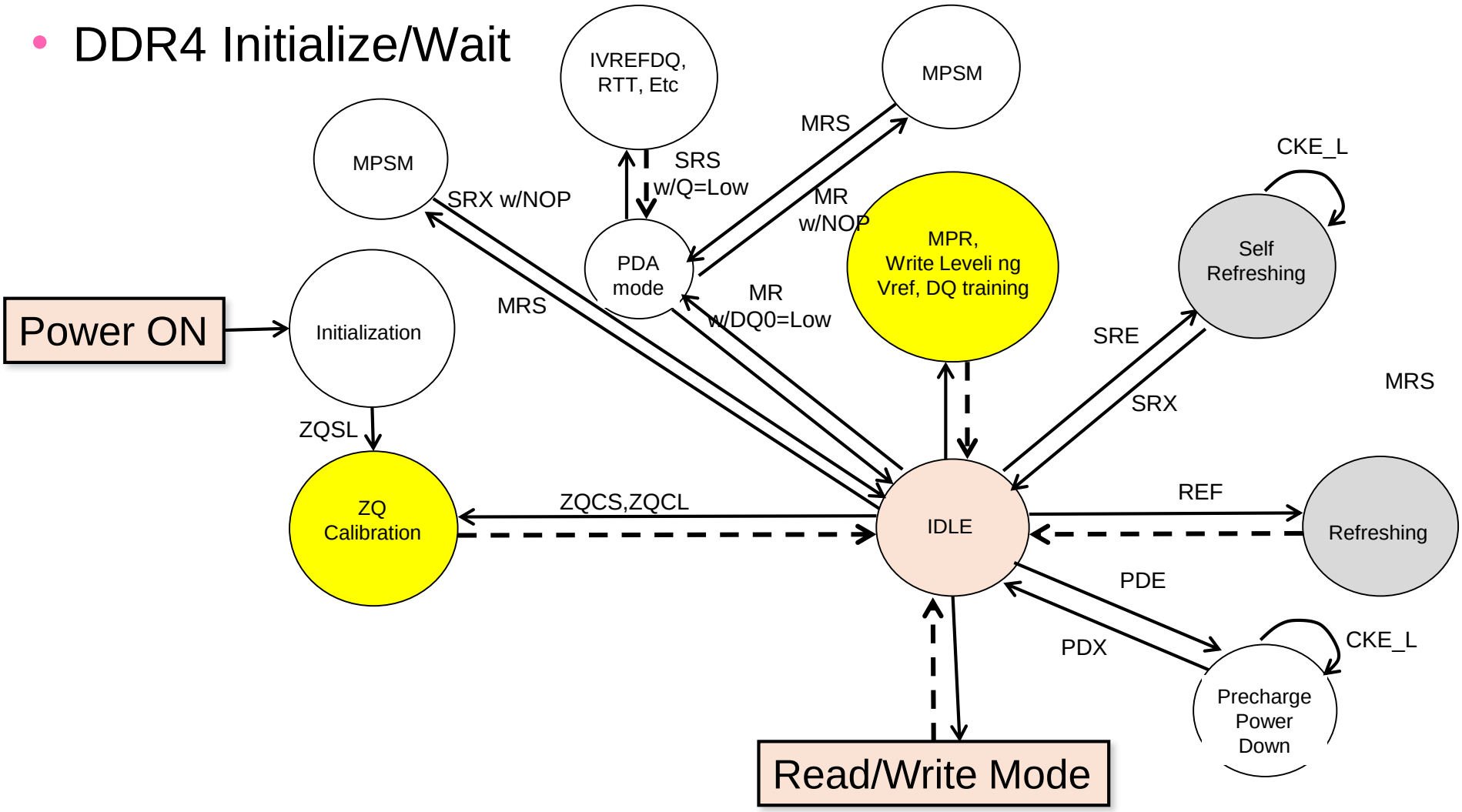
New Feature of Future IO Device

- Training
  - Execute Initial Stage
    - 1. Driver: Send Test Pattern Data
    - 2. Receiver: Send Back Received Data
    - 3. Driver: Set Difficult Driver/Receiver Characteristics
    - Back to Step 1
  - Already Implemented
    - DDR4/DDR5
    - PCI Express/USB 3~, High-Speed Serial



Training/Setting

- DDR4 Initialize/Wait



What is Best Case Analysis?

- Training Feature selects Best combination of Driver/Receiver
  - Best sets of each PCB
  - Variation of Each IC's Characteristics
- PCB works in Best Case
- Simulation can not simulate Best Case
  - Mode has only Max/Typ/Min case
  - Can not simulate include the variation of each IC

How to Execute Best Case Analysis?

- If simulation result has no error, actual PCB should work well
- IBIS Model supports “Model Selector”
- IBIS-AMI

- In DDR4 Simulation, It should be executed manually
  - 1. Use Low (34 ohm) Driver/Middle ODT (60 ohm) Models and Typ case simulation
  - 2. If result is OK, it’s OK.

    If result is NG, change the model and re-simulate

    (It’s necessary to judge which is better Faster/Slower)

IBIS Model

- Easy (Accustomed) to use
  - Good tools (Viewer, Editor)
  - [Model selector] (Simulator's Issue)

- Can not support Analog Filter

```
[Model Selector]          Progbuffer1
|
OUT_2        2 mA buffer without slew rate control
OUT_4        4 mA buffer without slew rate control
OUT_6        6 mA buffer without slew rate control
OUT_4S       4 mA buffer with slew rate control
OUT_6S       6 mA buffer with slew rate control
|
[Model Selector]          Progbuffer2
|
OUT_2        2 mA buffer without slew rate control
OUT_6        6 mA buffer without slew rate control
OUT_6S       6 mA buffer with slew rate control
OUT_8S       8 mA buffer with slew rate control
OUT_10S     10 mA buffer with slew rate control
```

IBIS-AMI

- Good (Best) way
  - Maybe Implemented Best Case Analysis, already
    - Simulation for PCI Express

- Can not review/evaluate the Model
  - No Viewer, Editor

Conclusion

- IC's Training Feature is very useful to make easy PCB Design
- It's the good idea to expand implementation for not only DDR4/DDR5, PCIe but also other fast signals
- "Best Case Analysis" is enough for Training Devices
  - Actual PCB should have better result than Simulation
- Both IBIS Model and IBIS-AMI can support "Best Case Analysis" without any enhancement

Reference

- Maeda “Is Typ. Analysys Enough? What Is Corner Condition?” 2016 Asian IBIS Summit, Tokyo
- Masuko, Maeda “Embedded DDR4 Design Simulation” 2016 Asian IBIS Summit, Tokyo
- Maeda “DDR System Simulation: What Issue to Simulate” 2017 Asian IBIS Summit, Tokyo