Package Models for Critical Timing Validation with IBIS (Based on DDR Design)

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JPCA

- Japan Electronics Packaging and Circuit Association

JPCA Electronics Related Industry

- Material
- Chemical
- Circuit
- Equipment • Test
- Trading • Service
JPCA Design Academy

• DDR4 Project

ASIC Vendor’s Reference Design

Reference Design
- Megtron 6
- 16 Layers
- Constraint

User’s Requirements

Change Condition
- Material FR4
- Line / Space
- Via size
- Cross Section

Cannot Apply the Same Design
Change Layout

Good Result

Propose!

* Satisfy the Manufacturing Requirements
* Satisfy the System Developer’s Requirements
Trial Board Overview

- Clock: 1200MHz
- Data rate: 2400Mbps
- Data: 8bit burst mode
- FPGA: Xilinx Kintex UltraScale -1156 pin
- DDR4: Micron MT40A256M16GE -96 pin, 2Byte

Differential Clocks
Address / Command / Control

Data: Bytelane 0
DQS0
Data Bytelane 1
DQS1
Data Bytelane 2
DQS2
Data Bytelane 3
DQS3
Data Bytelane 4
DQS4
Data Bytelane 5
DQS5
Data Bytelane 6
DQS6
Data Bytelane 7
DQS7

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Trial Board Stackup

Trial Board Stackup

DDR4 x4

FPGA
**DQ Simulation Example**

Package Power Model is important for SI/PI and it’s already addressed on BIRD discussion.
Example of DDR4 Timing Chart

Timing definition example for Read operation

- Many Timing specification (parameters) are defined
- It’s impossible to measure all with IBIS simulations
What do you see with SI simulation?

- **SI**
  - Reflection
  - Crosstalk
  - Skew in a Byte signals
  - Signal level
  - Topology check

- **Power**
  - Power noise
  - Decap effect

- **Timing?**
  - Can you see it?
What do you see with SI simulation?

Eye Pattern: One Byte DQ Simulation
Read operation: Controller Die pin

- We could see eye opening (This is a kind of timing)
- Clearance: Eye Mask <-> Signal
Focus on One Bit

Test Topology (Extracted DQ)

Simplified

- DDR4 Memory IO
- FPGA IO

Driver (Memory)
- Pkg
- 49.15mm
- 40Ω
- Receiver (FPGA)
- Pkg
- LCR
- LCR
What do you see with SI simulation?

DQ at Controller: Data Read

- Rising time of Die pin is slower than Pkg pin
- Which curve is used for measurement?
  - Die pin should be used but this curve is...
Ex1: Use [Define Package Model]

Ex2: Replace Pkg model with T-Line

Ex3: Remove Pkg model

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Package stub length of Ex2 is given as ‘Package stub length sheet’ as below.

<table>
<thead>
<tr>
<th>PinName</th>
<th>NetName</th>
<th>Delay_Max(pS)</th>
<th>Delay_Min(pS)</th>
<th>Length_Max(mm)</th>
<th>Length_Min(mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AE23</td>
<td>DQ0</td>
<td>70.274</td>
<td>69.575</td>
<td>10.531</td>
<td>10.536</td>
</tr>
</tbody>
</table>

Maybe Ex2 is more realistic.
IBIS Specification Supports PKG Length

• [Pin Numbers] support Package stub length
  – Support distributed Pkg model (with [Number of Sections] and with Len > 0)
    • Ex:
      [Pin Numbers]
      A1 Len=0 L=1.2n/ Len=1.2 L=2.0n C=0.5p R=0.05/ Len=0 L=2.0n C=1.0p/

• [Define Package Model] doesn’t support length with [Model Data]
  – Support LCR matrix only

• Which model is better?
  – I want to do both
  – But I have never seen “Len” at [Pin Numbers] keyword
How to Treat Package Length

• Lumped constant (LCR) is useful for SI/PI simulation
• Lumped constant (LCR) is not sufficient for Timing Verification
• Best is Package S-Parameter model
  – Many SI simulators don’t support S-parameter
• EX2 (Page15) is required in use T-Line (impedance)
  – Most of IBIS models don’t support “Len” parameter
  – Impedance is not specified anywhere
Required Information for Timing Verification

- Package impedance is required in [Pin Numbers] section
- Package impedance and Length are required in [Define Package Model]
END