



Package Models for Critical Timing Validation with IBIS (Based on DDR Design)

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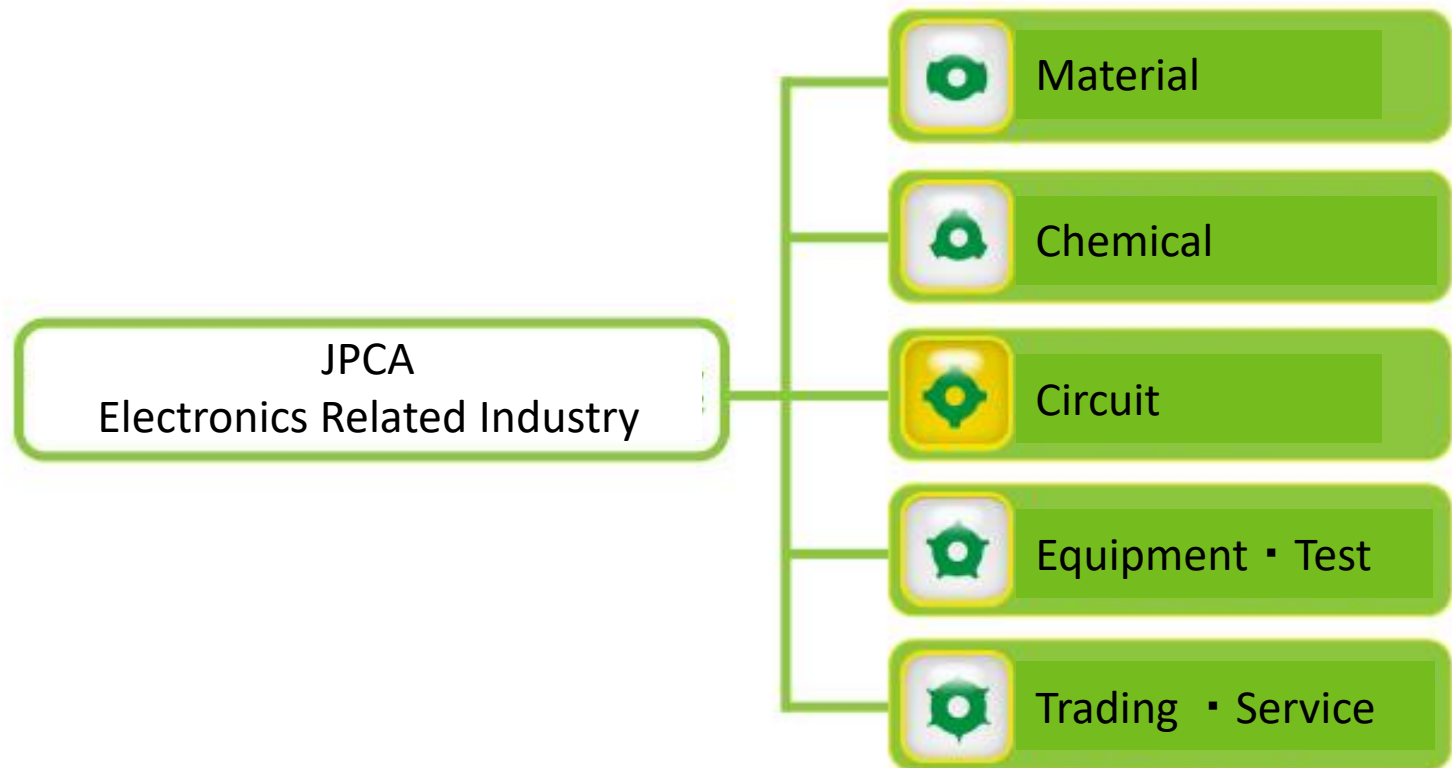
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JPCA

- Japan Electronics Packaging and Circuits Association

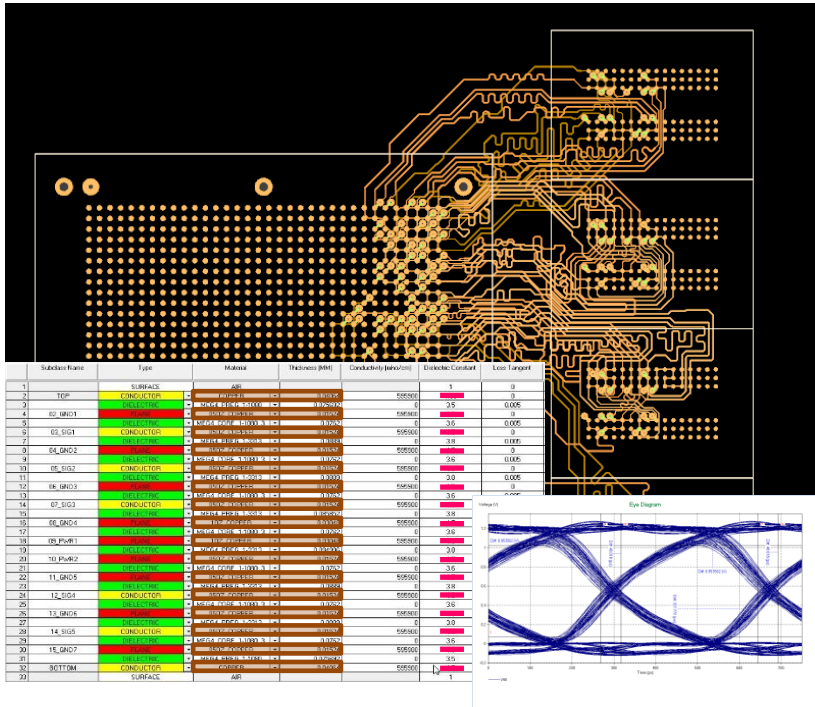




JPCA Design Academy

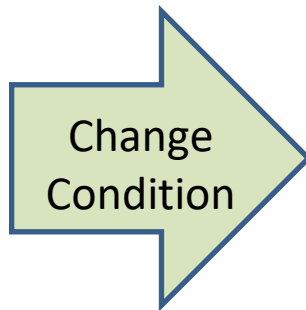
• DDR4 Project

ASIC Vendor's Reference Design

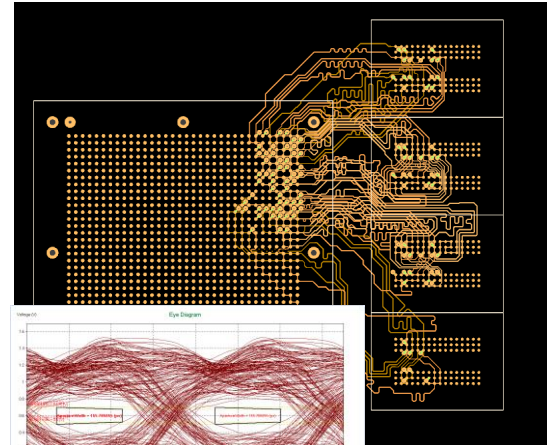


Reference Design

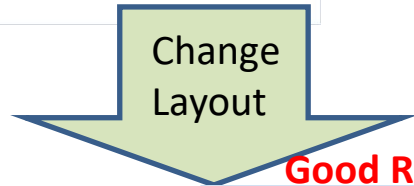
- Megtron 6
- 16 Layers
- Constraint



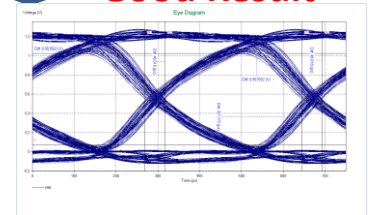
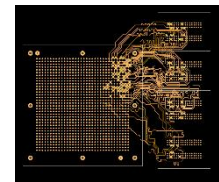
- Material FR4
- Line / Space
- Via size
- Cross Section



Cannot Apply the Same Design



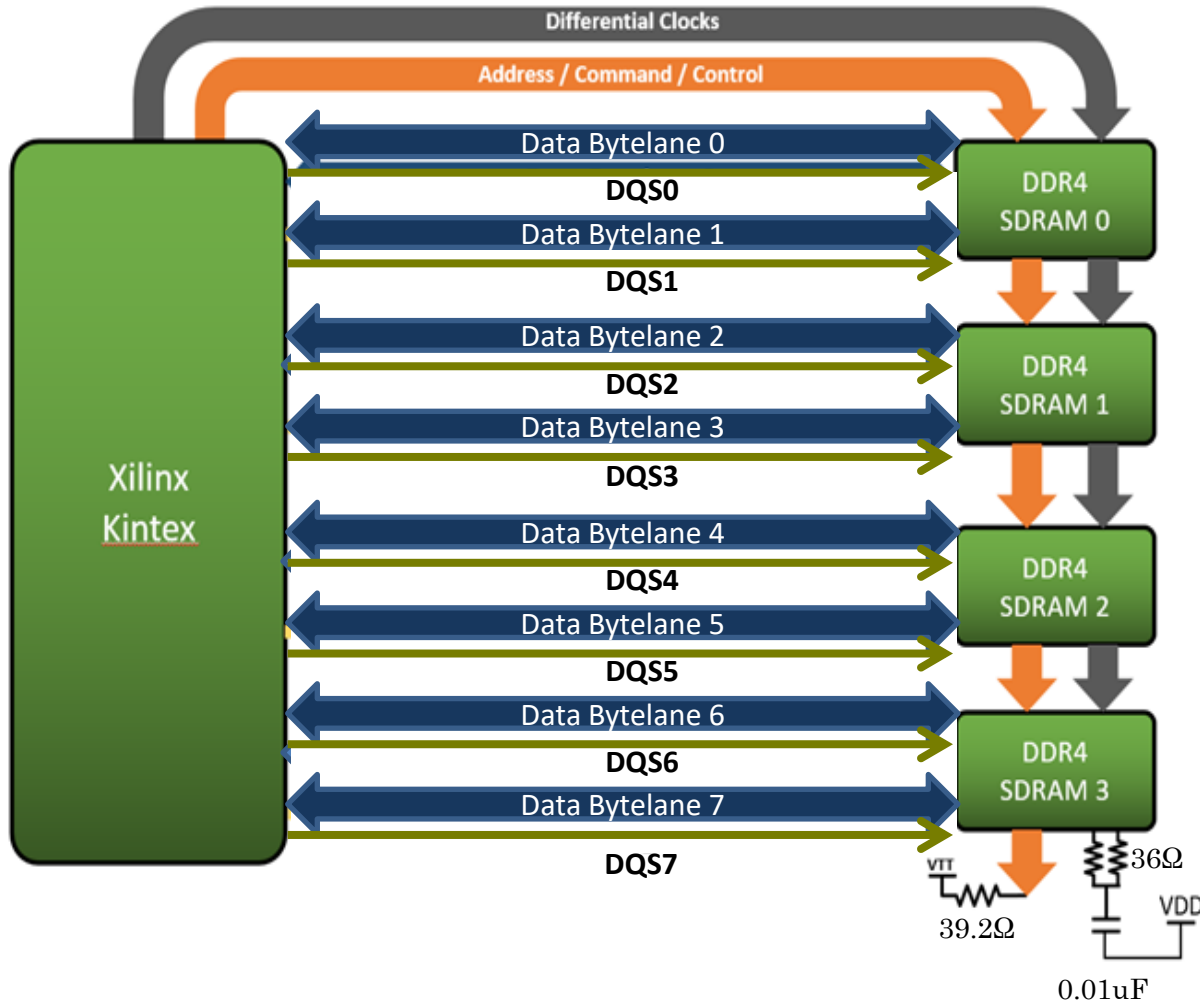
- * Satisfy the Manufacturing Requirements
- * Satisfy the System Developer's Requirements



Good Result



Trial Board Overview



Clock: 1200MHz

Data rate: 2400Mbps

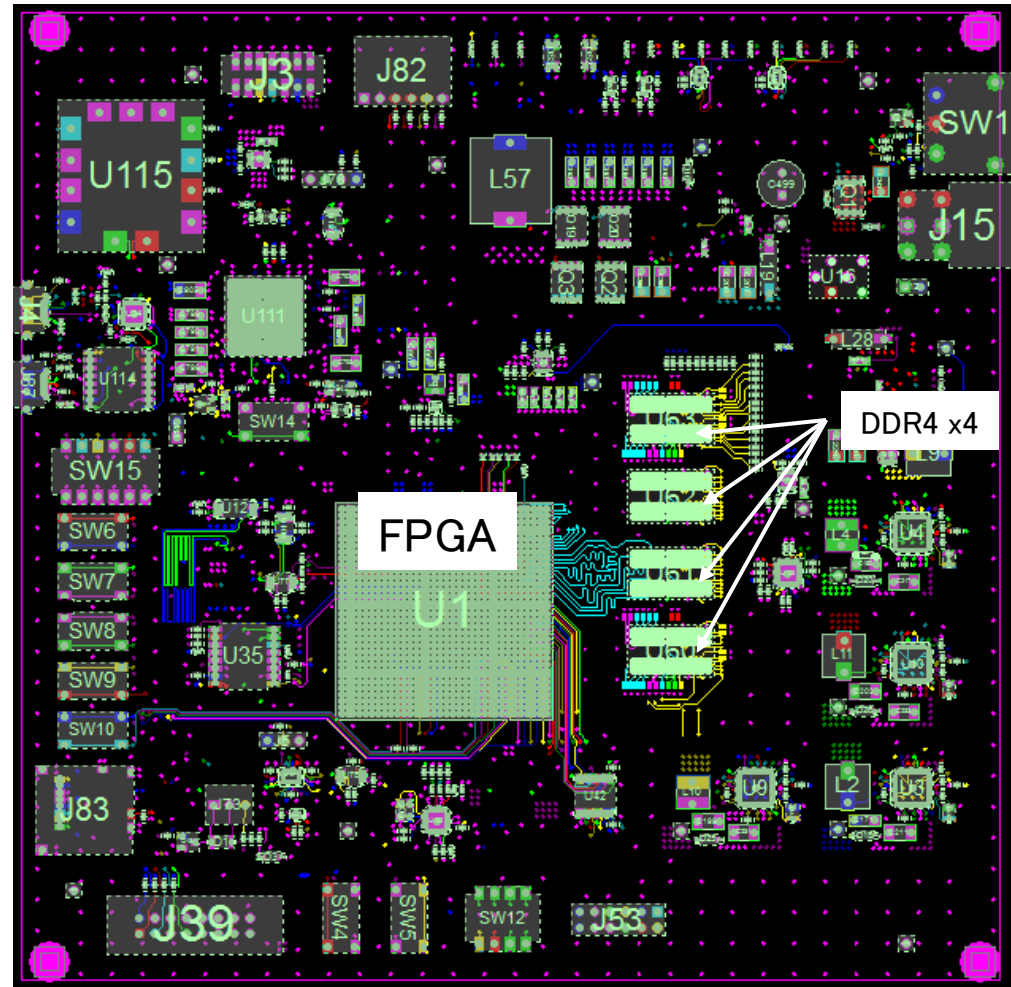
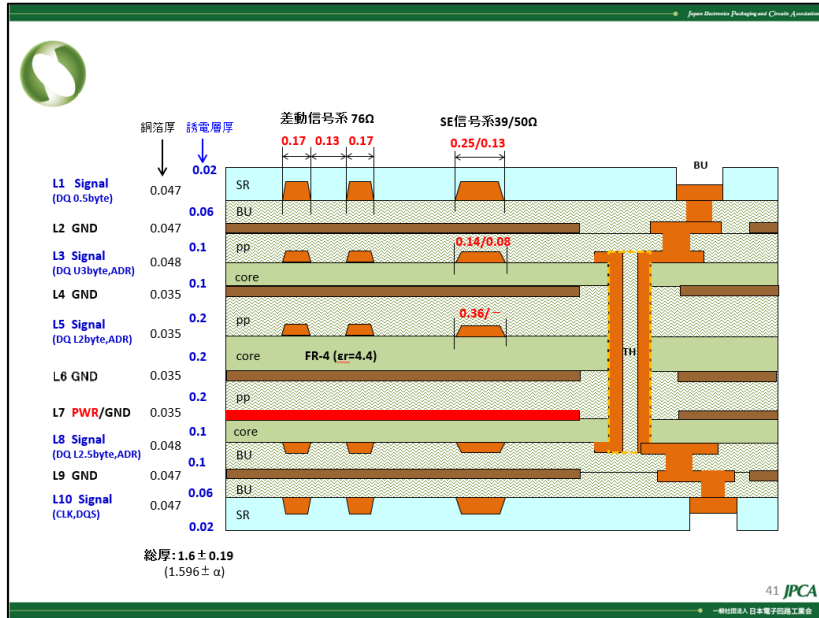
Data: 8bit burst mode

FPGA: Xilinx Kintex UltraScale
-1156 pin

DDR4: Micron MT40A256M16GE
-96 pin, 2Byte

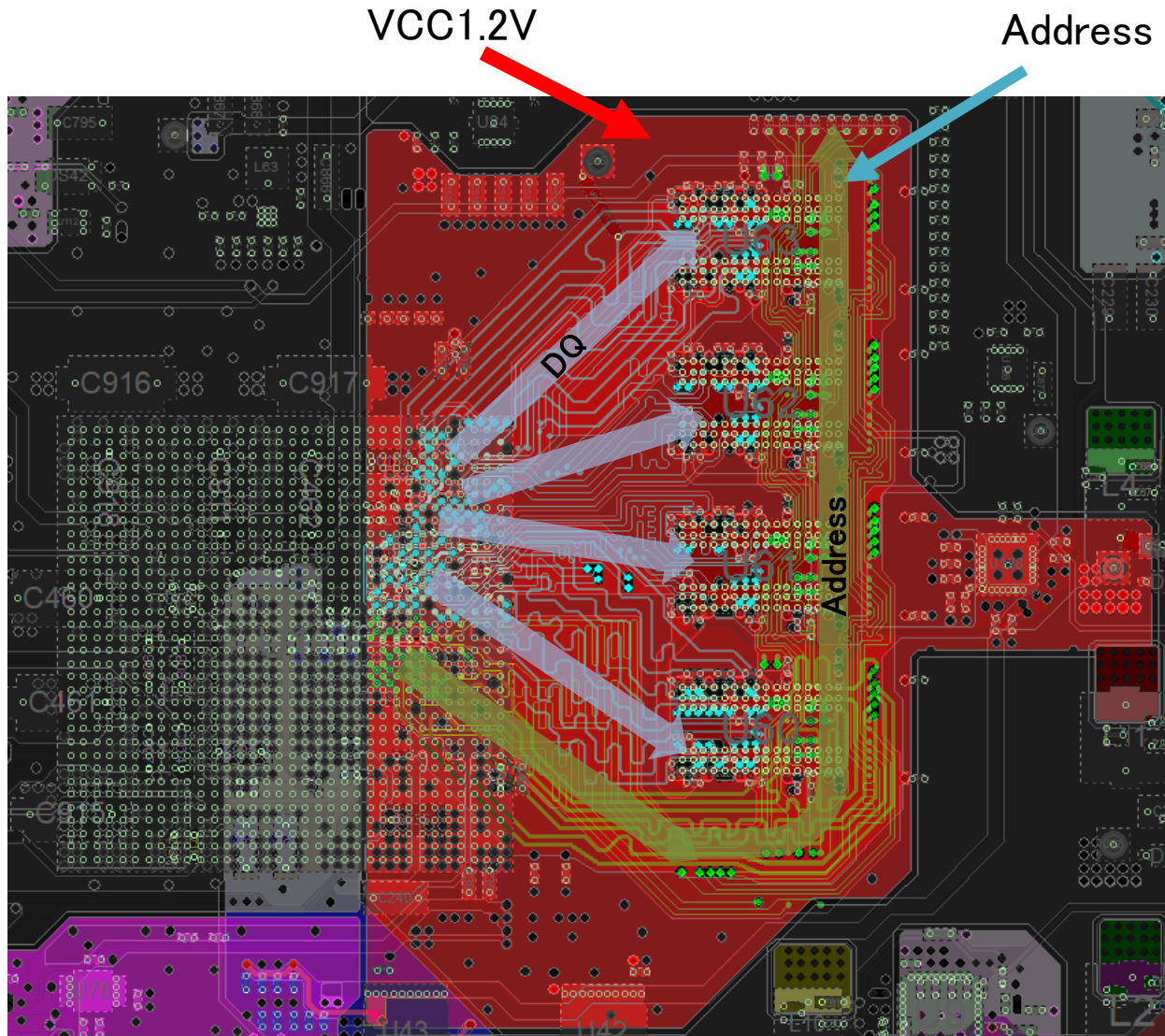


Trial Board Stackup





Trial Board Layout

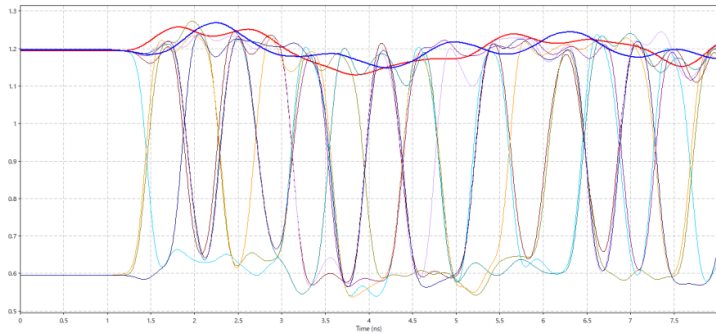




DQ Simulation Example

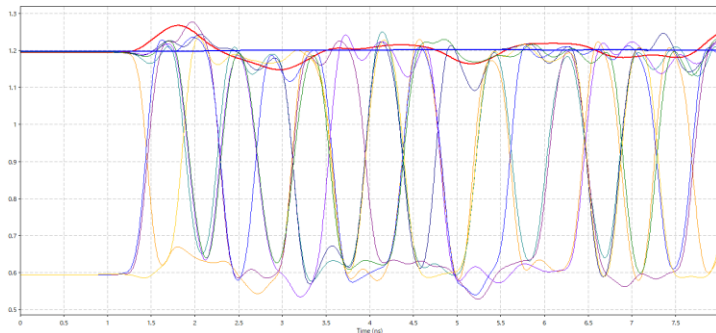
— 1.2V Die
— 1.2V PCB

Package Power Model is important for SI/PI and it's already addressed on BIRD discussion.



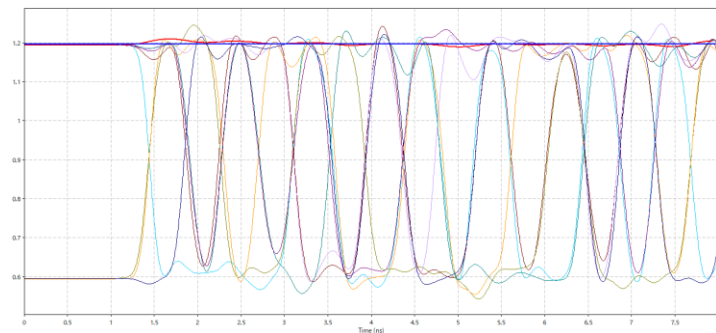
PCB
no decap

PKG
no decap



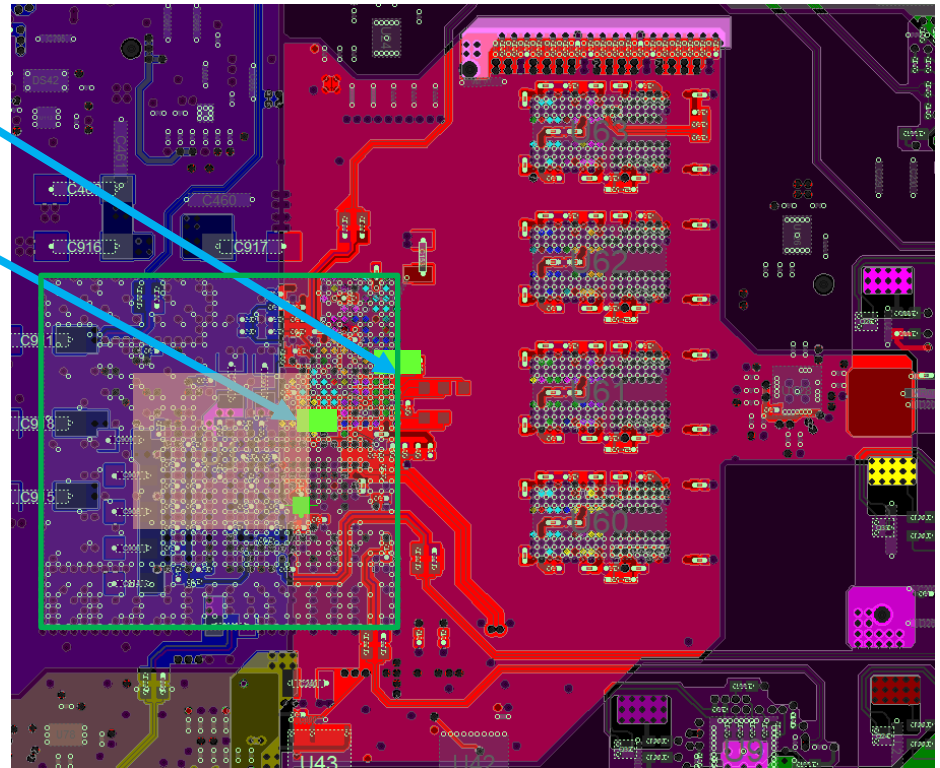
PCB
0.1uF

PKG
no decap



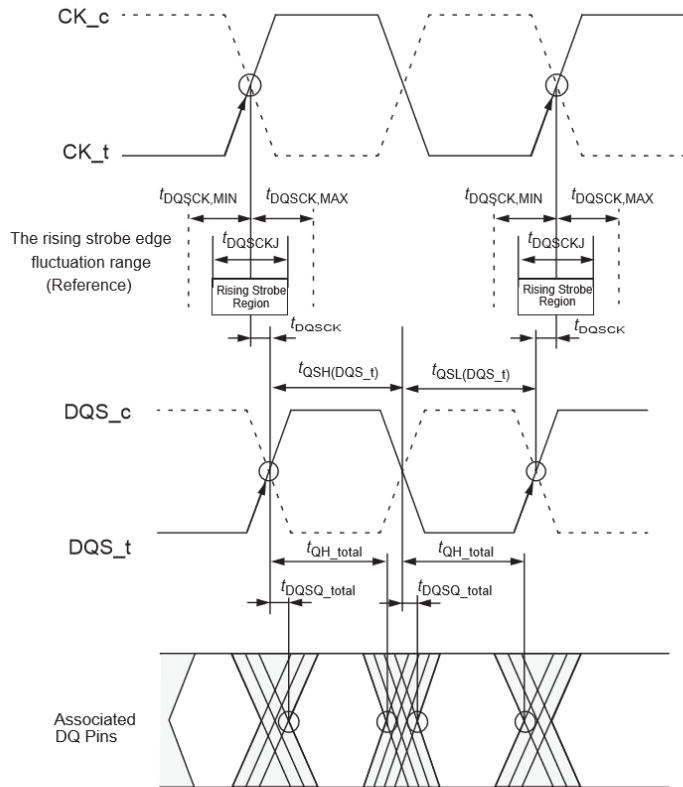
PCB
0.1uF

PKG
0.1uF

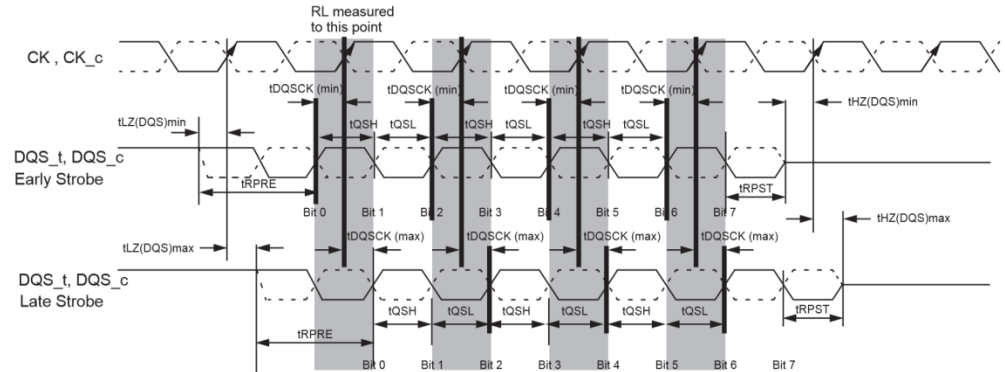


Example of DDR4 Timing Chart

Timing definition example for Read operation



JEDEC Standard: JESD79-4A
READ Timing Definition

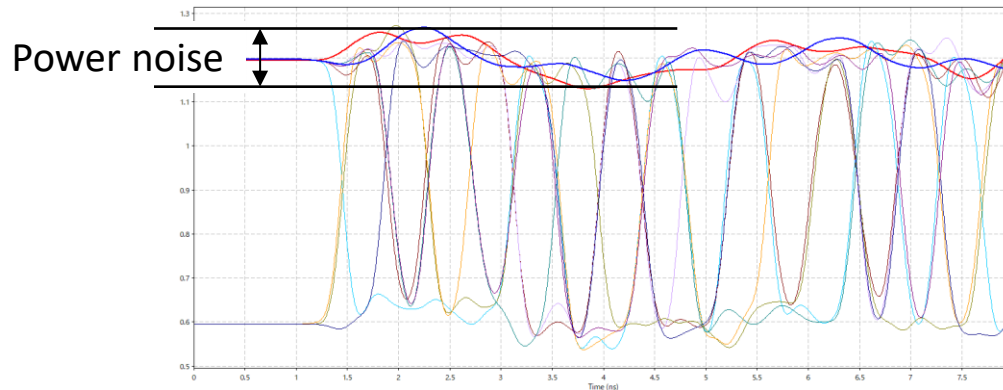


JEDEC Standard: JESD79-4A
Clock to Data Strobe Relationship

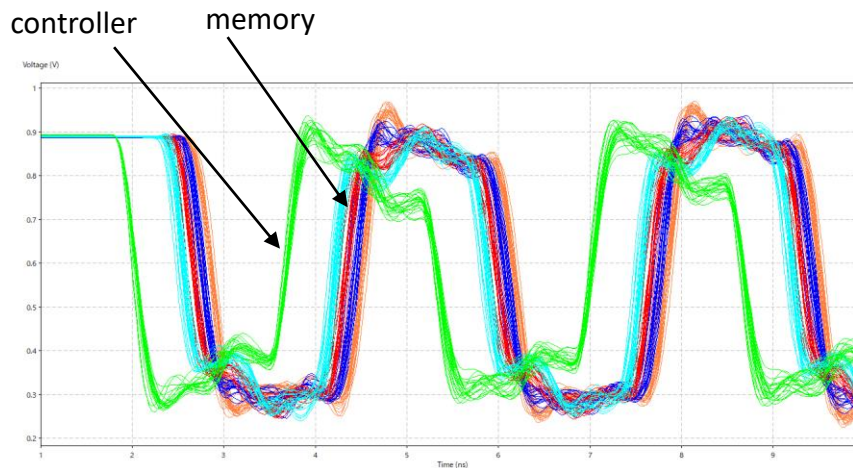
- Many Timing specification (parameters) are defined
- It's impossible to measure all with IBIS simulations



What do you see with SI simulation ?



Multibit DQ Simulation



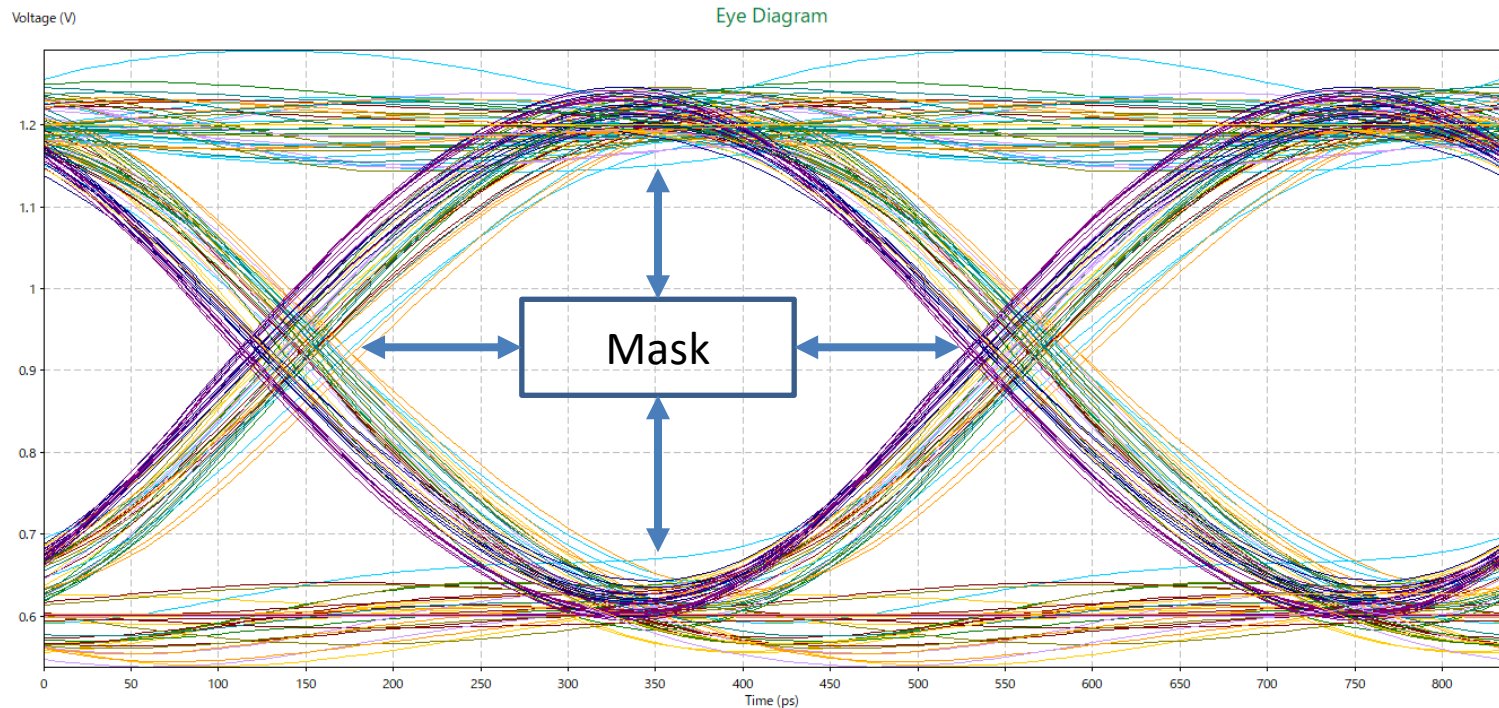
Address/Cmd simulation

- SI
 - Reflection
 - Crosstalk
 - Skew in a Byte signals
 - Signal level
 - Topology check
- Power
 - Power noise
 - Decap effect
- Timing ?
 - Can you see it ?



What do you see with SI simulation ?

Eye Pattern: One Byte DQ Simulation
Read operation: Controller Die pin

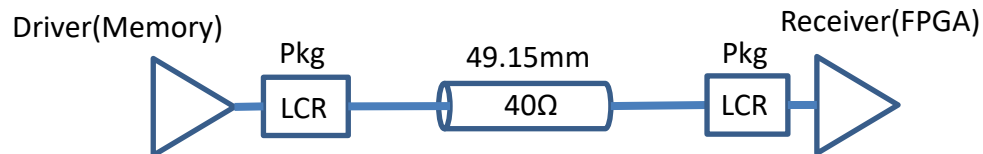
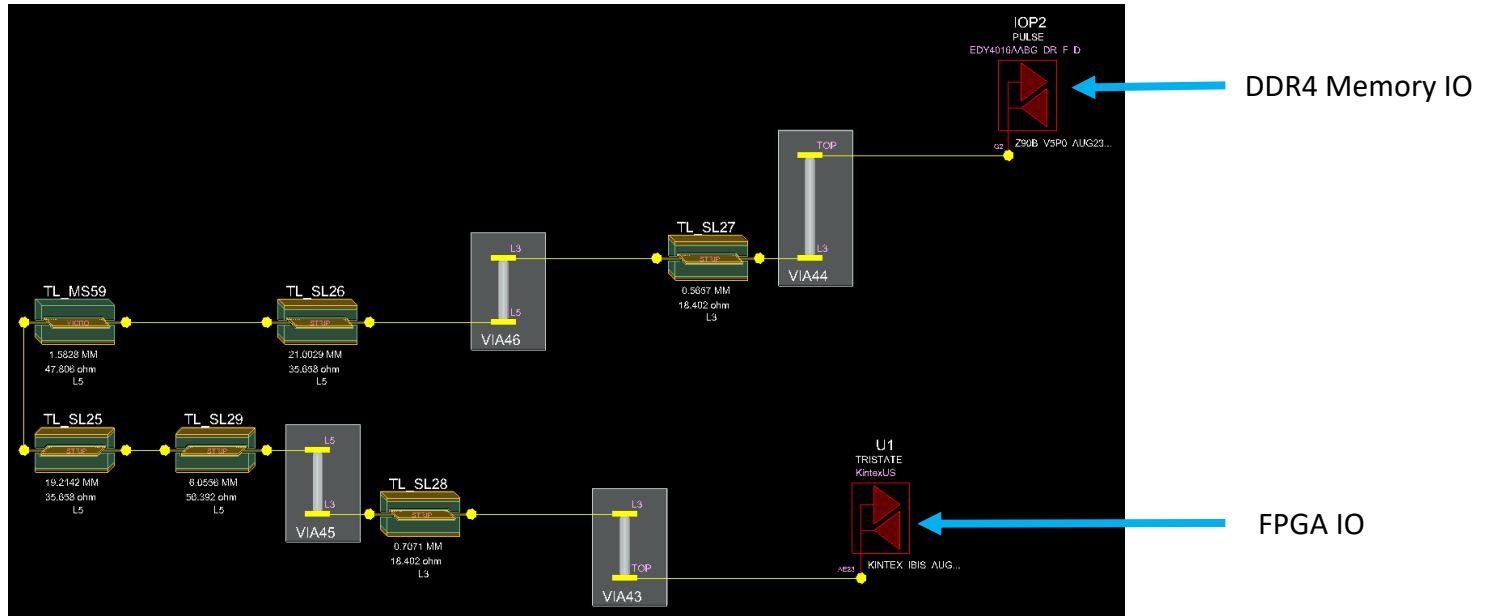


- We could see eye opening (This is a kind of timing)
- Clearance: Eye Mask <-> Signal



Focus on One Bit

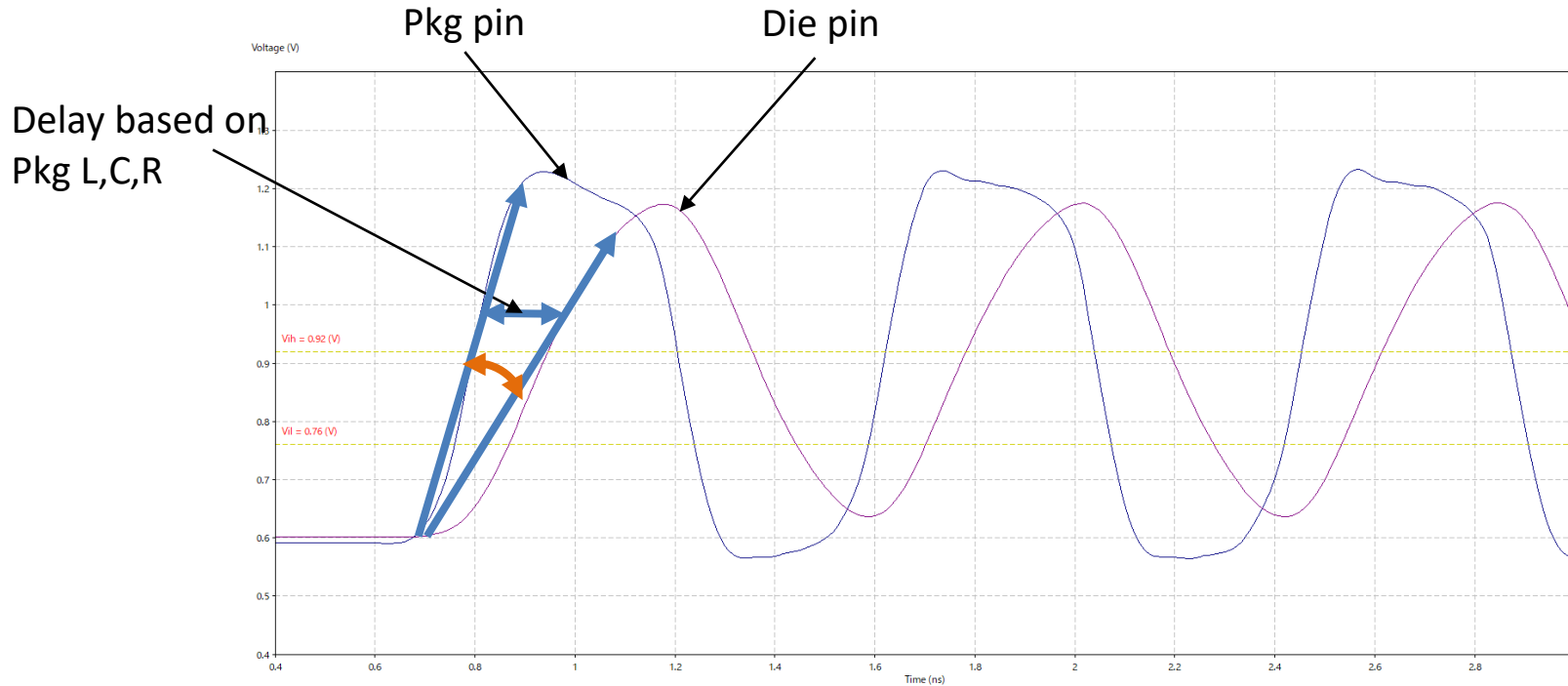
Test Topology (Extracted DQ)





What do you see with SI simulation ?

DQ at Controller: Data Read

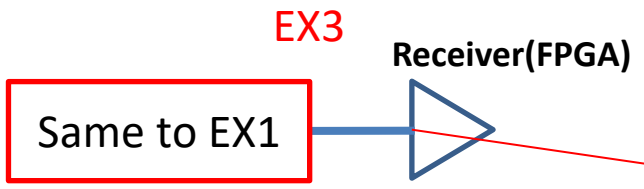
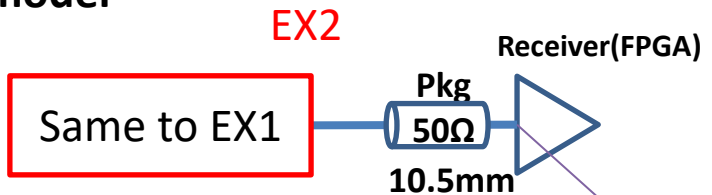
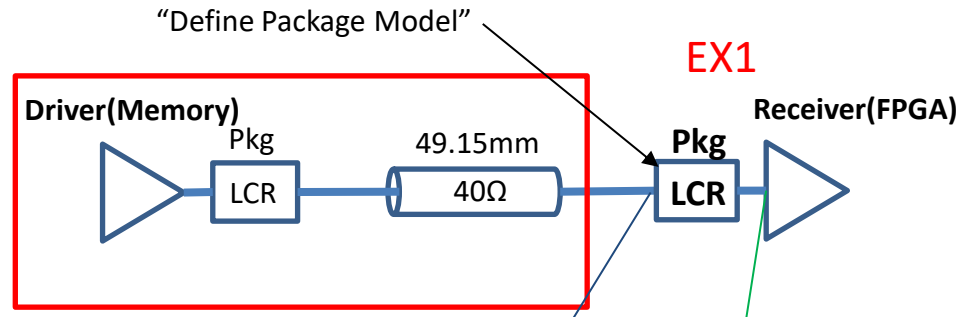


- Rising time of Die pin is slower than Pkg pin
- Which curve is used for measurement?
 - Die pin should be used but this curve is...

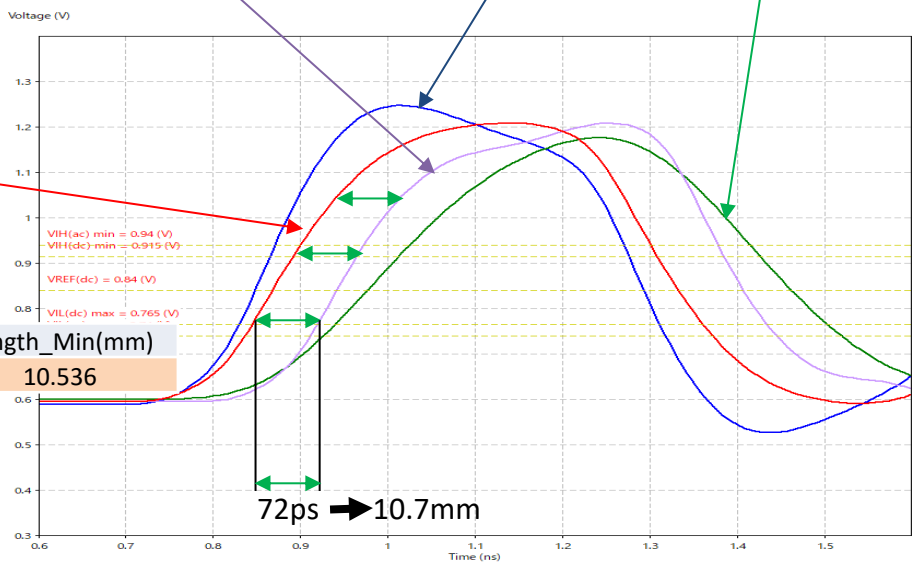


Package Effect on SI simulation

- EX1: Use [Define Package Model]
- EX2: Replace Pkg model with T-Line
- EX3: Remove Pkg model



Package stub length of EX2 is given as 'Package stub length sheet' as below.



PinName	NetName	Delay_Max(pS)	Delay_Min(pS)	Length_Max(mm)	Length_Min(mm)
AE23	DQ0	70.274	69.575	10.531	10.536

Maybe EX2 is more realistic.



IBIS Specification Supports PKG Length

- [Pin Numbers] support Package stub length
 - Support distributed Pkg model (with [Number of Sections] and with Len > 0)
 - Ex:
[Pin Numbers]
A1 Len=0 L=1.2n/ Len=1.2 L=2.0n C=0.5p R=0.05/ Len=0 L=2.0n C=1.0p/
- [Define Package Model] doesn't support length with [Model Data]
 - Support LCR matrix only
- Which model is better ?
 - I want to do both
 - But I have never seen “Len” at [Pin Numbers] keyword

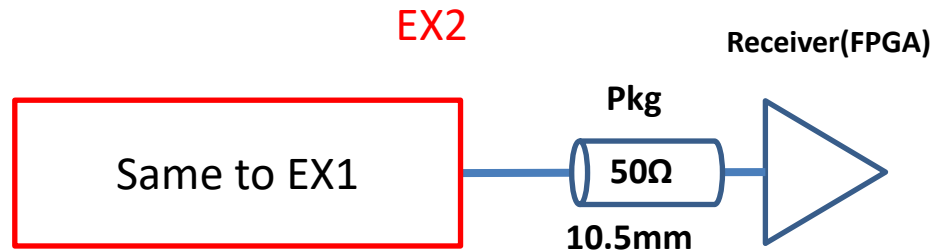


How to Treat Package Length

- Lumped constant (LCR) is useful for SI/PI simulation
- Lumped constant (LCR) is not sufficient for Timing Verification
- Best is Package S-Parameter model
 - Many SI simulators don't support S-parameter
- EX2 (Page15) is required in use T-Line (impedance)
 - Most of IBIS models don't support "Len" parameter
 - Impedance is not specified anywhere



Required Information for Timing Verification



- Package impedance is required in [Pin Numbers] section
- Package impedance and Length are required in [Define Package Model]



END