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Silicon to Software™

Study on potential feature additions for bit-by-bit simulation technique to address the DDR5 requirements.

Asian IBIS Summit, Tokyo, Japan
November 12, 2018

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Synopsys Inc.

Background: Increasing Challenges in DDR4 and beyond

Achieving Low BER with ISI, Crosstalk, SSO and Clock/Random Jitter

- Lossy coupled transmission lines
  - Inter-Symbol Interference (ISI) and Crosstalk co-exist
- Highly nonlinear transistor buffer
  - Tens of thousands of transistors
  - Simultaneous Switching Operation (SSO) strongly affects driver timing (Power Supply Induced Jitter : PSIJ)
- Low Bit Error Rate (BER) requirement for (LP)DDR4
  - DDR3 and earlier try to achieve 100% pass with a guard-banded (derating table) setup
  - (LP)DDR4 admits random (unbounded) jitter, achieve BER ~= 10^{-16} (*1)
- Equalizer (FFE and/or DFE) requirement for DDR5

Conventionally: 100~1000 bit transient

Quick yet thorough design prediction becomes essential for complex/high-speed DDR systems

Now and future: convolution/superposition techniques and pure SPICE transient simulation should both be used

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Analysis Flow for DDR

To capture nonlinear, multi-lane and single ended system performance

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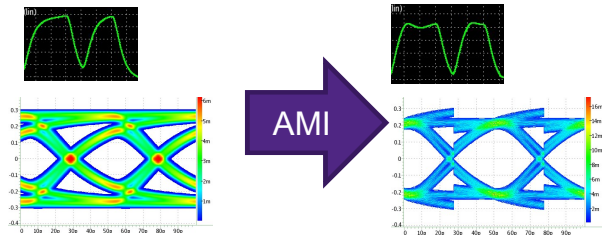
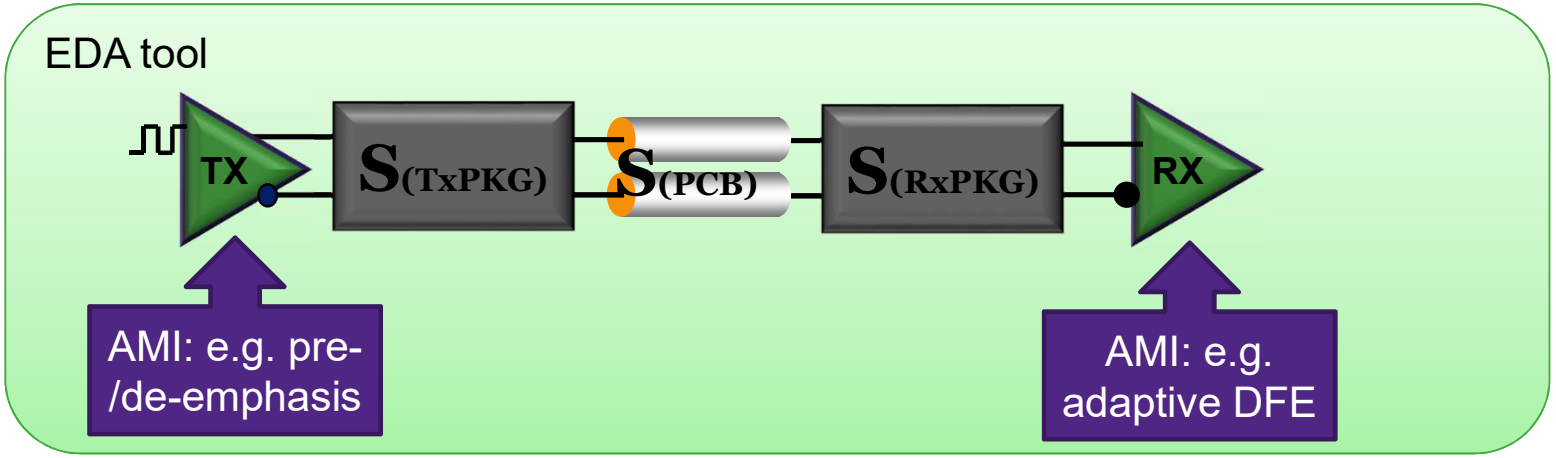
Introduction to IBIS-AMI

- IBIS-AMI: Algorithmic Modeling Interface
  - Complex waveform filters by programing languages (e.g. C/C++)
    - waveform in, waveform out
  - Interface with EDA tools (simulators)
  - A model consists of two files
    - Compiled runtime library (binary) file : *.dll (windows), *.so (unix)
    - Parameter control (text) file : *.ami
  - IBIS-AMI flow requires channel analysis specific information
    - Unit Interval, Bit segment size, impulse response etc.





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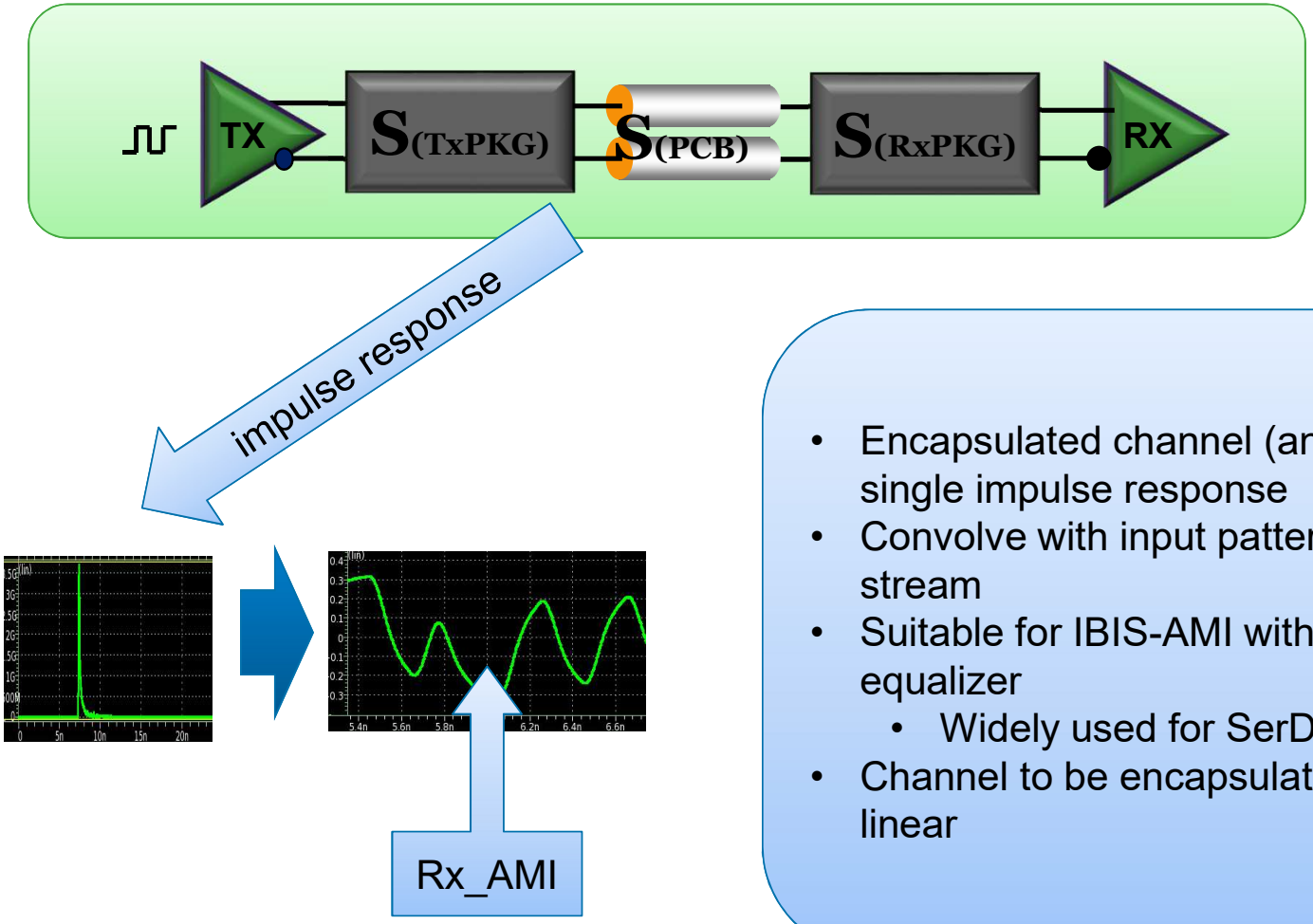
Simulation technique comparisons (1: convolution)



- Encapsulated channel (analog part) into single impulse response
- Convolve with input pattern to get an output stream
- Suitable for IBIS-AMI with non-LTI Tx equalizer
  - Widely used for SerDes simulations
- Channel to be encapsulated has to be linear

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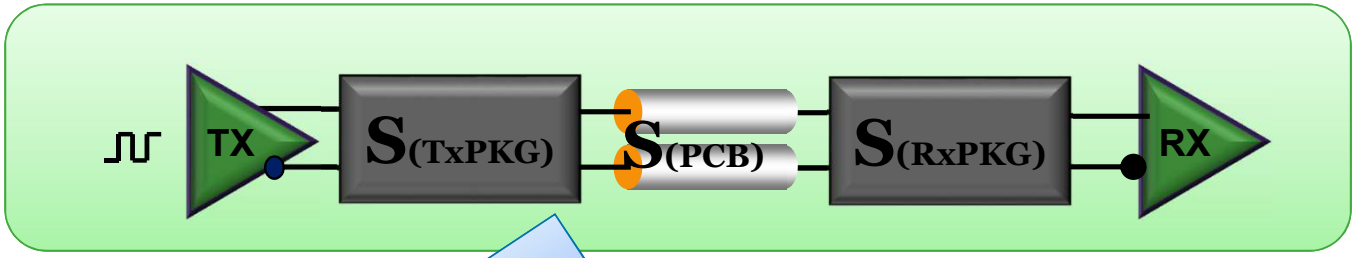
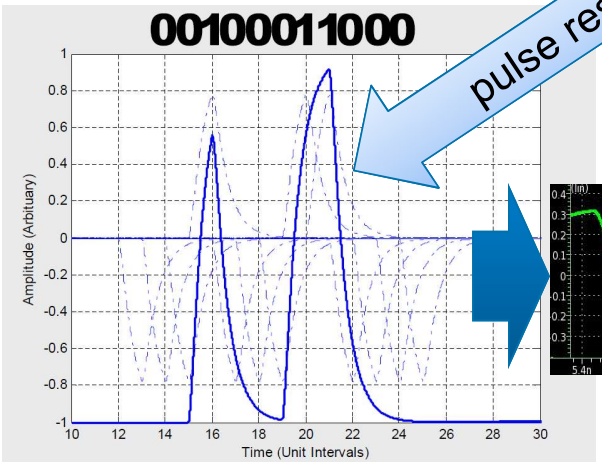
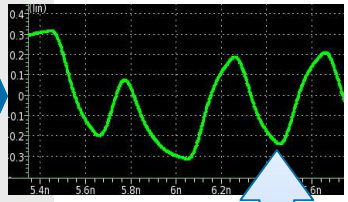
Simulation technique comparisons (2: superposition)





pulse response



Rx_AMI

- Known as StatEye (www.stateye.org)
- Characterize channel responses with edge pattern (pulse) responses
- Superposition to create bit stream output
- Rise/fall asymmetry and nonlinearity can be included in edge pattern (pulse) response
  - Extendable to multi-edge patterns
  - Suitable for single-ended protocol
- Non-LTI Rx-AMI can be taken
- Difficult to make multi-stage flow
  - Difficult to take Tx-AMI model if non-LTI

Anthony Sanders, Mike Resso and John D'Ambrosia, "Channel Compliance Testing Utilizing Novel Statistical Eye Methodology," DesignCon 2004

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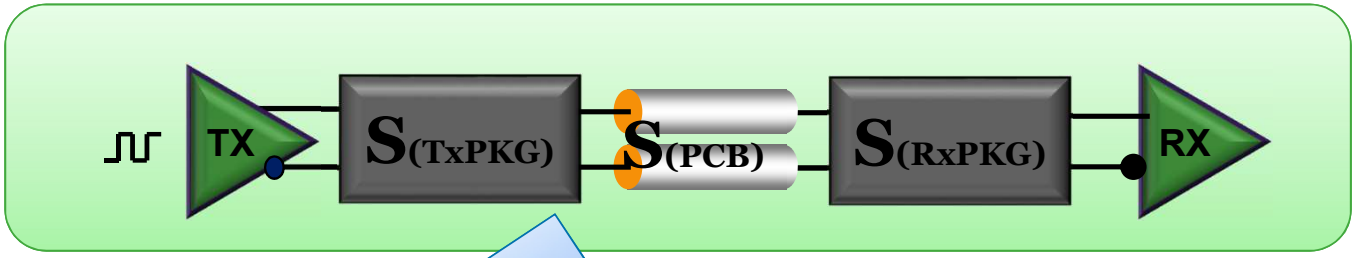
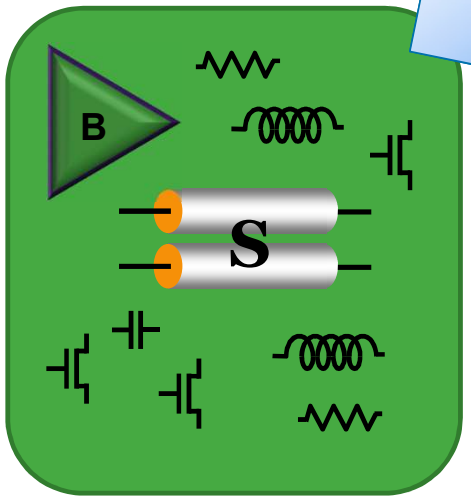
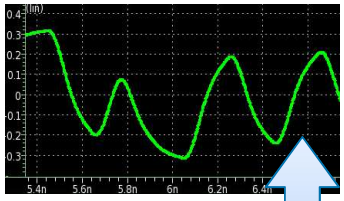
Simulation technique comparisons (3: transient)



Circuit elements





Rx_AMI

- Captures any non-LTI effects
  - Reference result
- Works well with IBIS buffer with composite current model
- SSO and crosstalk effect can accurately be taken
- Time consuming
- Difficult to establish multi-stage flow
  - Difficult to take Tx-AMI model if non-LTI
- Non-LTI Rx-AMI can be taken

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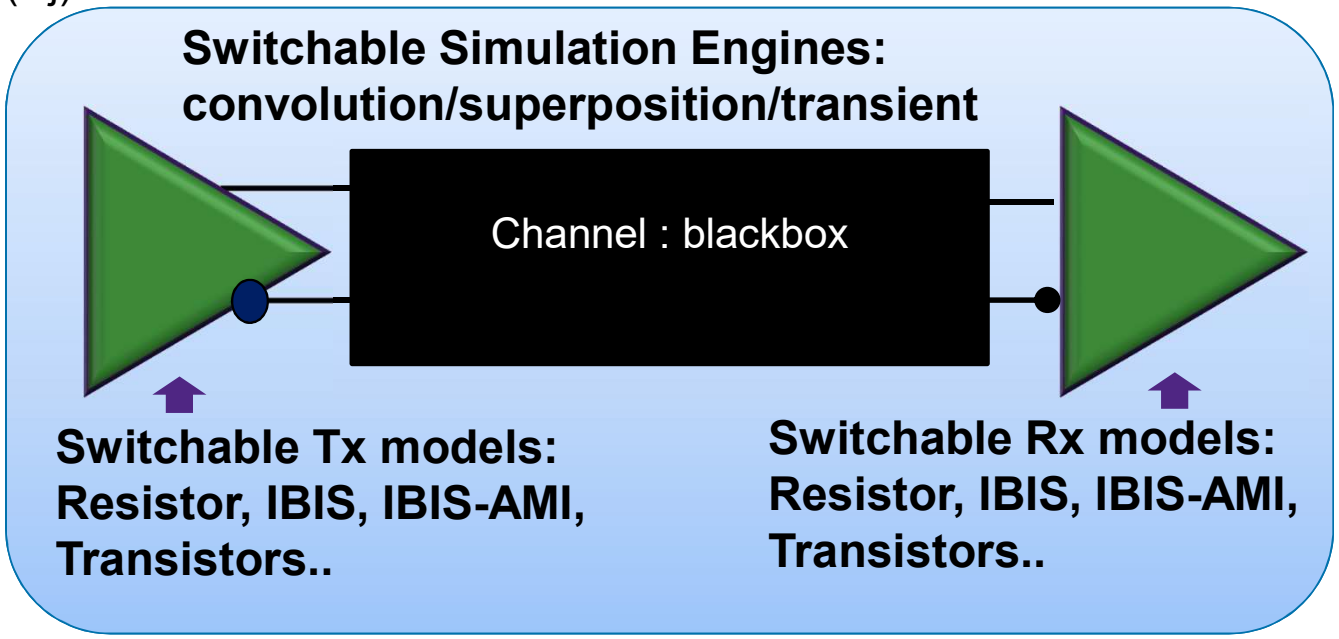
DDR Design Requires Configurable Testbench

- Traditionally DDR designers:
  - Used to use IBIS and/or transistor models for both Tx and Rx
  - Used to use transient with relatively short bit length
- Current and upcoming DDR specs additionally requires:
  - Complex equalization esp, Rx DFE
  - Requires statistically defined jitter (Rj) and BER down to 10^{-16}

EDA tool and MODEL needs to support configurable (switchable) testbench.



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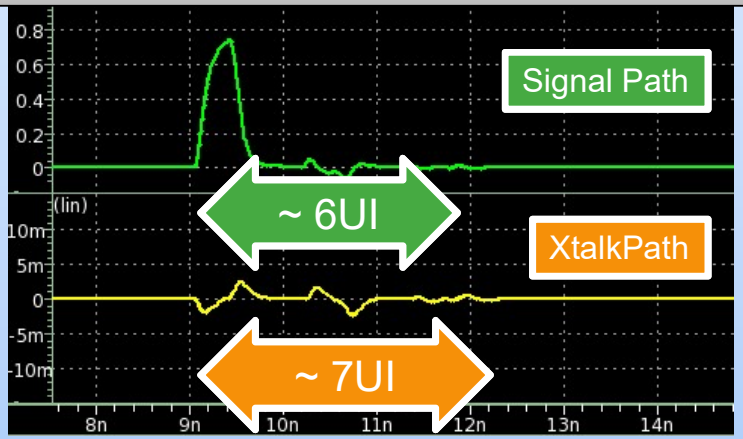
Potential Analysis Flow for DDR5

- (short) transient to create reference data
  - deterministic component: ISI + Crosstalk (and Equalization)

Single Bit Response
(ISI: how many subsequent bits are affected)



Possible ISI (required TSTOP)
~= 2^6 x 2^7 = 4096 bits

- Superposition flow for long bit sequence

Tx with Equalization	• Edge pattern (e.g. pulse) response with
	  • IBIS' driver schedule
	  • Behavioral filter
	  • Transistor models

SSO	• Edge pattern (e.g. pulse) response with
	  • IBIS composite current model
	  • Transistor model

Xtalk/ISI/ Rj/PSIj	• Edge response superposition
Rx with Equalization	• IBIS-AMI • with external clock extension

Correlation study

Overall system performance

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Capturing SSO in Eye Diagram Generation

Create a Power Supply Induced Jitter (PSIJ) Distribution and Apply to Signal (DQ) Eye Diagram

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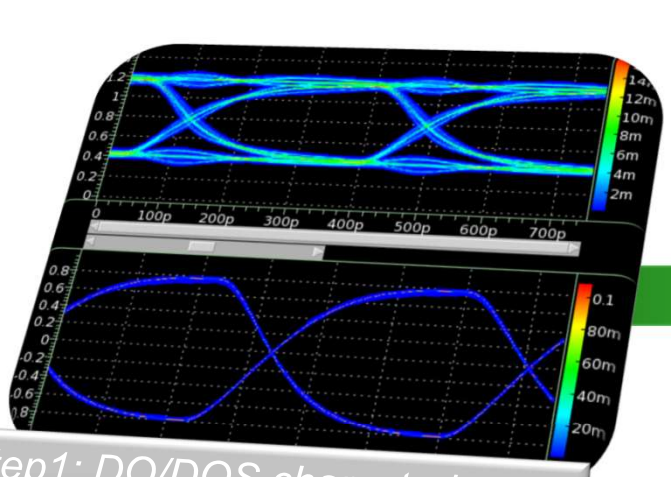
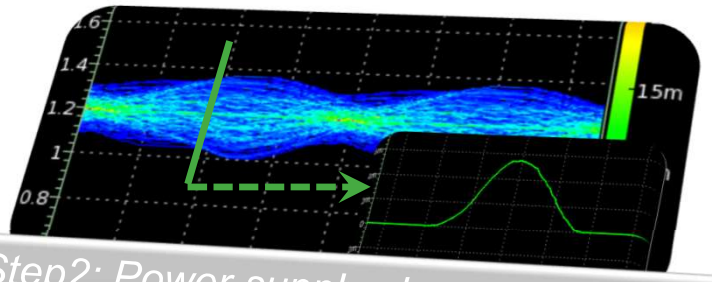
Two Step Approach

DQ/DQS Characterizations plus SSO Characterization



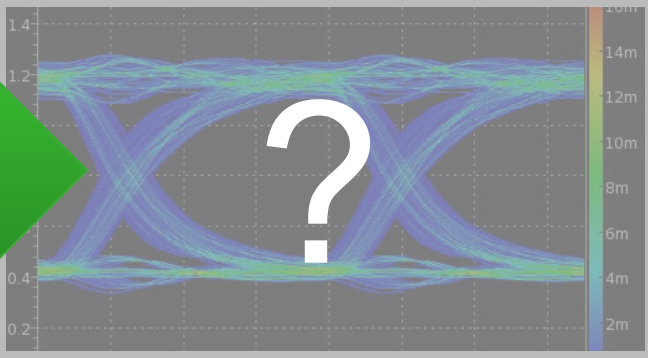
Step1: DQ/DQS characterization to capture inter-symbol interference (ISI), crosstalk and clock jitter



Step2: Power supply characterization for Simultaneous Switching Operation (SSO) effect and derive Power Supply Induced Jitter (PSIJ) profile

convolution

Overall Channel performance



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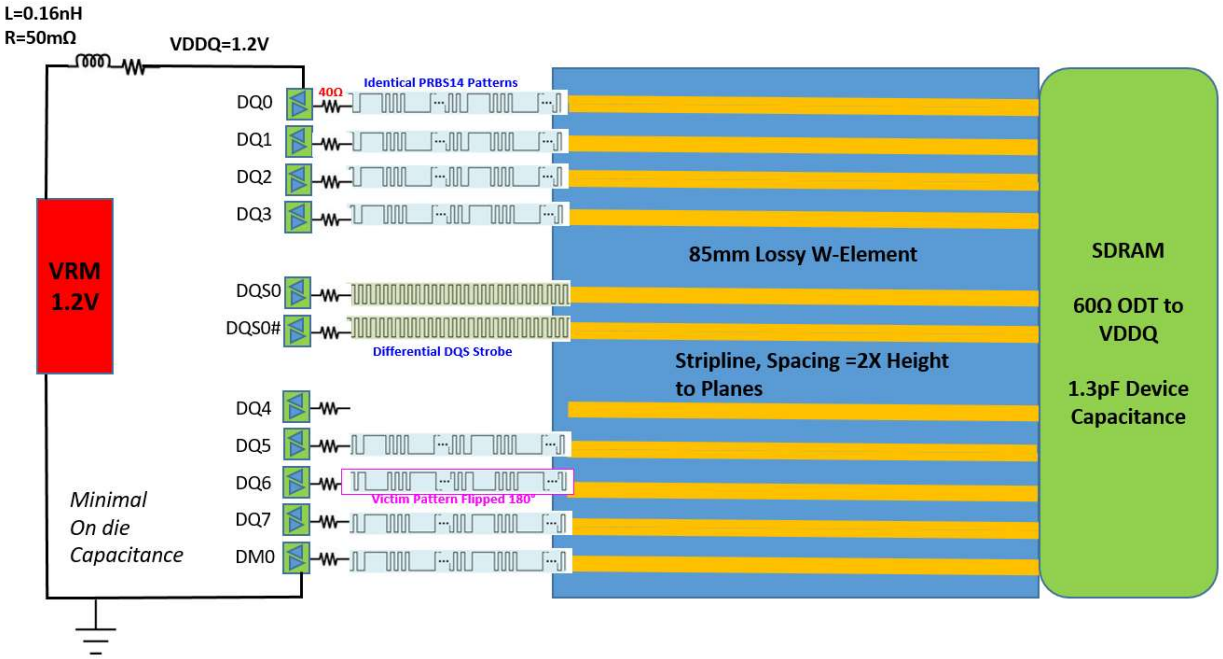
Target System (*1)

- DDR4 with 2667Mbps
- Simulate a single byte lane during a write operation
- Identical PRBS patterns to excite SSO effects. Then flip one bit to excite odd mode coupling on one of the bits.
- Minimal decoupling capacitor included
- 85mm of 51Ω stripline
- 60Ω ODT to VDDQ



(*1) John Ellis, “Capturing (LP)DDR4 Interface PSIJ and RJ Performance Accurately, Reliably and Quickly,” track 4, DesignCon 2017

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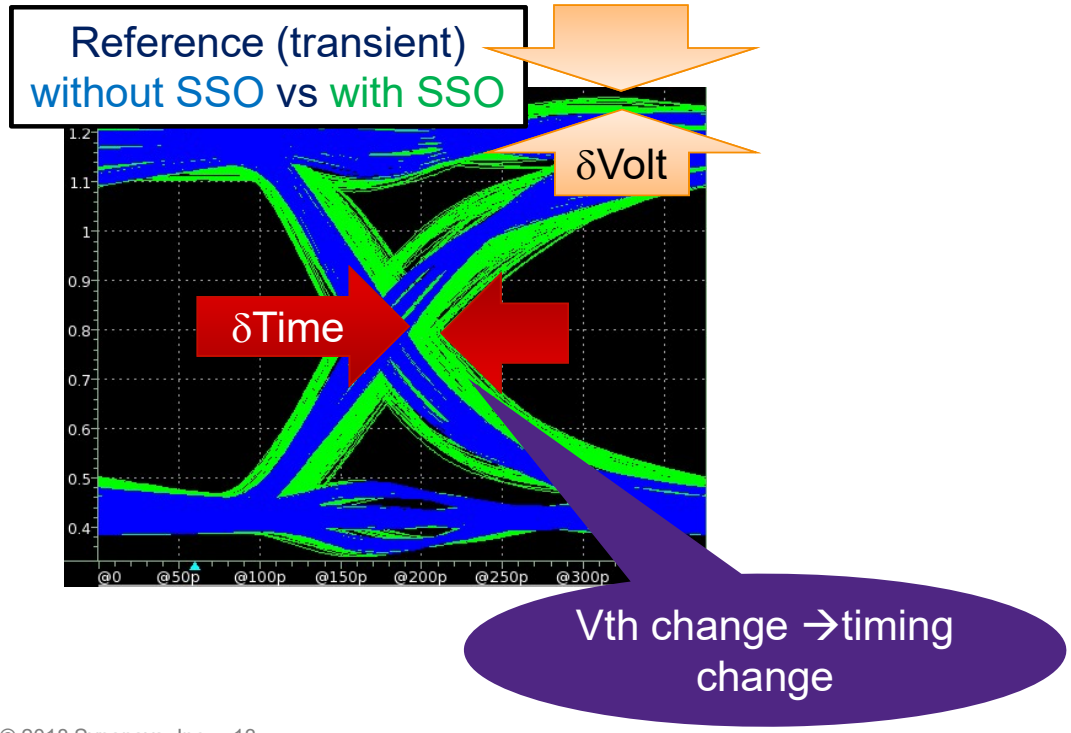
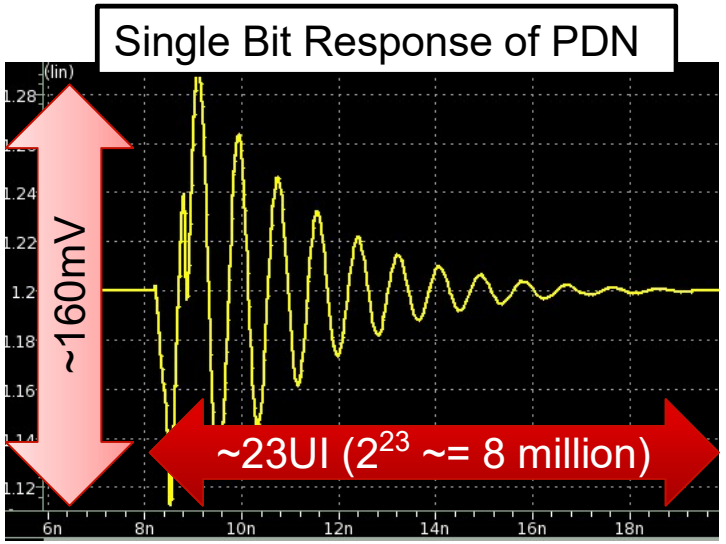
Challenges in SSO Noise Characterization

SSO Translates to Timing Uncertainty

- SSO is input pattern dependent
- Stronger timing variation than voltage variation
- Power Delivery Network (PDN) has long time constant (deeper ISI)





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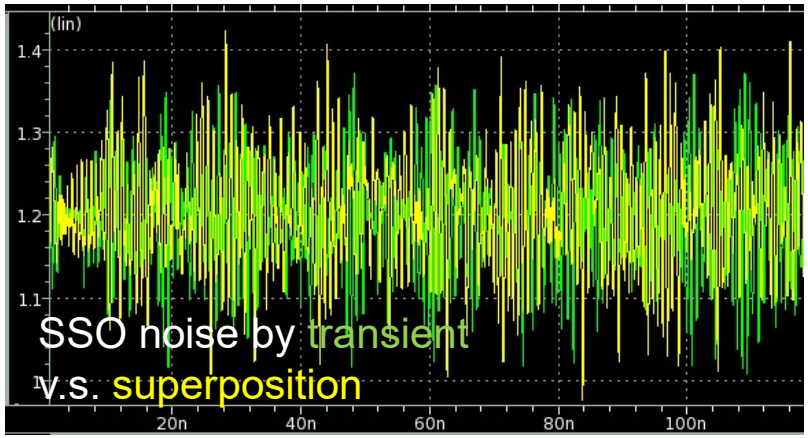
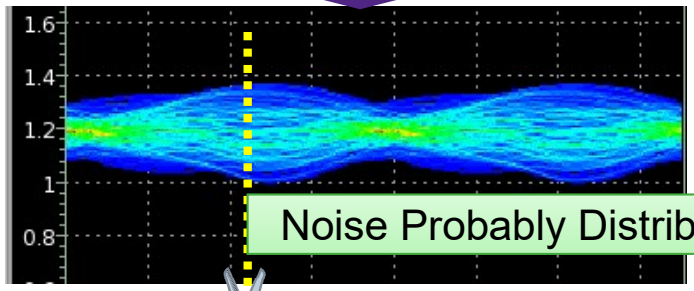
SSO Noise Probability Density Function (PDF)

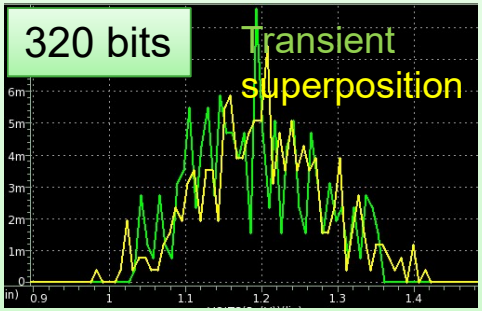
PDN: Deep ISI, Relatively Linear Network → Edge response superposition for SSO-PDF

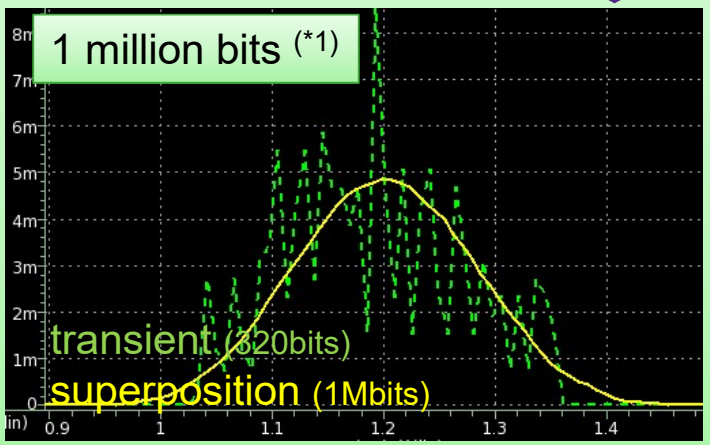


PDF (Noise Eye Diagram)



Noise Probably Distribution





(*1): StatEye runtime ~20sec

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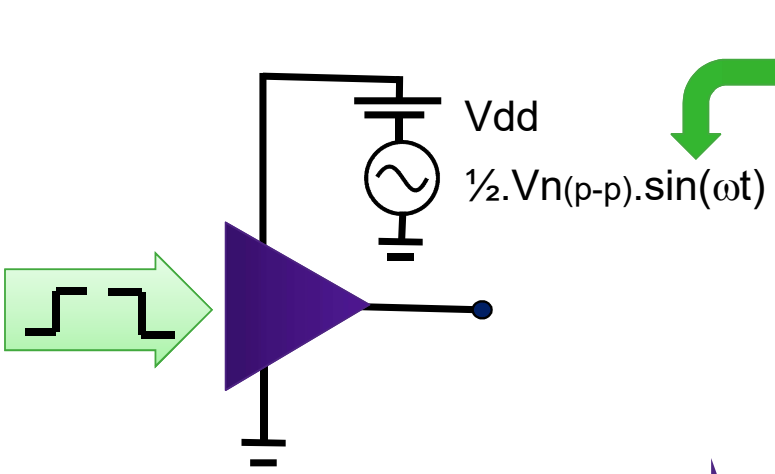
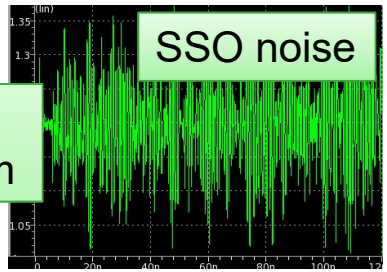
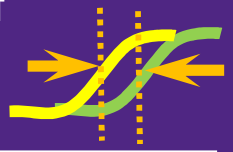
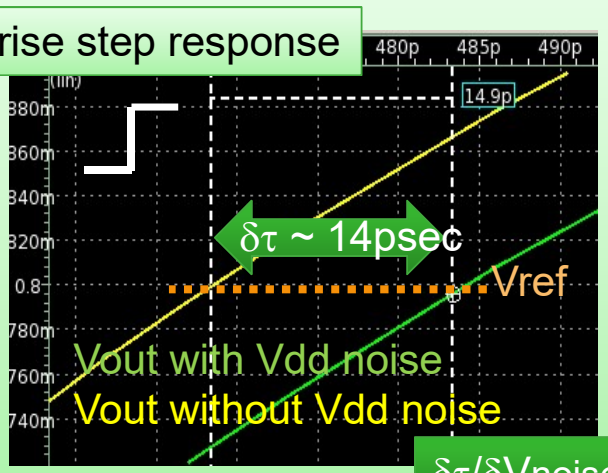
Translate Voltage Noise to Timing Jitter

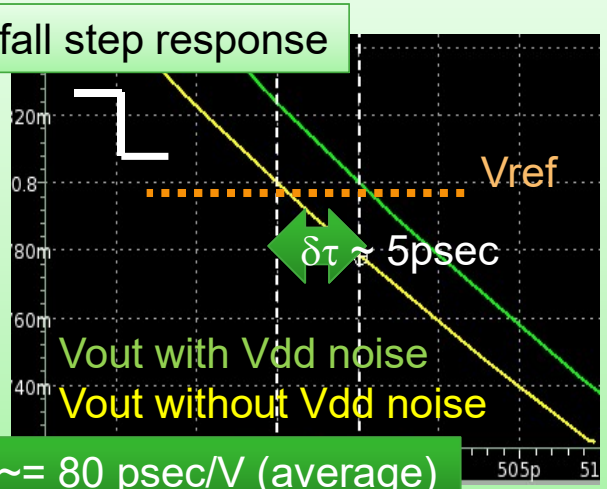




- Single Buffer Transient (rise/fall step) with sin(ωt) noise on Vdd
- Measure δτ (with v.s. without noise) on Vout at Vref
- Compute δτ/δVnoise







δτ/δVnoise ~= 80 psec/V (average)

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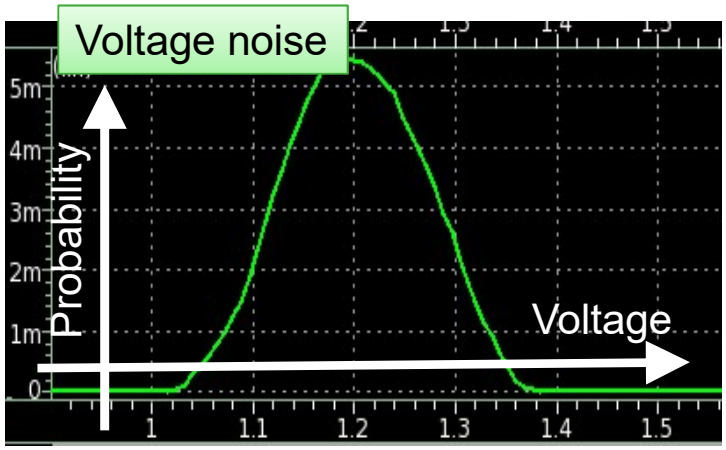
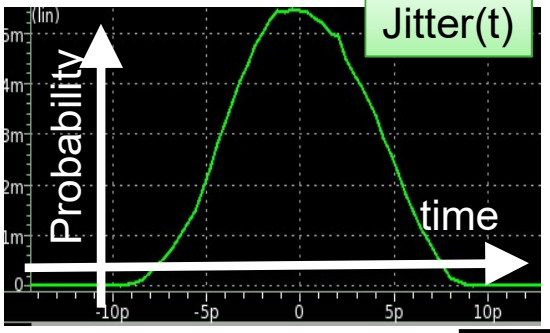
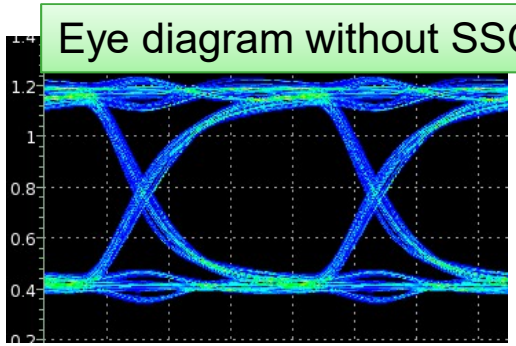
Applying SSO Timing Jitter

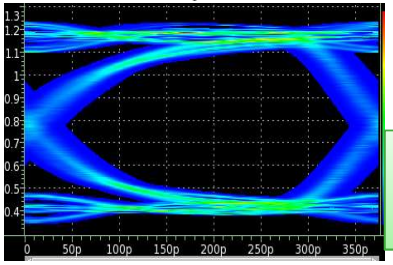


Noise(v) to Jitter(t)





convolution



Overall system performance

1. Applies $\delta\tau/\delta V_{noise}$ ~= 80 psec/V (average) to Voltage noise
2. Convolute timing jitter probability with non-SSO eye diagram

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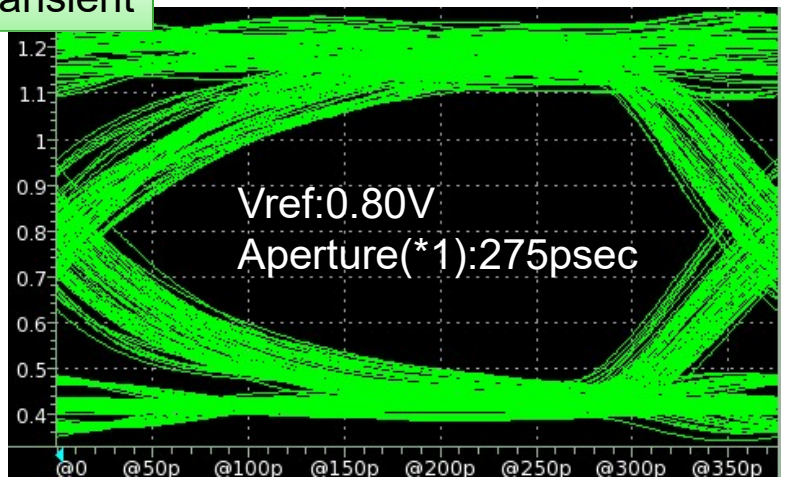
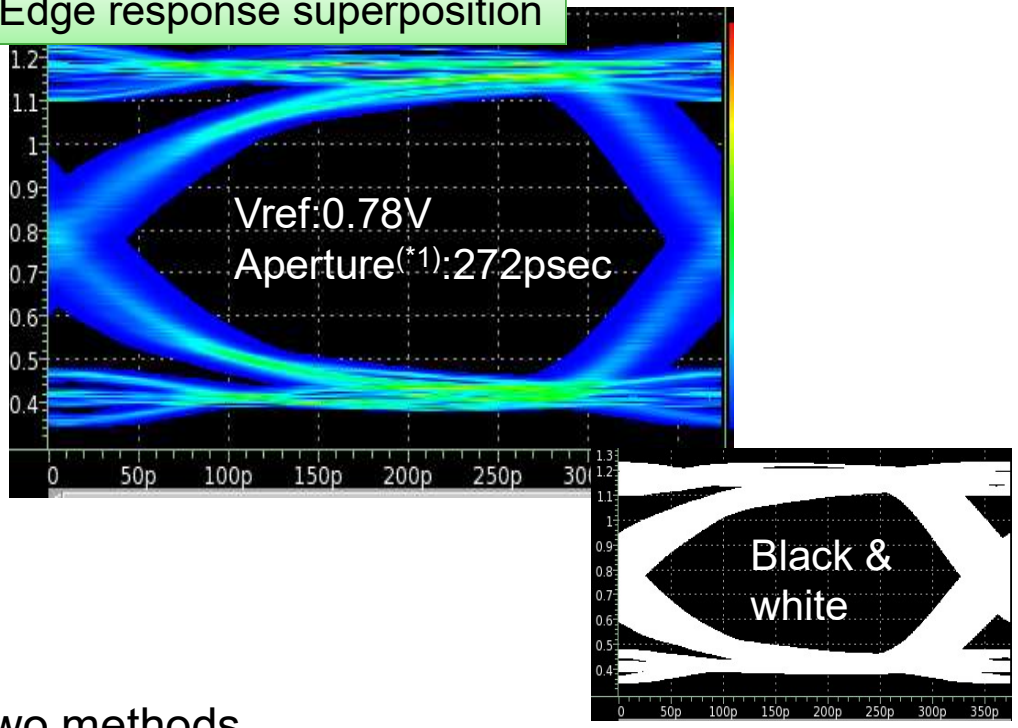
Correlation Study with Transient

transient



Edge response superposition



- Good agreement between two methods

(*1): measured at V=Vref +/- 60mV

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External Clock Extension for IBIS-AMI

For DDR5

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Proposal in JEDEC for DFE with DQS

8.10 Rx Stressed Eye - Q3'18 Ballot #1848.18A Proposal

The stressed eye tests provide the methodology for creating the appropriate stress for the DRAM's receiver with the combination of ISI (both loss and reflective), jitter (Rj, Dj, DCD), and crosstalk noise. The receiver must pass the appropriate BER rate when the equivalent stressed eye is applied through the combination of ISI, jitter and crosstalk.

Figure 154 — Example of Rx Stressed Test Setup in the Presence of ISI, Jitter and Crosstalk

- (Rx) IBIS-AMI flow needs extensions
  - Take external clock for bit slicer
  - Take external clock in eye diagram generation

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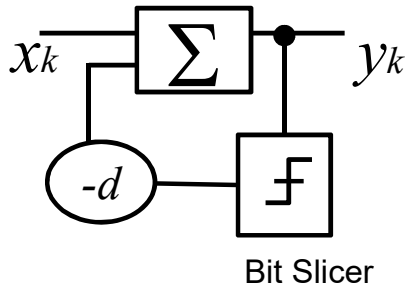
Potential Interface addition in IBIS-AMI

- Use “double **`*clock_times`**” array
  - Conventionally used to let the EDA tools know the CDR clock ticks (output)
  - For DDR5, this array for the EDA tools to let IBIS-AMI model know the external clock ticks (input)

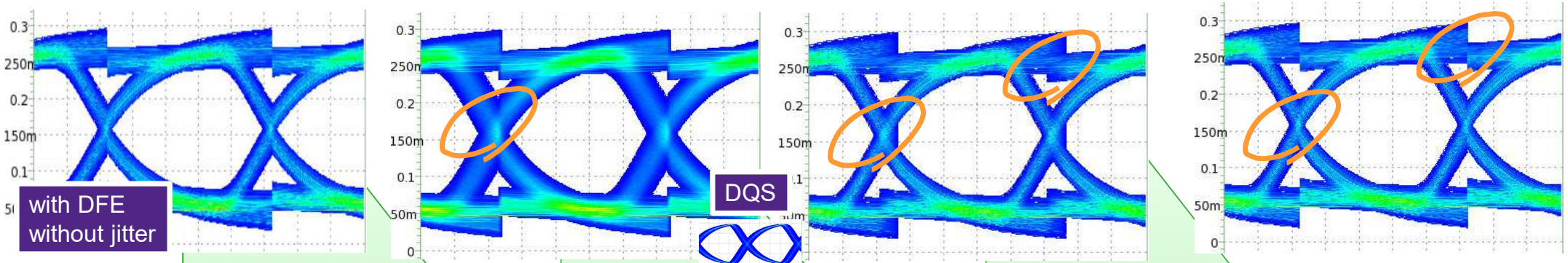
```
long AMI_GetWave (double *wave,
      long wave_size,
      double *clock_times,
      char **AMI_parameters_out,
      void *AMI_memory)
```

- Additional reserved parameter “External_Clock”
  - Has to be included in IBIS-AMI string when specified : **`(My_DFE(External_Clock True)(…))`**
  - Let EDA tool prepare clock ticks stored in **`*clock_times`** array

Result 1: Correlated Jitter Case



- Apply identical sinusoidal jitter (Sj) sequence to both DQ and DQS
- DQ has an Rx side DFE with (tap, weight) = (1, 0.02), (2, 0.01)



Add Sj (10ps) to DQ:
- jitter narrows the opening

Use non-ideal clock (Sj=10ps) in eye generation:
- Jitter suppressed
- DFE timing uncertain

Use non-ideal clock (Sj=10ps) also in DFE:
- Jitter suppressed
- DFE timing cleaned

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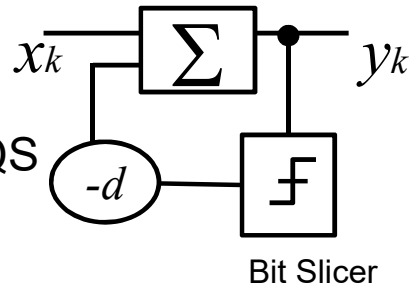
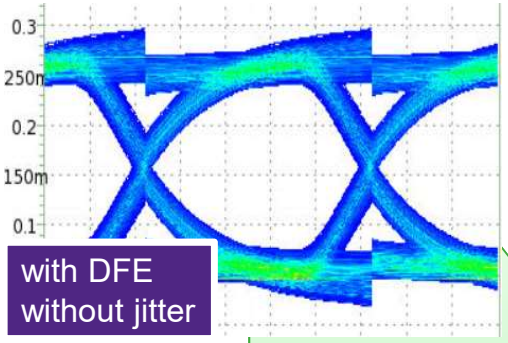
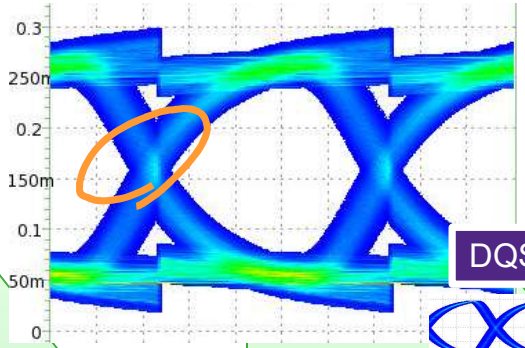
Result 2: Uncorrelated Jitter Case



- Apply sinusoidal jitter (Sj) sequence with different frequency to DQ and DQS
- DQ has an Rx side DFE with (tap, weight) = (1, 0.02), (2, 0.01)

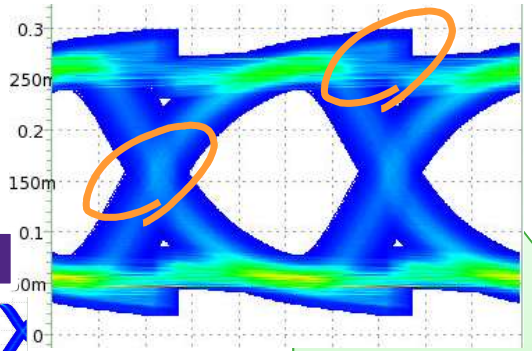


with DFE without jitter

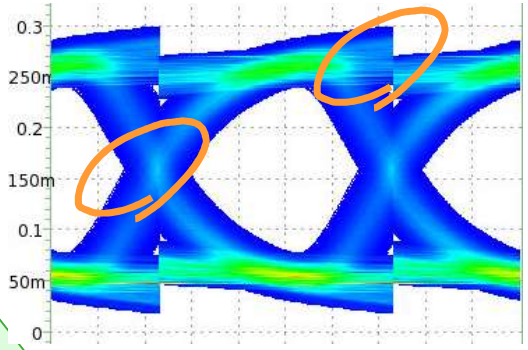


DQS

Add Sj (10ps) to DQ:
- jitter narrows the opening



Use non-ideal clock (Sj=10ps) in eye generation:
- Jitter grows
- DFE timing uncertain



Use non-ideal clock (Sj=10ps) also in DFE:
- Jitter remains
- DFE timing cleaned

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Conclusions

- Discussed about challenges and requirements for DDR4/5 designs
  - Combinational use of multiple methods would be essential
  - Comparison among multiple analysis engines and models
  - Potential flow for DDR5 to capture ISI/nonlinearity/crosstalk/SSO/Equalizer
- Demonstrated two step approach to take SSO effect in DDR analyses
  - Generated SSO noise probability density
  - Determined Voltage noise to timing jitter translation factor
  - Achieved good correlation between transient and edge response superposition methods
- Discussed IBIS-AMI enhancement to take external clock ticks
  - External clock has to be taken into account both in DFE and in eye diagram generation

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Thank You