Simulation Technology for Memory Designers in DDR4/5

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DDR5 is coming

The data eye is closing

Memory channel BW limited
Rj improving slowly
Xtalk effects increasingly severe
Agenda

• DDR4 Highlights
• 4 challenges for memory designers in DDR4/5
• A Look at JEDEC’s current DDR5 proposal
• How will we model DDR5 devices in simulation?
• A side-by-side comparison of some approaches for DDR5 simulation
## LP/DDRx Highlights

<table>
<thead>
<tr>
<th>Specification</th>
<th>DDR3</th>
<th>DDR4</th>
<th>LPDDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate / Pin (Mbps)</td>
<td>800 - 2133</td>
<td>1600 - 3200</td>
<td>1333 - 4266</td>
</tr>
<tr>
<td>Bus Width</td>
<td>4, 8, 16</td>
<td>4, 8, 16</td>
<td>2, 4, 16, 32</td>
</tr>
<tr>
<td>Voltage</td>
<td>1.5 / 1.35</td>
<td>1.2</td>
<td>1.1</td>
</tr>
<tr>
<td>Vref</td>
<td>External Vref (=Vref/2)</td>
<td>Internal Vref</td>
<td>Internal Vref</td>
</tr>
<tr>
<td>Signal Evaluation</td>
<td>Setup/Hold time</td>
<td>Mask (considered BER)</td>
<td></td>
</tr>
<tr>
<td>Data I/O</td>
<td>CTT (Center Tapped Termination)</td>
<td>POD (Pseudo Open Drain)</td>
<td>LVSTL (Low Voltage Swing Terminated Logic)</td>
</tr>
</tbody>
</table>
LP/DDRx Highlights

- Lower VDD voltage and Pseudo-Open Drain (POD) reduces power consumption by 40%.
- Internal VREF training performed within the IC receiver, to optimize VREF level. Retraining at regular intervals.
- Data lines are calibrated at the IC, to reduce their skew to the strobe.
- Data Bus Inversion (DBI).
Shrinking eye due to package, PCB and connectors
Today’s Disruption

The fuzzy eye takes over

LP/DDR4 receiver requirements defined by masks instead of setup / hold and DC voltage swings

- Simpler definition of DRAM requirements and system design.
- More compatible with LPDDR4 training procedures.
- Eliminates troublesome slew rate derating.
- Bit Error Rate (BER) spec recovers timing and noise margin.

Fundamental paradigm shift with DDR4

Source: JEDEC Standard JESD209-4B/JESD79-4B
NOTE 2  The design specification is a BER < TBD. The BER will be characterized and extrapolated if necessary using a dual dirac method.

BER = Probability that DRAM will sample outside the mask region

- DAC quantization error
- Comparator hysteresis
- Comparator offset error
- Internal noise and crosstalk

Region where DRAM receiver is most likely to sample input signal

- Latch timing
- Clock receiver hysteresis
- DRAM internal skews
- Internal noise converted to jitter

Source: JEDEC Standard JESD209-4B
Challenges for DDR4/DDR5

Challenge #1

Timing margin will be further eroded by ISI and RJ; The Rx Mask becomes the contract between Controller and DRAM in order to achieve at least prescribed BER (1e-16 for DDR4).

<table>
<thead>
<tr>
<th>Number of UI</th>
<th>BER</th>
<th>Eye Width</th>
<th>Eye Height</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.3e5</td>
<td>7.69e-6</td>
<td>352.72 ps</td>
<td>310.9 mV</td>
</tr>
<tr>
<td>2.80e6</td>
<td>3.57e-7</td>
<td>347.52 ps</td>
<td>288.3 mV</td>
</tr>
<tr>
<td>6.31e7</td>
<td>1.58e-8</td>
<td>339.70 ps</td>
<td>275.8 mV</td>
</tr>
<tr>
<td>1.10e8</td>
<td>9.13e-9</td>
<td>339.06 ps</td>
<td>271.1 mV</td>
</tr>
<tr>
<td>1e9</td>
<td>1e-9</td>
<td>336.45 ps</td>
<td>265.6 mV</td>
</tr>
</tbody>
</table>

Source: JEDEC Standard JESD209-4B

EH and EW keep shrinking at lower BER
Challenges for DDR4/DDR5

Challenge #2

Crosstalk.
As the speed increases, so does the amount of coupling between adjacent neighbors.

Even at slow speed grades the additional noise reduces margin to mask!
Additional jitter and amplitude noise due to Simultaneous Switching Noise (SSO/SSN) and other time-varying distortions.

No PDN – Ideal VCCO

With SSON

Challenges for DDR4/DDR5
Channel attenuation and ISI becomes more significant so tunable Equalization (De-emphasis, DFE) on Tx and Rx become necessary to deal with closed eyes.
De-Emphasis Controller

Algorithm for determining Equalization And De-Emphasis

Means for measuring signal quality

3-Tap De-Emphasis

Control

Tx

Mode Reg

Longer Latency for Training

Simpler to Characterize

Gain t2 t3 t4 t1

DAC

DFE

DQS

Rx

Control

Vref_offset

FF
Common-mode problem in IBIS-AMI

- IBIS-AMI only defines differential signal. Common-mode (CM) in single-ended (SE) signal is undefined and thrown away.
- IBIS-AMI waveform always centers at 0V. Signal level is off compared to Vref.
Common-mode implications

- One of the key implications of having the DC offset thrown away, is that margin to the **Rx BER Mask requires correct DC offsets** (to know where to place the mask).
- In other words, there is a single Vref for the entire byte-lane. The spec defines the Rx Mask to be centered on **Vcent_DQ**.
Asymmetric rise and fall edges lead to data DCD jitter and crossing level shift, degrading timing and voltage margins with respect to Rx mask.

- Pull-up and pull-down behaviors depend on the analog channel and therefore must be included in analog channel response characterization.

- AMI has only one impulse response and can’t capture difference between rise and fall edges. Response needs to be characterized separately for each edge.

- Asymmetry between rise and fall edges is much more severe in single-ended signal than in differential signal. It gets worse as data rate increases.

- With different responses for different edges, IBIS-AMI’s convolution scheme is no longer applicable. Moreover, Tx GetWave output waveform becomes useless as a result.
# Current Proposals in the EDA Community

## DDR5 approaches

<table>
<thead>
<tr>
<th>Statistical DDR Bus</th>
<th>IBIS-AMI</th>
<th>SPICE + Verilog-A</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Sim speed:</strong> Very Fast</td>
<td><strong>Sim speed:</strong> Fast</td>
<td><strong>Sim Speed:</strong> Very Slow</td>
</tr>
<tr>
<td><strong>Pros:</strong></td>
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<td><strong>Pros:</strong></td>
</tr>
<tr>
<td>- Calculates ultralow BER contours (e.g. 1e-16) for Rx BER mask</td>
<td>- Well-defined model interface / concealment of IP</td>
<td>- Captures all non-linear and time-varying effects</td>
</tr>
<tr>
<td>- Correct Eye Shape and DC offset!</td>
<td>- Can support both statistical and bit-by-bit simulations</td>
<td>- <strong>Impractical</strong> to simulate enough bits to ever extrapolate BER contours accurately to 1e-16!</td>
</tr>
<tr>
<td>- Finds optimal DFE tap weights</td>
<td>- Future possibility for back-channel adaption</td>
<td>- Sharing of encrypted HSPICE models requires HSPICE</td>
</tr>
<tr>
<td>- In the future can be extended to support Bit-by-Bit mode</td>
<td>- <strong>Cons:</strong></td>
<td>- Verilog-A implementation complexity and requires compiled Verilog-A for IP protection (not supported in all tools)</td>
</tr>
<tr>
<td>- Simplicity of EQ modeling</td>
<td>- <strong>Cons:</strong></td>
<td>- Simulator support for sweeps?</td>
</tr>
<tr>
<td><strong>Cons:</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- No non-linear or time-varying effects.</td>
<td>- Incorrect Eye-shape and DC offset</td>
<td></td>
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<tr>
<td>- IP protection not standardized</td>
<td>- Complexity of modeling</td>
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