



# A PRACTICAL METHODOLOGY FOR SERDES DESIGN

Asian IBIS Summit, Tokyo, Japan, November 12, 2018

Authors:

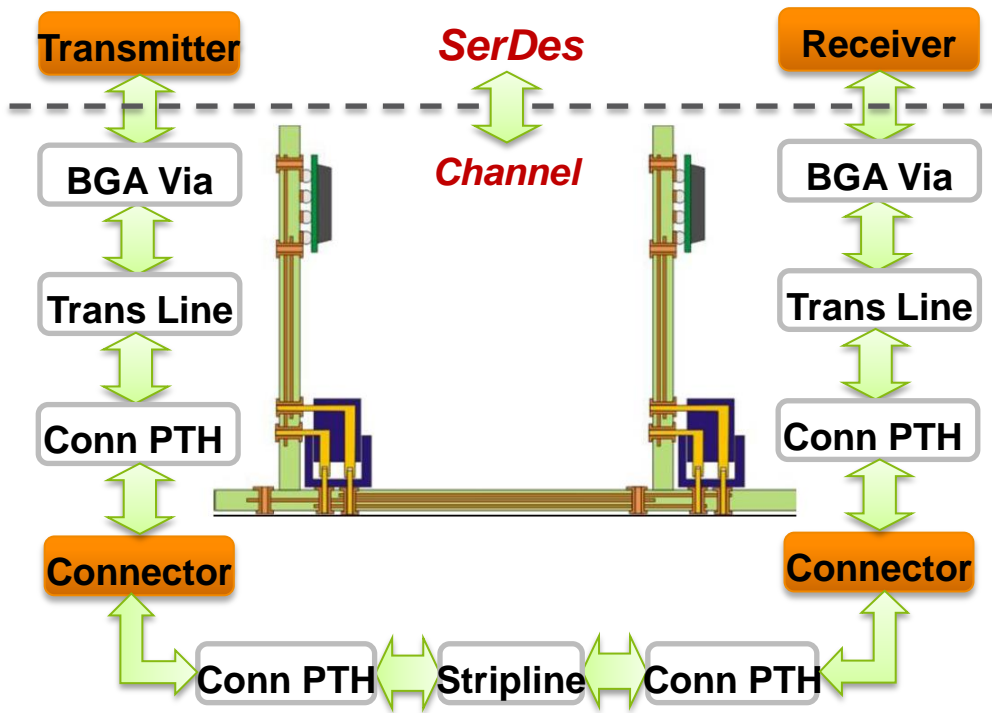
Amy Zhang, Guohua Wang, David Zhang, Zilwan Mahmud,  
Anders Ekholm

# AGENDA



- › Challenges in Traditional Simulation
- › The DOE/RSM Solution
- › CEI 28G-VSR IF Design with DOE
- › Question and Suggestion for IBIS-AMI

# SERDES & CHANNEL



- › Transceiver Equalization
- › Via impedance
- › Trace impedance
- › Trace loss
- › Connector characteristics

# MISSION IMPOSSIBLE



- › Equalization settings
  - FFE
    - › Precursor – 10 taps
    - › Postcursor – 10 taps
  - CTLE
    - › Off; Fixed; Adapt
  - DFE
    - › Off; Fixed; Adapt
- › Via impedance
  - 3 corners (TC/WC/BC)
- › Trace impedance
  - 3 corners (TC/WC/BC)
- › Connector characteristics
  - 3 corners (TC/WC/BC)
- › Trace loss
  - 3 corners (TC/WC/BC)

Assuming 10min for each simulation case:

- Running bits:  $1 \cdot 10^6$
- Sampling per bit: 64
- Block size: 1024

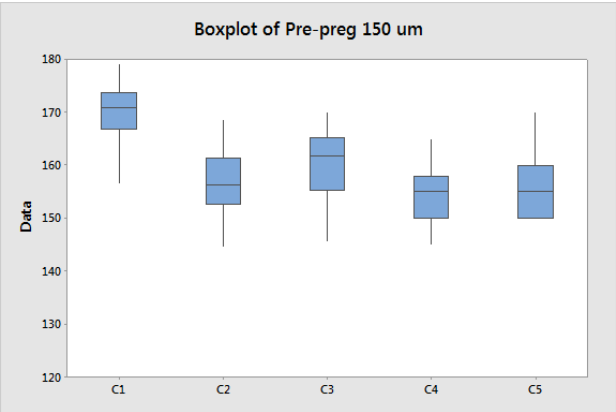
Total time consumption of simulation:

$$\begin{aligned} & 10 \cdot 10 \cdot 10 \cdot 3^6 \\ & = 729000 \text{ minutes} \\ & = \mathbf{506.25 \text{ days}} \end{aligned}$$

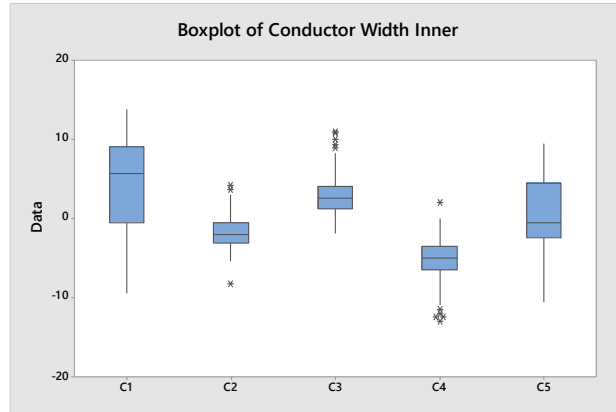
# MANUFACTURING VARIATION



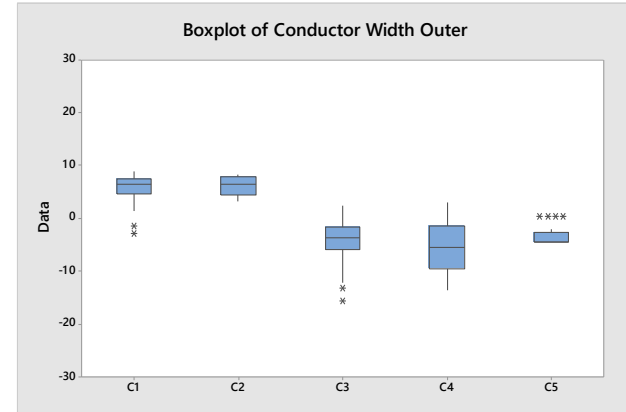
## Dielectric thickness



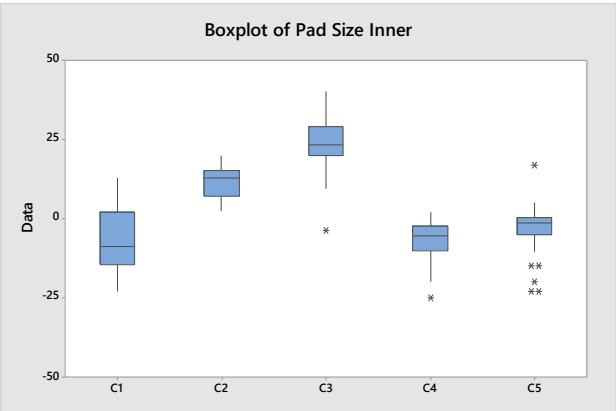
## Trace width inner



## Trace width outer



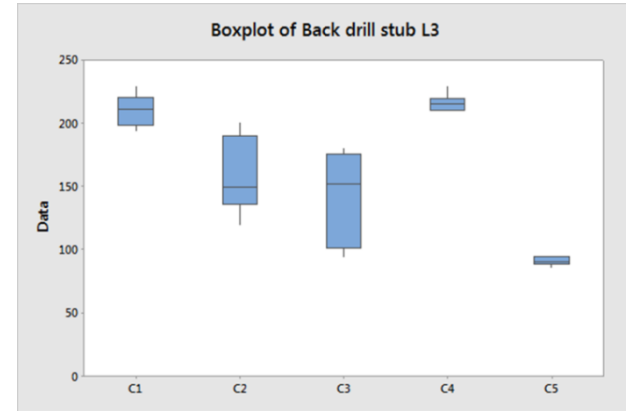
## Boxplot of Pad Size Inner



## Boxplot of Pad Size Outer



## Boxplot of Back drill stub L3



## Pad size inner

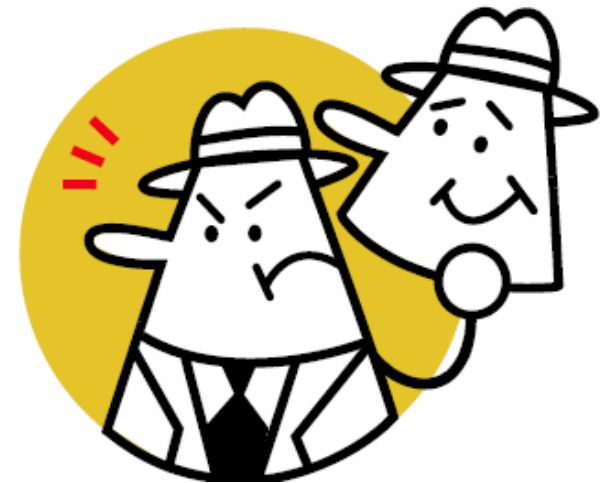
## Pad size outer

## Back drilling stub

# CHALLENGE



- › Complex system design
  - How to manage conflicting objectives?
  - Millions of system configurations to check
- › Analysis iteration time
  - How long will it take to get an answer?
  - If simulations take minutes and there are millions of settings to check it will take months to complete
- › Design decisions
  - How to manage multiple design decisions?
- › Manufacturing variation
  - How does this impact performance?
  - Can my design minimize the risk?



# THE DOE/RSM SOLUTION

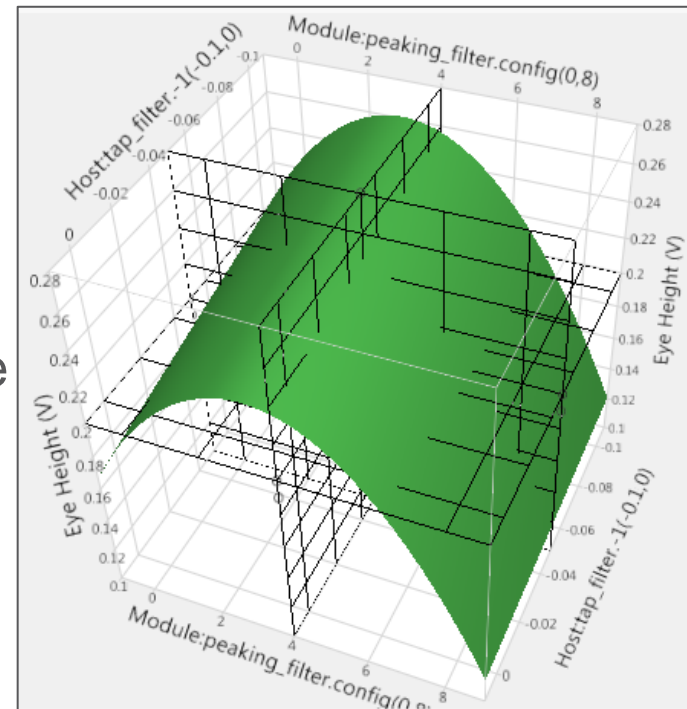


## > The Ideal:

- What if we had an equation where you put in the system conditions and out came system performance?

## > Approximating the Ideal:

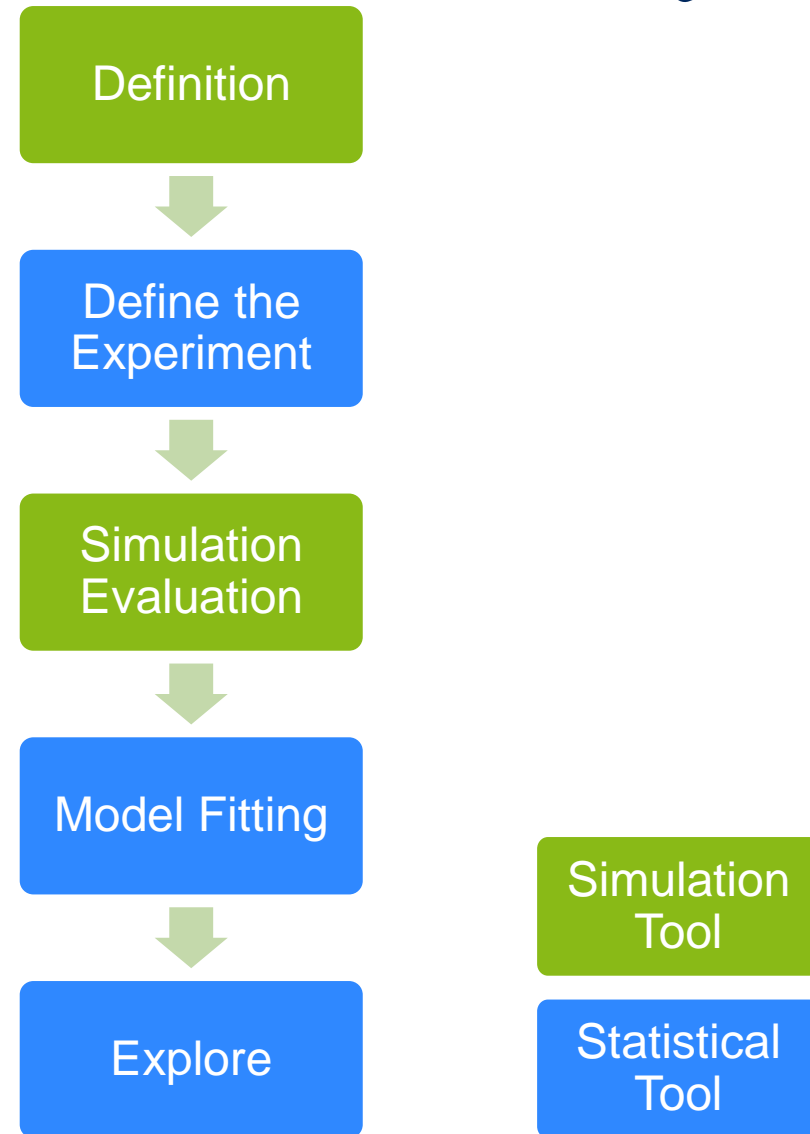
- Statistically sample the parameter space
  - > Design of Experiment (DOE)
- Use your knowledge of the system under analysis to apply an appropriate model to the data
  - > Response Surface Model (RSM)
- Validate model
- Utilize model to optimize and explore



# DESIGN OF EXPERIMENT PROCESS

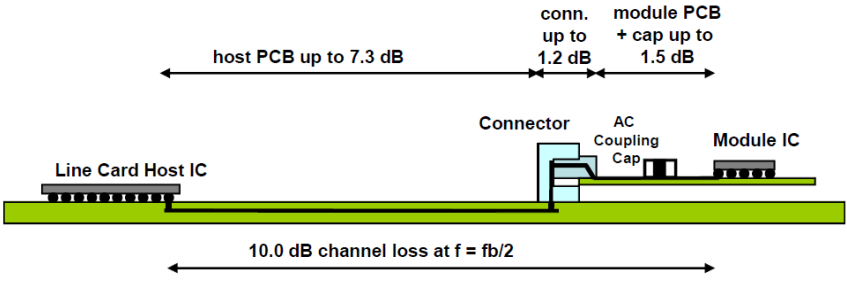


- › Definition
  - Link topology
  - Parameter space
- › Define the experiments
  - Define model
  - Create cases
- › Simulation and evaluation
  - Simulate all cases
  - Quantify performance of all cases
- › Model fitting
  - Response surface model
  - Least squares fit
- › Explore
  - Virtual “what if” analysis
  - Optimize
  - Defects per million (DPM) analysis

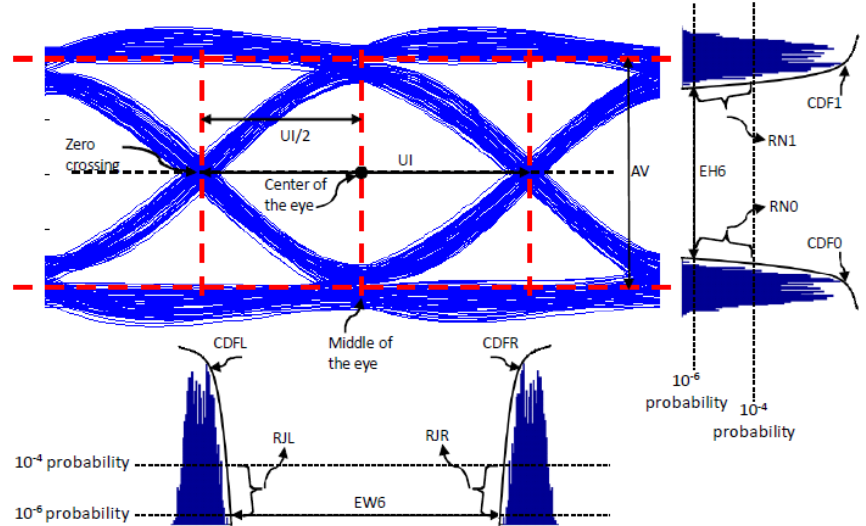




# CEI 28G-VSR



## CEI-28G-VSR Channel



## TP1a jitter and Eye Height parameters

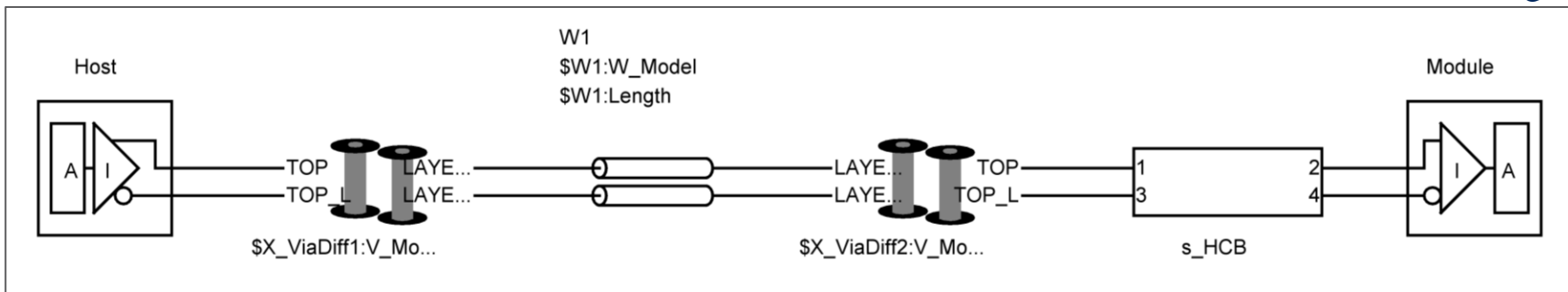
## Host-to-Module Electrical Specifications at TP1a (host output)

Parameter	Min.	Max.	Units	Conditions
Differential Voltage pk-pk	-	900	mV	
Common Mode Noise RMS	-	17.5	mV	See <a href="#">Section 13.3.5</a>
Differential Termination Resistance Mismatch	-	10	%	At 1 MHz See <a href="#">Section 13.3.6</a>
Differential Return Loss (SDD22)	-	See <a href="#">Equation 13-19</a>	dB	
Common Mode to Differential conversion and Differential to Common Mode Conversion (SDC22, SCD22)	-	See <a href="#">Equation 13-21</a>	dB	
Common Mode Return Loss (SCC22)	-	-2	dB	From 250 MHz to 30 GHz
Transition Time, 20 to 80%	10	-	ps	See <a href="#">Section 13.3.10</a>
Common Mode Voltage	-0.3	2.8	V	Referred to host ground
Eye Width at 10 <sup>-15</sup> probability (EW15) <sup>1</sup>	0.46	-	UI	See <a href="#">Section 13.3.11</a>
Eye Height at 10 <sup>-15</sup> probability (EH15) <sup>1</sup>	95	-	mV	See <a href="#">Section 13.3.11</a>

$$EW15 = 0.46UI$$

$$EH15 = 95mV$$

# DEFINITION



Item	Design Para.	Factor	Factor Type	Min	Typ	Max
1	EQ: FFE	Host:Tap_Filter.-1	Continuous	-0.1	-	0
2	EQ: FFE	Host:Tap_Filter.1	Continuous	-0.2	-	0
3	EQ: CTLE	Module:peaking_filter.config	Continuous	0	-	8
4	Channel length (inch)	W_Length	Continuous	2	-	6
5	Dielectric constant	Er	Continuous	3.85	-	3.95
6	Loss tangent	Loss_Tangent	Continuous	0.075	-	0.085
7	Conductor roughness (RMS)	Conductor_Roughness	Continuous	0.2	-	0.3
8	Dielectric height (mil)	Dielectric_Height_H1	Continuous	4.3	-	4.7
9	Differential separation (mil)	Differential_Separation	Continuous	5.9	-	6.7
10	Trace width (mil)	Trace_Width	Continuous	3.5	-	4.3
11	Trace thickness (mil)	Trace_Thickness	Continuous	0.57	-	0.67
12	Via type with diff. stub (mil)	X_ViaDiff1_V_MODEL	Categorical	Stub_2mil	Stub_6mil	Stub_10mil

# DEFINE THE EXPERIMENT



**Custom Design**

**Responses**

Response Name	Goal	Lower Limit	Upper Limit	Importance
Eye Height	Maximize	0.095	.	.
Eye Width	Maximize	16.5	.	.

**Factors**

Name	Role	Changes	Values
HOST:TAP_FILTER.-1	Continuous	Easy	-0.1
HOST:TAP_FILTER.1	Continuous	Easy	-0.2
MODULE:PEAKING_FILTER.CC	Continuous	Easy	0
SW1:CONDUCTOR_ROUGHNESS	Continuous	Easy	0.2
SW1:DIELECTRIC_HEIGHT_H1	Continuous	Easy	4.3
SW1:DIFFERENTIAL_SEPARATION	Continuous	Easy	5.9
SW1:ER	Continuous	Easy	3.6
SW1:LENGTH	Continuous	Easy	2
SW1:LOSS_TANGENT	Continuous	Easy	0.006
SW1:TRACE_THICKNESS	Continuous	Easy	0.57
SW1:TRACE_WIDTH	Continuous	Easy	3.5
SW1:DIFF1:V_MODEL	Categorical	Easy	Diff_Via_LongStub   Diff_Via_MiddleStub   Diff_Via_ShortStub

**Define Factor Constraints**

Name	Estimability
Intercept	Necessary
HOST:TAP_FILTER.-1	Necessary
HOST:TAP_FILTER.1	Necessary
MODULE:PEAKING_FILTER.CONFIG	Necessary
SW1:CONDUCTOR_ROUGHNESS	Necessary
SW1:DIELECTRIC_HEIGHT_H1	Necessary
SW1:DIFFERENTIAL_SEPARATION	Necessary
SW1:ER	Necessary

**Design Generation**

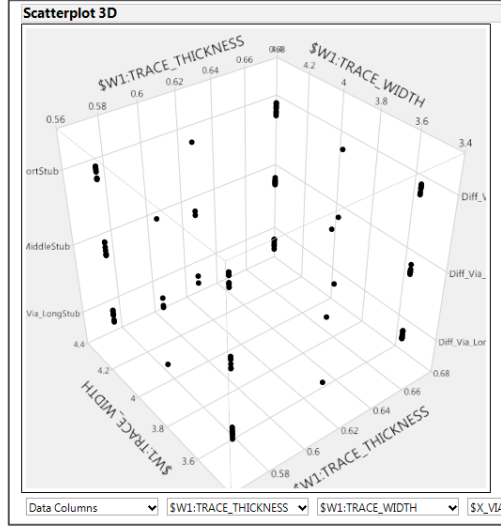
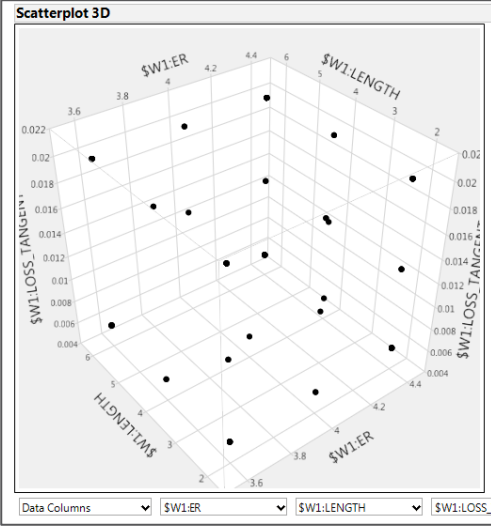
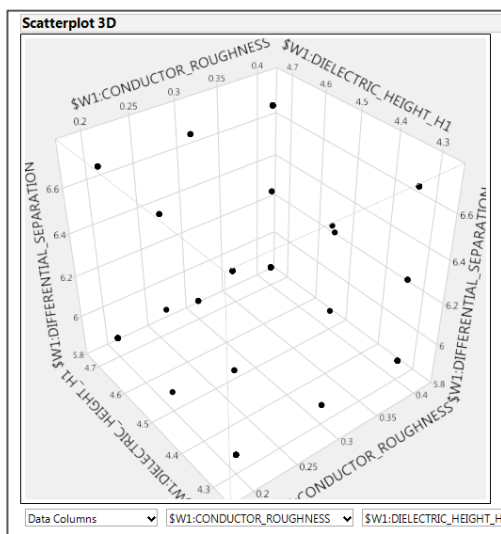
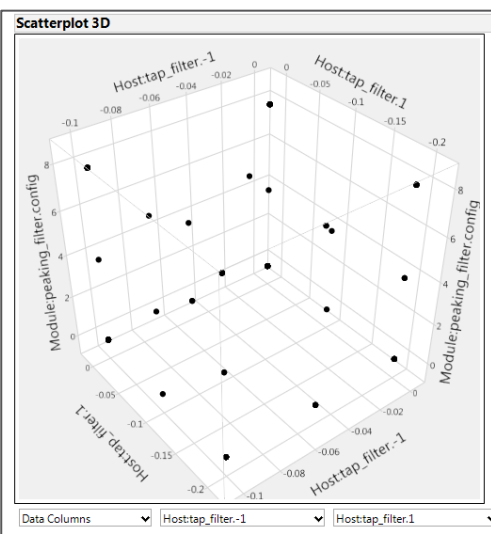
Group runs into random blocks of size: 2

Number of Center Points: 0  
Number of Replicate Runs: 0

**Number of Runs:**

- Minimum: 102
- Default: 108
- User Specified: 108

**Make Design**

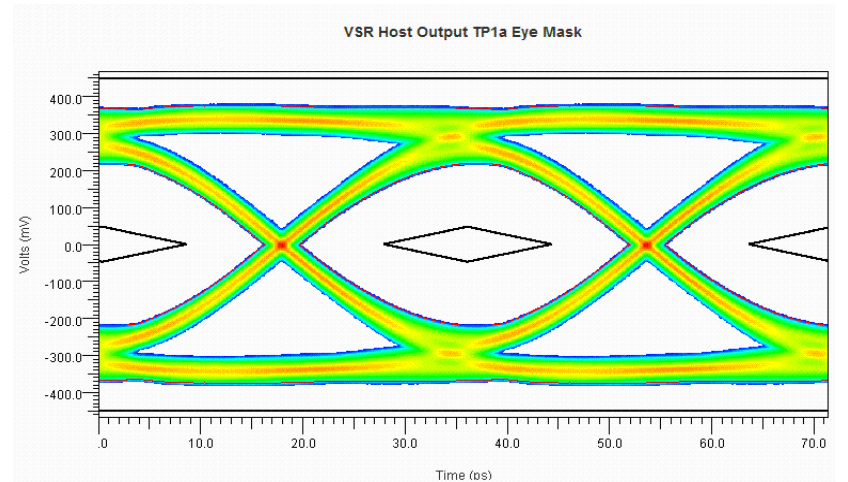
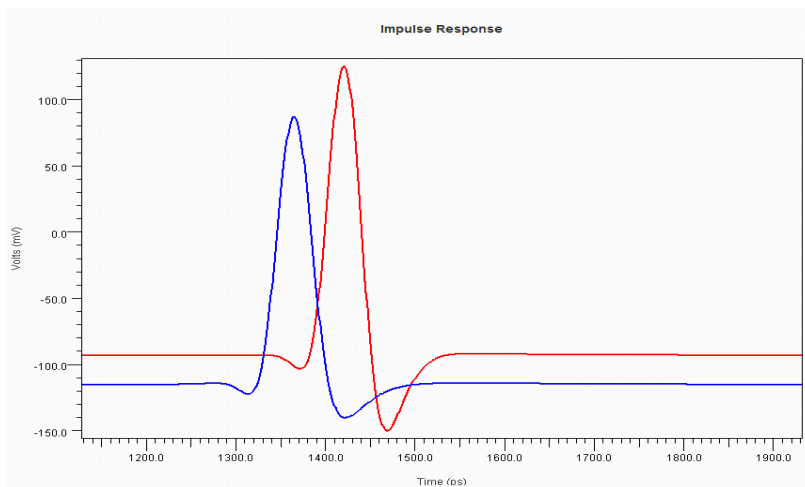
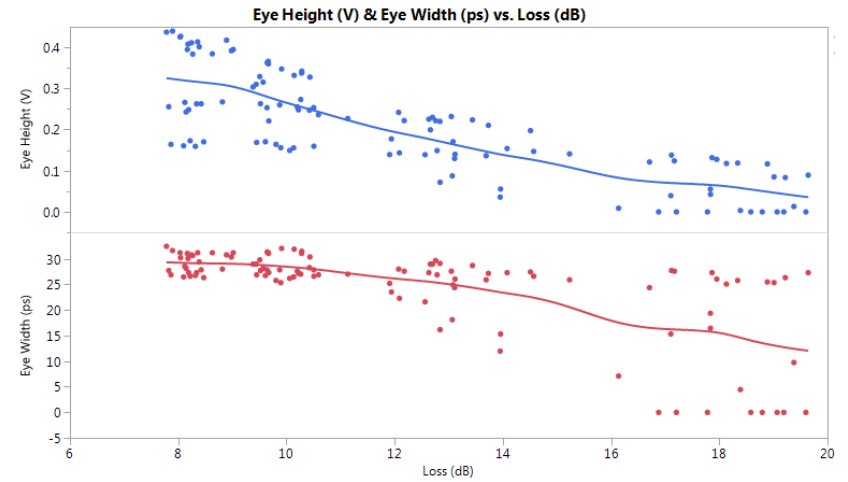
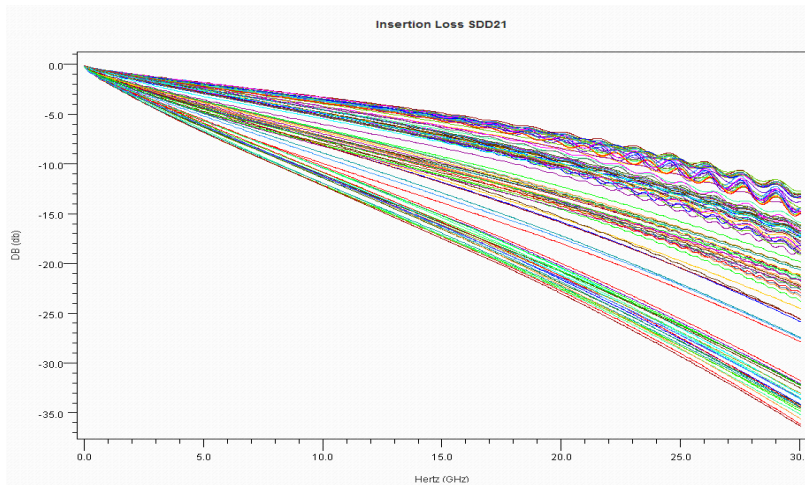


## 3D plots for parameter space

# SIMULATION EVALUATION



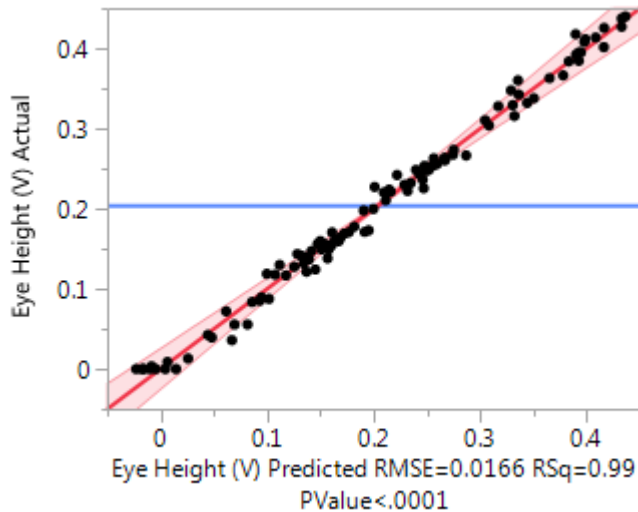
› Run the simulation and evaluate the results



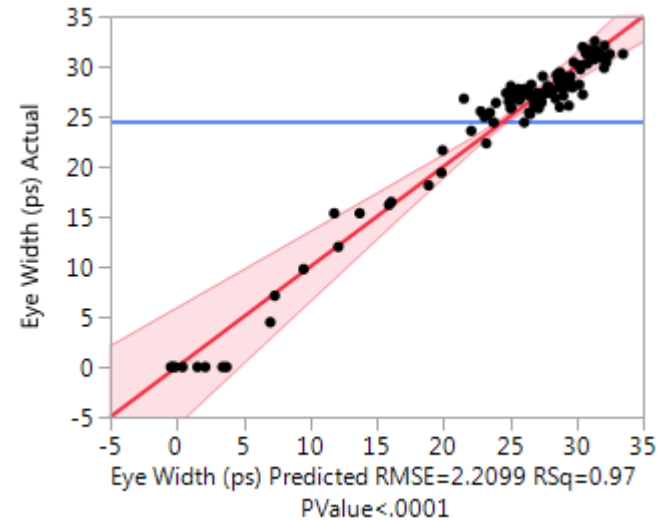
# MODEL FITTING



- › Model fitting is the process of finding the equation (or surface) which best matches the data points
- › Verify quality of fitting



Summary of Fit	
RSquare	0.991304
RSquare Adj	0.981756
Root Mean Square Error	0.016616
Mean of Response	0.204904
Observations (or Sum Wgts)	108

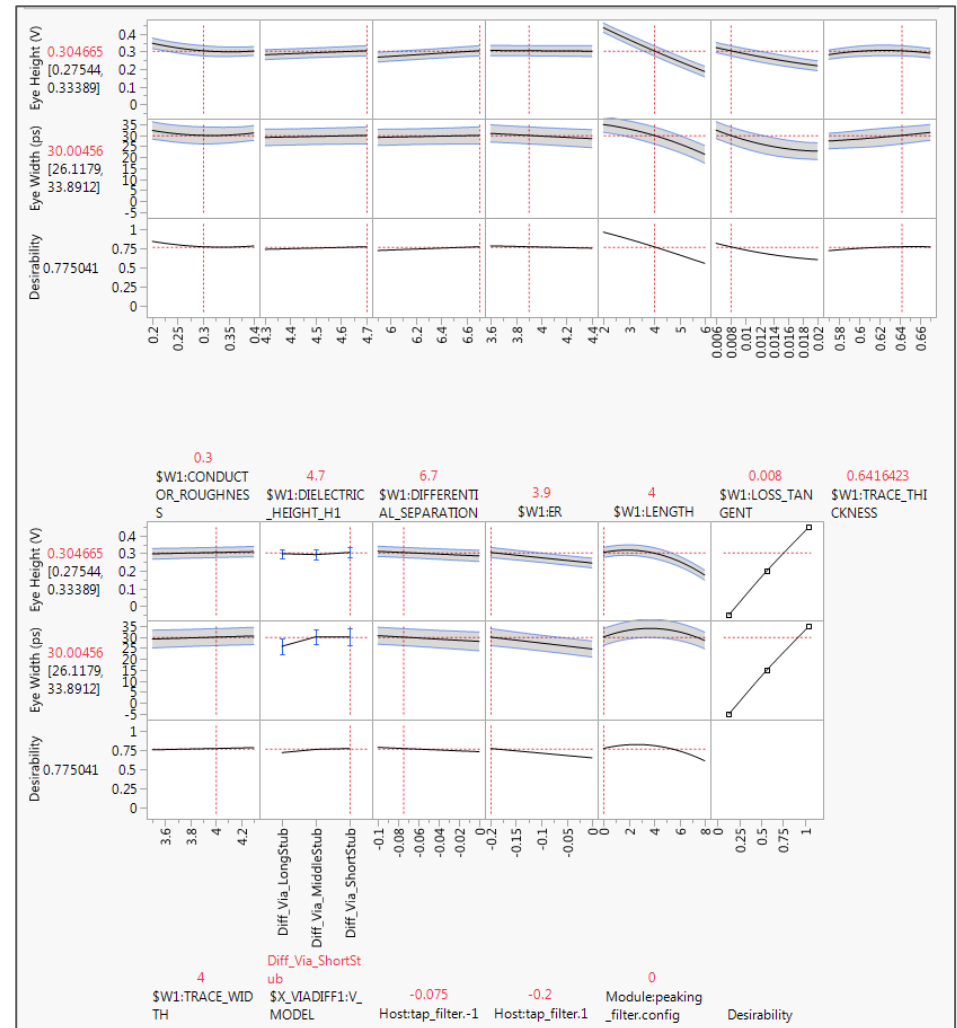


Summary of Fit	
RSquare	0.967963
RSquare Adj	0.932785
Root Mean Square Error	2.209945
Mean of Response	24.539
Observations (or Sum Wgts)	108

# EXPLORE: PREDICTION PROFILER



- > Confidence interval
  - Quality of model fitting
- > Slope
  - Influence
  - Importance
  - Sensitivity
- > Vertical red line
  - “What if ” analysis
  - Interactions
- > Desirability function/Optimization
  - Best case of design factors
  - Worst case of manufacturing factors
  - Robustness to minimize variation impact

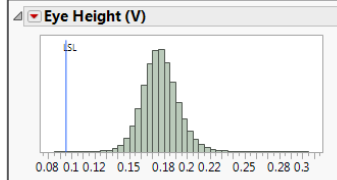


# EXPLORE: DPM ANALYSIS



- Use the Equation Simulator to evaluate the response equation at millions of conditions.
- Assign a sampling distribution to each factor, i.e. trace length, manufacturing variation etc.
- Millions of system configurations can be evaluated in seconds to obtain realistic predicted yield plots.

The Equation Simulator interface displays a grid of input factors with their respective distributions and values. Factors include SWL\_CONDUCT, SWL\_DELECTRIC, SWL\_DIFFERENT, SWL\_ER, SWL\_LENGTH, SWL\_LOSS\_TAN, SWL\_TRACE\_TH, SWL\_HEIGHT\_HI, SWL\_HEIGHT\_LO, SWL\_HEIGHT\_TH, SWL\_HEIGHT\_TH2, SWL\_HEIGHT\_TH3, SWL\_HEIGHT\_TH4, SWL\_HEIGHT\_TH5, SWL\_HEIGHT\_TH6, SWL\_HEIGHT\_TH7, SWL\_HEIGHT\_TH8, SWL\_HEIGHT\_TH9, SWL\_HEIGHT\_TH10, SWL\_HEIGHT\_TH11, SWL\_HEIGHT\_TH12, SWL\_HEIGHT\_TH13, SWL\_HEIGHT\_TH14, SWL\_HEIGHT\_TH15, SWL\_HEIGHT\_TH16, SWL\_HEIGHT\_TH17, SWL\_HEIGHT\_TH18, SWL\_HEIGHT\_TH19, SWL\_HEIGHT\_TH20, SWL\_HEIGHT\_TH21, SWL\_HEIGHT\_TH22, SWL\_HEIGHT\_TH23, SWL\_HEIGHT\_TH24, SWL\_HEIGHT\_TH25, SWL\_HEIGHT\_TH26, SWL\_HEIGHT\_TH27, SWL\_HEIGHT\_TH28, SWL\_HEIGHT\_TH29, SWL\_HEIGHT\_TH30, SWL\_HEIGHT\_TH31, SWL\_HEIGHT\_TH32, SWL\_HEIGHT\_TH33, SWL\_HEIGHT\_TH34, SWL\_HEIGHT\_TH35, SWL\_HEIGHT\_TH36, SWL\_HEIGHT\_TH37, SWL\_HEIGHT\_TH38, SWL\_HEIGHT\_TH39, SWL\_HEIGHT\_TH40, SWL\_HEIGHT\_TH41, SWL\_HEIGHT\_TH42, SWL\_HEIGHT\_TH43, SWL\_HEIGHT\_TH44, SWL\_HEIGHT\_TH45, SWL\_HEIGHT\_TH46, SWL\_HEIGHT\_TH47, SWL\_HEIGHT\_TH48, SWL\_HEIGHT\_TH49, SWL\_HEIGHT\_TH50. Each factor has a dropdown menu for its distribution (Normal, Uniform, etc.) and a numerical value. A 'Simulate' button is visible at the bottom right.



**Quantiles**

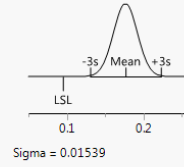
100.0%	maximum	0.303737325
99.5%		0.2243340845
97.5%		0.2092660094
90.0%		0.1959440746
75.0%	quartile	0.1859877813
50.0%	median	0.1760331586
25.0%	quartile	0.166580583
10.0%		0.1580772079
2.5%		0.1480528544
0.5%		0.1378933585
0.0%	minimum	0.0888225912

**Summary Statistics**

Mean	0.1766736
Std Dev	0.0153896
Std Err Mean	1.539e-5
Upper 95% Mean	0.1767037
Lower 95% Mean	0.1766434
N	1000000

**Capability Analysis**

Specification	Value	Portion	% Actual
Lower Spec Limit	0.095	Below LSL	0.0005
Spec Target		Above USL	
Upper Spec Limit		Total Outside	0.0005

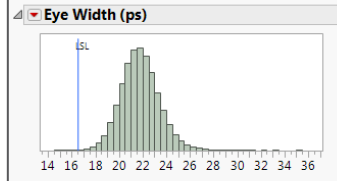


**Long Term Sigma**

Capability	Index	Lower CI	Upper CI
CP	1.769	1.766	1.772
CPK			
CPM			
CPL	1.769	1.766	1.772
CPU			

Portion	Percent	PPM	Quality
Below LSL	0.0000	0.0557	6.807
Above USL			
Total Outside	0.0000	0.0557	6.807



**Quantiles**

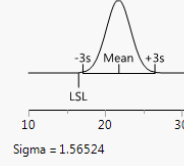
100.0%	maximum	35.456087649
99.5%		26.336860295
97.5%		25.015524568
90.0%		23.760532769
75.0%	quartile	22.746889325
50.0%	median	21.697181775
25.0%	quartile	20.696139496
10.0%		19.811354145
2.5%		18.843565212
0.5%		17.993301776
0.0%	minimum	14.651097415

**Summary Statistics**

Mean	21.755885
Std Dev	1.5652401
Std Err Mean	0.0015652
Upper 95% Mean	21.758953
Lower 95% Mean	21.752817
N	1000000

**Capability Analysis**

Specification	Value	Portion	% Actual
Lower Spec Limit	16.5	Below LSL	0.0115
Spec Target		Above USL	
Upper Spec Limit		Total Outside	0.0115



**Long Term Sigma**

Capability	Index	Lower CI	Upper CI
CP	1.119	1.118	1.121
CPK			
CPM			
CPL	1.119	1.118	1.121
CPU			

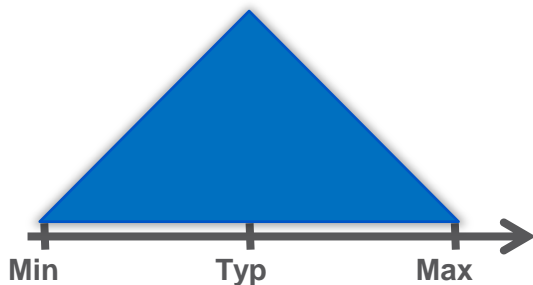
Portion	Percent	PPM	Quality
Below LSL	0.0393	392.7163	4.858
Above USL			
Total Outside	0.0393	392.7163	4.858



# QUESTION FOR IBIS-AMI



- › IBIS-AMI currently and traditionally uses a *Typ*, *Min*, *Max* parameter definition.
- › This is based on a *Best/Worst* case scenario analysis. E.g. 100% confidence.
- › Best/Worst case analysis has served us well during the years and still does in some cases, however more and more cases will not reach design closure using Best/Worst case analysis.
- › When it does not reach design closure how will we know how many of our produced units will fail ???

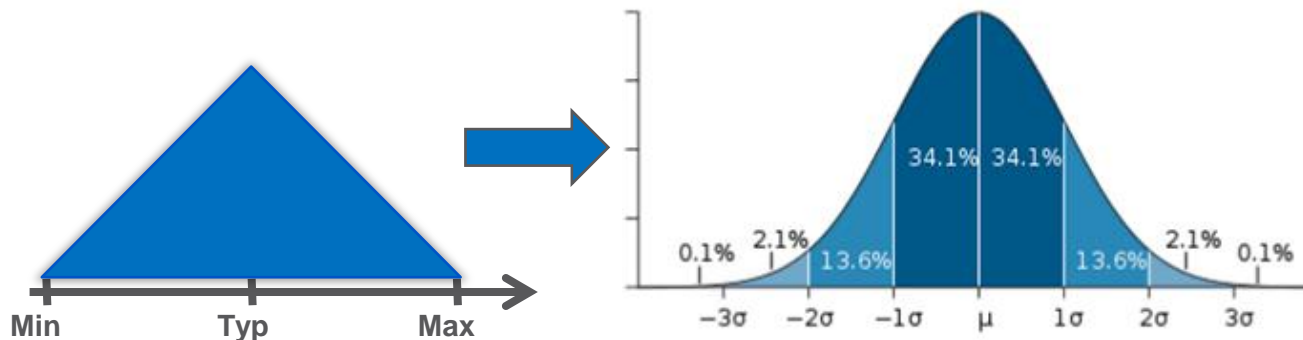




# SUGGESTION FOR IBIS-AMI



- › If we add an option to IBIS-AMI to support distribution data for parameters as an average/mean and a variation/sigma.
- › If we feel we can not assume a standard distribution we could even add support for other distributions.
- › These parameters could be used in DOE analysis scenarios and could help us predict confidence intervals for our products as well as DPM (Defect Per million) predictions.



# CONCLUSION



- › Our design work is moving beyond *Best Case, Worst Case* analysis.
- › We need to start working on an infrastructure both in modeling and tool support for statistical analysis.
- › We need to ensure that we can get the correct information from IC and PCB vendors on parameter distributions.
- › SI/PI statistical analysis is the next step to ensure our product quality.



**ERICSSON**