A PRACTICAL METHODOLOGY FOR SERDES DESIGN

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AGENDA

› Challenges in Traditional Simulation
› The DOE/RSM Solution
› CEI 28G-VSR IF Design with DOE
› Question and Suggestion for IBIS-AMI
SERDES & CHANNEL

› Transceiver Equalization
› Via impedance
› Trace impedance
› Trace loss
› Connector characteristics
MISSION IMPOSSIBLE

Equalization settings
- FFE
  - Precursor – 10 taps
  - Postcursor – 10 taps
- CTLE
  - Off; Fixed; Adapt
- DFE
  - Off; Fixed; Adapt

Via impedance
- 3 corners (TC/WC/BC)

Trace impedance
- 3 corners (TC/WC/BC)

Connector characteristics
- 3 corners (TC/WC/BC)

Trace loss
- 3 corners (TC/WC/BC)

Assuming 10min for each simulation case:
- Running bits: $1 \times 10^6$
- Sampling per bit: 64
- Block size: 1024

Total time consumption of simulation:
$10 \times 10 \times 10 \times 3^6$

= 729000 minutes

= 506.25 days
MANUFACTURING VARIATION

Dielectric thickness

Trace width inner

Trace width outer

Pad size inner

Pad size outer

Back drilling stub
Complex system design
- How to manage conflicting objectives?
- Millions of system configurations to check

Analysis iteration time
- How long will it take to get an answer?
- If simulations take minutes and there are millions of setting to check it will take months to complete

Design decisions
- How to manage multiple design decisions?

Manufacturing variation
- How does this impact performance?
- Can my design minimize the risk?
The Ideal:
- What if we had an equation where you put in the system conditions and out came system performance?

Approximating the Ideal:
- Statistically sample the parameter space
  - Design of Experiment (DOE)
- Use your knowledge of the system under analysis to apply an appropriate model to the data
  - Response Surface Model (RSM)
- Validate model
- Utilize model to optimize and explore
• Definition
  – Link topology
  – Parameter space
• Define the experiments
  – Define model
  – Create cases
• Simulation and evaluation
  – Simulate all cases
  – Quantify performance of all cases
• Model fitting
  – Response surface model
  – Least squares fit
• Explore
  – Virtual “what if” analysis
  – Optimize
  – Defects per million (DPM) analysis
CEI 28G-VSR

Host-to-Module Electrical Specifications at TP1a (host output)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential Voltage pk-pk</td>
<td>-</td>
<td>900</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Common Mode Noise RMS</td>
<td>-</td>
<td>17.5</td>
<td>mV</td>
<td>See Section 13.3.5</td>
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<tr>
<td>Differential Termination Resistance Mismatch</td>
<td>-</td>
<td>10</td>
<td>%</td>
<td>At 1 MHz See Section 13.3.6</td>
</tr>
<tr>
<td>Differential Return Loss (SDD22)</td>
<td>-</td>
<td>See Equation 13-19</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Common Mode to Differential conversion and Differential to Common Mode Conversion (SDD22)</td>
<td>-</td>
<td>See Equation 13-21</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Common Mode Return Loss (SCC22)</td>
<td>-</td>
<td>-2</td>
<td>dB</td>
<td>From 250 MHz to 30 GHz</td>
</tr>
<tr>
<td>Transition Time, 20 to 80%</td>
<td>10</td>
<td>-</td>
<td>ps</td>
<td>See Section 13.3.10</td>
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<tr>
<td>Common Mode Voltage</td>
<td>-0.3</td>
<td>2.8</td>
<td>V</td>
<td>Referred to host ground</td>
</tr>
</tbody>
</table>

**Eye Width at $10^{-15}$ probability (EW15)**

EW15 = 0.46UI

**Eye Height at $10^{-15}$ probability (EH15)**

EH15 = 95mV

TP1a jitter and Eye Height parameters
### Definition

<table>
<thead>
<tr>
<th>Item</th>
<th>Design Para.</th>
<th>Factor</th>
<th>Factor Type</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
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<tbody>
<tr>
<td>1</td>
<td>EQ: FFE</td>
<td>Host:Tap_Filter.-1</td>
<td>Continuous</td>
<td>-0.1</td>
<td>-</td>
<td>0</td>
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<tr>
<td>2</td>
<td>EQ: FFE</td>
<td>Host:Tap_Filter.1</td>
<td>Continuous</td>
<td>-0.2</td>
<td>-</td>
<td>0</td>
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<tr>
<td>3</td>
<td>EQ: CTLE</td>
<td>Module:peaking_filter.config</td>
<td>Continuous</td>
<td>0</td>
<td>-</td>
<td>8</td>
</tr>
<tr>
<td>4</td>
<td>Channel length (inch)</td>
<td>W_Length</td>
<td>Continuous</td>
<td>2</td>
<td>-</td>
<td>6</td>
</tr>
<tr>
<td>5</td>
<td>Dielectric constant</td>
<td>Er</td>
<td>Continuous</td>
<td>3.85</td>
<td>-</td>
<td>3.95</td>
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<tr>
<td>6</td>
<td>Loss tangent</td>
<td>Loss_Tangent</td>
<td>Continuous</td>
<td>0.075</td>
<td>-</td>
<td>0.085</td>
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<tr>
<td>7</td>
<td>Conductor roughness (RMS)</td>
<td>Conductor_Roughness</td>
<td>Continuous</td>
<td>0.2</td>
<td>-</td>
<td>0.3</td>
</tr>
<tr>
<td>8</td>
<td>Dielectric height (mil)</td>
<td>Dielectric_Height_H1</td>
<td>Continuous</td>
<td>4.3</td>
<td>-</td>
<td>4.7</td>
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<tr>
<td>9</td>
<td>Differential separation (mil)</td>
<td>Differential_Separation</td>
<td>Continuous</td>
<td>5.9</td>
<td>-</td>
<td>6.7</td>
</tr>
<tr>
<td>10</td>
<td>Trace width (mil)</td>
<td>Trace_Width</td>
<td>Continuous</td>
<td>3.5</td>
<td>-</td>
<td>4.3</td>
</tr>
<tr>
<td>11</td>
<td>Trace thickness (mil)</td>
<td>Trace_Thickness</td>
<td>Continuous</td>
<td>0.57</td>
<td>-</td>
<td>0.67</td>
</tr>
<tr>
<td>12</td>
<td>Via type with diff. stub (mil)</td>
<td>X_ViaDiff1_V_MODEL</td>
<td>Categorical</td>
<td></td>
<td>Stub_2mil</td>
<td>Stub_6mil</td>
</tr>
</tbody>
</table>
DEFINE THE EXPERIMENT

3D plots for parameter space
Run the simulation and evaluate the results
MODEL FITTING

› Model fitting is the process of finding the equation (or surface) which best matches the data points

› Verify quality of fitting
EXPLORE: PREDICTION PROFILER

- Confidence interval
  - Quality of model fitting
- Slope
  - Influence
  - Importance
  - Sensitivity
- Vertical red line
  - “What if ” analysis
  - Interactions
- Desirability function/Optimization
  - Best case of design factors
  - Worst case of manufacturing factors
  - Robustness to minimize variation impact
› Use the Equation Simulator to evaluate the response equation at millions of conditions.

› Assign a sampling distribution to each factor, i.e. trace length, manufacturing variation etc.

› Millions of system configurations can be evaluated in seconds to obtain realistic predicted yield plots.
IBIS-AMI currently and traditionally uses a Typ, Min, Max parameter definition.

This is based on a Best/Worst case scenario analysis. E.g. 100% confidence.

Best/Worst case analysis has served us well during the years and still does in some cases, however more and more cases will not reach design closure using Best/Worst case analysis.

When it does not reach design closure how will we know how many of our produced units will fail ????
If we add an option to IBIS-AMI to support distribution data for parameters as an average/mean and a variation/sigma.

If we feel we can not assume a standard distribution we could even add support for other distributions.

These parameters could be used in DOE analysis scenarios and could help us predict confidence intervals for our products as well as DPM (Defect Per million) predictions.
CONCLUSION

› Our design work is moving beyond *Best Case, Worst Case* analysis.

› We need to start working on an infrastructure both in modeling and tool support for statistical analysis.

› We need to ensure that we can get the correct information from IC and PCB vendors on parameter distributions.

› SI/PI statistical analysis is the next step to ensure our product quality.