

WELCOME FROM MIKE LABONTE, IBIS OPEN FORUM

Ladies and Gentlemen,

As chair of the IBIS Open Forum it is my pleasure to welcome you to the 2018 Asian IBIS Summit in Taipei and to thank you for your presentations and participation. We are grateful to our sponsors Cadence Design Systems, KairosTech Innovation (SPISim), and Synopsys for making this event possible.

Since 1993 IBIS has provided the digital electronics industry with specifications to make signal, timing, and power integrity analyses much easier and faster. With the introduction of IBIS-AMI in 2008, the IBIS community generated new energy for high speed electronic design. IBIS is now known by engineers worldwide and is a required technology for many applications.

Support for IBIS in Asia has been strong, and the IBIS Open Forum looks forward to continued innovation and contributions from technology companies in Asia.

Thank you!



Mike LaBonte
SiSoft
Chair, IBIS Open Forum

WELCOME FROM MIKE LABONTE, IBIS OPEN FORUM

女士們先生們，

作為 IBIS 開放論壇的主席，我很高興地歡迎您參加 2018 年在台北舉辦的亞洲 IBIS 峰會，感謝您的介紹和參與。我們非常感謝我們的讚助商 Cadence Design Systems, KairosTech Innovation (SPISim) 和 Synopsys，以使這一事件成為可能。

自 1993 年以來，IBIS 為數字電子行業提供了使信號，時序和電源完整性分析更容易和更快速的規範。隨著 IBIS-AMI 在 2008 年的推出，IBIS 社區為高速電子設計創造了新的能量。IBIS 現在已被世界各地的工程師所了解，是許多應用所需的技術。

IBIS 在亞洲的支持一直很強，IBIS 開放論壇期待著亞洲技術公司的不斷創新和貢獻。

谢谢!



Mike LaBonte (迈克 拉邦地)

SiSoft 公司

主席， IBIS 开放论坛

AGENDA AND ORDER OF THE PRESENTATIONS

(The actual agenda might be modified)

I B I S S U M M I T M E E T I N G A G E N D A

9:00	SIGN IN - Vendor Tables Open at 8:30	
9:30	WELCOME - Mike LaBonte (Chair, IBIS Open Forum) (SiSoft, USA)	
9:45	IBIS Update Mike LaBonte (SiSoft, USA)	5
10:05	A Practical Methodology for SerDes Design Amy Zhang*, Guohua Wang*, David Zhang*, Zilwan Mahmood**, Anders Ekholm** (Ericsson, *PRC, *Sweden) [Presented by Amy Zhang (Ericson, PRC)]	11
10:35	BREAK (Refreshments and Vendor Tables)	
10:55	Characterizing and Modeling of a Clamped Non-Linear CTE/AGC Skipper Liang (Cadence Design Systems, ROC)	21
11:50	FREE BUFFET LUNCH (Hosted by Sponsors) - Vendor Tables	
13:20	Model Correlation for IBIS-AMI Wenyan Xie*, Guohua Wang*, David Zhang*, Anders Ekholm** (Ericsson, *PRC, **Sweden) [Presented by Anders Ekholm (Ericsson, Sweden)]	37
14:10	BREAK (Refreshments and Vendor Tables)	
14:30	Study of DDR Asymmetric Rt/Ft in Existing IBIS-AMI Flow Wei-hsing Huang#, Wei-kai Shih## (SPISim, #USA, ##Japan) [Presented by Wei-hsing Huang (SPISim, USA)]	52
15:00	DISCUSSION	
15:20	CONCLUDING ITEMS	
15:30	END OF IBIS SUMMIT MEETING	

IBIS Update



<http://www.ibis.org/>

Mike LaBonte
SiSoft
Chair, IBIS Open Forum
2018 Asian IBIS Summit
Taipei, ROC
November 16, 2018

IBIS Update

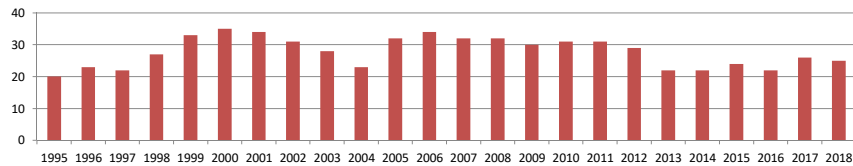
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Organization

25 IBIS Members



Number of Members by Year



IBIS Update

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Organization

IBIS Officers 2018-2019

- Chair: *Mike LaBonte, SiSoft*
Vice-Chair: *Lance Wang, IO Methodology Inc.*
Secretary: *Randy Wolff, Micron Technology*
Treasurer: *Bob Ross, Teraspeed Labs*
Librarian: *Anders Ekholm, Ericsson*
Postmaster: *Curtis Clark, ANSYS*
Webmaster: *Mike LaBonte, SiSoft*



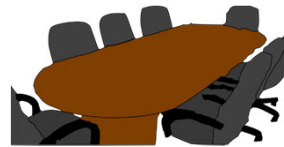
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Organization

IBIS Meetings

- Weekly teleconferences
 - Quality Task Group (Tuesdays)
 - Advanced Technology Modeling Task Group (Tuesdays)
 - Interconnect Task Group (Wednesdays)
 - Editorial Task Group (some Fridays)
- IBIS Open Forum teleconference every 3 weeks
 - 480 meetings so far
- IBIS Summit meetings: DesignCon, IEEE SPI, EDICON USA, EPEPS, Shanghai, Taipei, Tokyo



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Organization

SAE ITC

- SAE Industry Technologies Consortia is the parent organization of the IBIS Open Forum
- IBIS is assisted by SAE employees José Godoy, Phyllis Gross, Dorothy Lloyd
- SAE ITC provides financial, legal, and other services
- <http://www.sae-itc.org/>



IBIS Update

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Organization

Task Groups

- **Interconnect Task Group**
 - Chair: Michael Mirmak
 - http://ibis.org/interconn_wip/
 - Develop on-die/package/module/connector interconnect modeling BIRDS
- **Advanced Technology Modeling Task Group**
 - Chair: Arpad Muranyi
 - http://ibis.org/atm_wip/
 - Develop most other technical BIRDS
- **Quality Task Group**
 - Chair: Mike LaBonte
 - http://ibis.org/quality_wip/
 - Oversee IBISCHK parser testing and development
- **Editorial Task Group**
 - Chair: Michael Mirmak
 - http://ibis.org/editorial_wip/
 - Produce IBIS Specification documents

BIRD = Buffer Issue Resolution Document

IBIS Update

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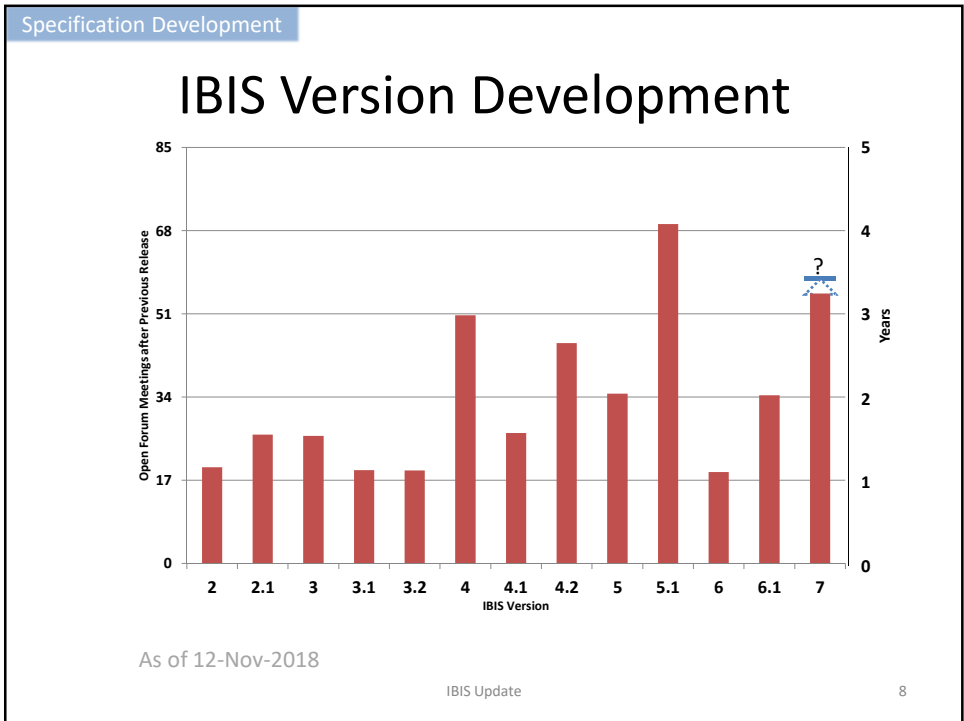
Specification Development

IBIS Milestones

<p><u>I/O Buffer Information Specification</u></p> <ul style="list-style-type: none"> • 1993-1994 IBIS 1.0-2.1: <ul style="list-style-type: none"> - Behavioral buffer model (fast simulation) - Component pin map (easy EDA import) • 1997-1999 IBIS 3.0-3.2: <ul style="list-style-type: none"> - Package models - Electrical Board Description (EBD) - Dynamic buffers • 2002-2006 IBIS 4.0-4.2: <ul style="list-style-type: none"> - Receiver models - AMS languages • 2007-2012 IBIS 5.0-5.1: <ul style="list-style-type: none"> - IBIS-AMI SerDes models - Power aware • 2013-2015 IBIS 6.0-6.1: <ul style="list-style-type: none"> - PAM4 multi-level signaling - Power delivery package models • 2019? IBIS 7.0 	<p><u>Other Work</u></p> <ul style="list-style-type: none"> • 1995: ANSI/EIA-656 <ul style="list-style-type: none"> - IBIS 2.1 • 1999: ANSI/EIA-656-A <ul style="list-style-type: none"> - IBIS 3.2 • 2001: IEC 62014-1 <ul style="list-style-type: none"> - IBIS 3.2 • 2003: ICM 1.0 <ul style="list-style-type: none"> - Interconnect Model Specification • 2006: ANSI/EIA-656-B <ul style="list-style-type: none"> - IBIS 4.2 • 2009: Touchstone 2.0* • 2011: IBIS-ISS 1.0 <ul style="list-style-type: none"> - Interconnect SPICE Subcircuit specification
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Current development

IBIS Update 7



Specification Development

Possible IBIS 7.0 Timeline

Meeting Date	Milestone
4/21/2017	Vote to establish 7.0 as the next IBIS version passes.
...	<i>BIRD review and acceptance (30 meetings)</i>
7/20/2018	7.0 BIRD set accepted.
...	<i>Editorial task group drafts IBIS 7.0</i>
12/21/2018	Editorial announces IBIS 7.0 ready. Review period begins
1/11/2019	
2/8/2019	Vote to ratify 7.0 scheduled for next meeting
3/1/2019	IBIS 7.0 ratified



Specification Development

BIRDs Included in IBIS 7.0

BIRD	Title
147.6	Back-channel Support
165	Parameter Passing Improvements for [External Circuit]s
179	New IBIS-AMI Reserved Parameter Special_Param_Names
180	Require Unique Pin Names in [Pin]
182	POWER and GND [Pin] signal_name as [Pin Mapping] bus_label
183	[Model Data] Matrix Subparameter Terminology Correction
184.2	Model_name and Signal_name Restriction for POWER and GND Pins
185.2	Section 3 Reserved Word Guideline Update
186.4	File Naming Rules
187.3	Format and Usage Out Clarifications
188.1	Expanded Rx Noise Support for AMI
189.6	Interconnect Modeling Using IBIS-ISS and Touchstone
191.2	Clarifying Locations for Si_location and Timing_location
192.1	Clarification of List Default Rules
193	Figure 29 corrections
194	Revised AMI Ts4file Analog Buffer Models
196.1	Prohibit Periods at the End of File Names

Specification Development

BIRDS Excluded from IBIS 7.0

BIRD	Title
166.2	Resolving problems with Redriver Init Flow
181.1	I-V Table Clarifications
190	Clarification for Redriver Flow
195.1	Enabling [Rgnd] and [Rpower] Keywords for Input Models

Green = Approved BIRD

IBIS Update

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[Thank You]



IBIS Open Forum:
Web: <http://www.ibis.org>
Email: ibis-info@freelists.org

We welcome participation
by all IBIS model makers,
EDA tool vendors, IBIS model
users, and interested parties.

IBIS Update

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A PRACTICAL METHODOLOGY FOR SERDES DESIGN

Asian IBIS Summit, Taipei, Taiwan, November 16, 2018

Authors:

Amy Zhang, Guohua Wang, David Zhang, Zilwan Mahmud,
Anders Ekholm

AGENDA



- › Challenges in Traditional Simulation
- › The DOE/RSM Solution
- › CEI 28G-VSR IF Design with DOE
- › Question and Suggestion for IBIS-AMI

SERDES & CHANNEL

The diagram illustrates the SerDes & Channel components and their interactions. It shows a Transmitter on the left and a Receiver on the right, connected by a Channel. The components are arranged in a vertical stack on both sides: Transmitter, BGA Via, Trans Line, Conn PTH, and Connector. The Channel is represented by a horizontal line connecting the Conn PTHs of the Transmitter and Receiver. The Channel is further divided into Conn PTH, Stripline, and Conn PTH. The SerDes is shown as a dashed line connecting the Transmitter and Receiver. The Channel is shown as a solid line connecting the Conn PTHs of the Transmitter and Receiver.

- > Transceiver Equalization
- > Via impedance
- > Trace impedance
- > Trace loss
- > Connector characteristics

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MISSION IMPOSSIBLE

- > Equalization settings
 - FFE
 - > Precursor – 10 taps
 - > Postcursor – 10 taps
 - CTLE
 - > Off; Fixed; Adapt
 - DFE
 - > Off; Fixed; Adapt
- > Via impedance
 - 3 corners (TC/WC/BC)
- > Trace impedance
 - 3 corners (TC/WC/BC)
- > Connector characteristics
 - 3 corners (TC/WC/BC)
- > Trace loss
 - 3 corners (TC/WC/BC)

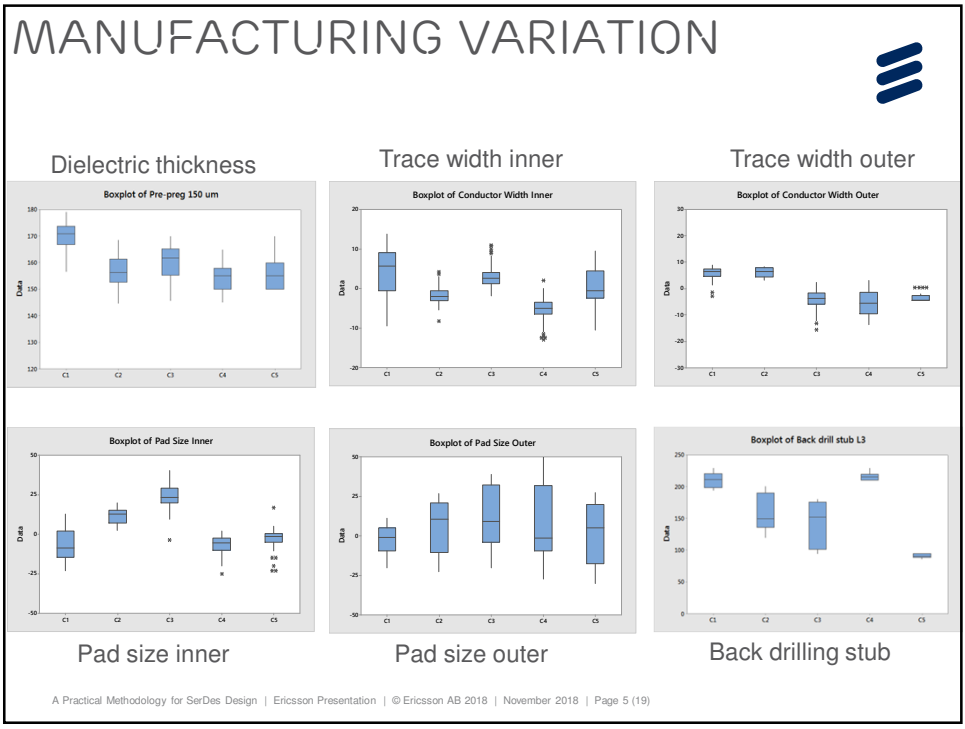
Assuming 10min for each simulation case:

- Running bits: $1 \cdot 10^6$
- Sampling per bit: 64
- Block size: 1024

Total time consumption of simulation:

$$10 \cdot 10^6 \cdot 64 \cdot 1024 = 729000 \text{ minutes} = 506.25 \text{ days}$$

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CHALLENGE

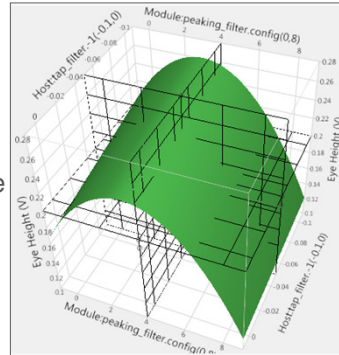
- › Complex system design
 - How to manage conflicting objectives?
 - Millions of system configurations to check
- › Analysis iteration time
 - How long will it take to get an answer?
 - If simulations take minutes and there are millions of setting to check it will take months to complete
- › Design decisions
 - How to manage multiple design decisions?
- › Manufacturing variation
 - How does this impact performance?
 - Can my design minimize the risk?

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THE DOE/RSM SOLUTION



- › The Ideal:
 - What if we had an equation where you put in the system conditions and out came system performance?
- › Approximating the Ideal:
 - Statistically sample the parameter space
 - › Design of Experiment (DOE)
 - Use your knowledge of the system under analysis to apply an appropriate model to the data
 - › Response Surface Model (RSM)
 - Validate model
 - Utilize model to optimize and explore

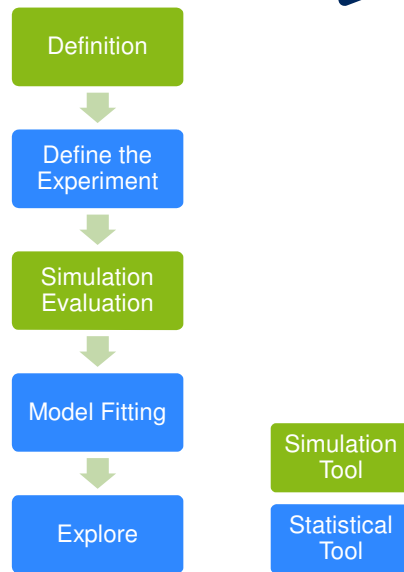


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DESIGN OF EXPERIMENT PROCESS



- › Definition
 - Link topology
 - Parameter space
- › Define the experiments
 - Define model
 - Create cases
- › Simulation and evaluation
 - Simulate all cases
 - Quantify performance of all cases
- › Model fitting
 - Response surface model
 - Least squares fit
- › Explore
 - Virtual “what if” analysis
 - Optimize
 - Defects per million (DPM) analysis



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CEI 28G-VSR

host PCB up to 7.3 dB
conn. up to 1.2 dB
module PCB + cap up to 1.5 dB

10.0 dB channel loss at $f = fb/2$

CEI-28G-VSR Channel

Zero
Center of the eye
 $UI/2$
 UI
 AV
 $EH6$
 $RN1$
 RNO
 $CDR1$
 $CDR0$
 10^{-4} probability
 10^{-4} probability
Middle of the eye
 $CDR1$
 RK
 RJR
 $EW6$
 10^{-4} probability

TP1a jitter and Eye Height parameters

Parameter	Min.	Max.	Units	Conditions
Differential Voltage pk-pk	-	900	mV	
Common Mode Noise RMS	-	17.5	mV	See Section 13.3.5
Differential Termination Resistance Mismatch	-	10	%	At 1 MHz See Section 13.3.6
Differential Return Loss (SDD22)	-	See Equation 13-19	dB	
Common Mode to Differential conversion and Differential to Common Mode Conversion (SDC22, SCD22)	-	See Equation 13-21	dB	
Common Mode Return Loss (SCC22)	-	-2	dB	From 250 MHz to 30 GHz
Transition Time, 20 to 80%	10	-	ps	See Section 13.3.10
Common Mode Voltage	-0.3	2.8	V	Referred to host ground
Eye Width at 10^{-15} probability ($EW15$) ¹	0.46	-	UI	See Section 13.3.11
Eye Height at 10^{-15} probability ($EH15$) ¹	95	-	mV	See Section 13.3.11

$EW15 = 0.46UI$
 $EH15 = 95mV$


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DEFINITION

Item	Design Para.	Factor	Factor Type	Min	Typ	Max
1	EQ: FFE	Host:Tap_Filter,-1	Continuous	-0.1	-	0
2	EQ: FFE	Host:Tap_Filter,1	Continuous	-0.2	-	0
3	EQ: CTLE	Module:peaking_filter.config	Continuous	0	-	8
4	Channel length (inch)	W_Length	Continuous	2	-	6
5	Dielectric constant	Er	Continuous	3.85	-	3.95
6	Loss tangent	Loss_Tangent	Continuous	0.075	-	0.085
7	Conductor roughness (RMS)	Conductor_Roughness	Continuous	0.2	-	0.3
8	Dielectric height (mil)	Dielectric_Height_H1	Continuous	4.3	-	4.7
9	Differential separation (mil)	Differential_Separation	Continuous	5.9	-	6.7
10	Trace width (mil)	Trace_Width	Continuous	3.5	-	4.3
11	Trace thickness (mil)	Trace_Thickness	Continuous	0.57	-	0.67
12	Via type with diff. stub (mil)	X_ViaDiff1_V_MODEL	Categorical	Stub_2mil	Stub_6mil	Stub_10mil

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DEFINE THE EXPERIMENT



Custom Design

Responses

Response Name	Goal	Lower Limit	Upper Limit	Importance
Eye Height	Maximize	0.075		
Eye Width	Maximize	16.5		

Factors

Name	Role	Changes	Values
HOST_TAP_FILTER_1	Continuous	Easy	0,1
HOST_TAP_FILTER_4	Continuous	Easy	0,2
MODULE_PEAKING_FILTER_CC	Continuous	Easy	0,1
SWI_CONDUCTOR_ROUGHNESS	Continuous	Easy	0,2
SWI_DELECTRIC_HEIGHT_H1	Continuous	Easy	6,3
SWI_DIFFERENTIAL_SEPARATION	Continuous	Easy	5,9
SWI_IBR	Continuous	Easy	1,6
SWI_LENGTH	Continuous	Easy	2
SWI_LOSS_TANGENT	Continuous	Easy	0,008
SWI_TRACE_THICKNESS	Continuous	Easy	0,57
SI_3DREFLECT_MODEL	Categorical	Easy	1,5

Define Factor Constraints

Name	Estimability
Intercept	Necessary
HOST_TAP_FILTER_1	Necessary
HOST_TAP_FILTER_4	Necessary
MODULE_PEAKING_FILTER_CONTR	Necessary
SWI_CONDUCTOR_ROUGHNESS	Necessary
SWI_DELECTRIC_HEIGHT_H1	Necessary
SWI_DIFFERENTIAL_SEPARATION	Necessary
SWI_IBR	Necessary

Design Generation

Number of Center Points: 0
 Number of Replicate Runs: 0

Number of Runs: Minimum 102
 Default 108
 User Specified 108


Make Design

Scatterplot 3D

3D plots for parameter space

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SIMULATION EVALUATION



▶ Run the simulation and evaluate the results

Insertion Loss SDD21

Eye Height (V) & Eye Width (ps) vs. Loss (dB)

Impulse Response

VSR Host Output TPIa Eye Mask

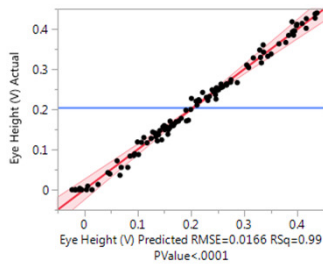
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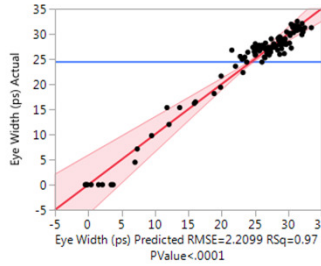
MODEL FITTING



- › Model fitting is the process of finding the equation (or surface) which best matches the data points
- › Verify quality of fitting



Summary of Fit	
RSquare	0.991304
RSquare Adj	0.981756
Root Mean Square Error	0.016616
Mean of Response	0.204904
Observations (or Sum Wgts)	108



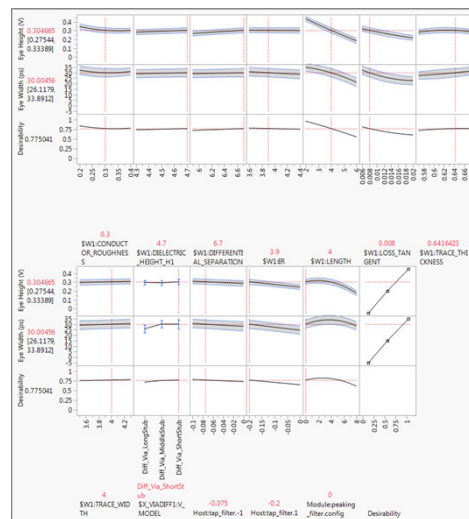
Summary of Fit	
RSquare	0.967963
RSquare Adj	0.932785
Root Mean Square Error	2.209945
Mean of Response	24.539
Observations (or Sum Wgts)	108

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EXPLORE: PREDICTION PROFILER



- › Confidence interval
 - Quality of model fitting
- › Slope
 - Influence
 - Importance
 - Sensitivity
- › Vertical red line
 - “What if ” analysis
 - Interactions
- › Desirability function/Optimization
 - Best case of design factors
 - Worst case of manufacturing factors
 - Robustness to minimize variation impact

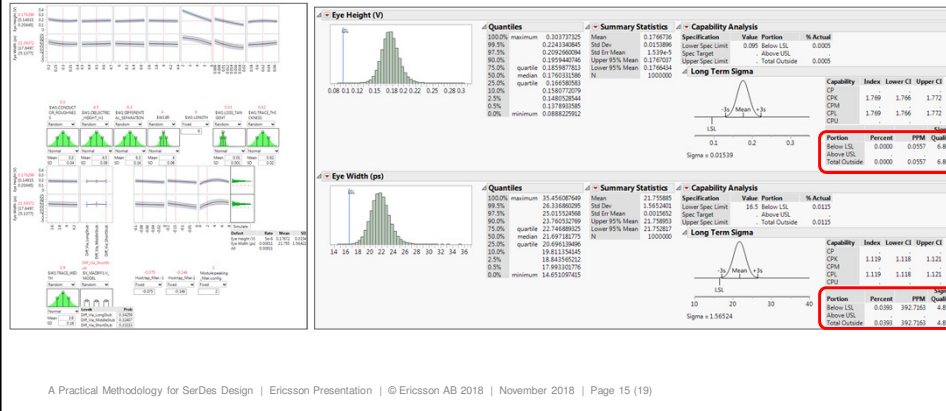


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EXPLORE: DPM ANALYSIS



- › Use the Equation Simulator to evaluate the response equation at millions of conditions.
- › Assign a sampling distribution to each factor, i.e. trace length, manufacturing variation etc.
- › Millions of system configurations can be evaluated in seconds to obtain realistic predicted yield plots.

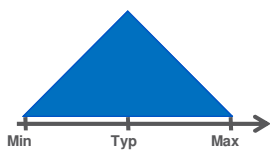


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QUESTION FOR IBIS-AMI



- › IBIS-AMI currently and traditionally uses a *Typ, Min, Max* parameter definition.
- › This is based on a *Best/Worst* case scenario analysis. E.g. 100% confidence.
- › Best/Worst case analysis has served us well during the years and still does in some cases, however more and more cases will not reach design closure using Best/Worst case analysis.
- › When it does not reach design closure how will we know how many of our produced units will fail ???

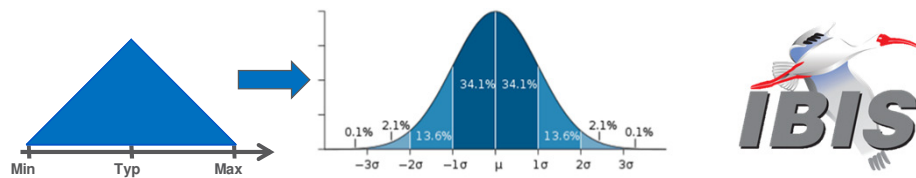


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SUGGESTION FOR IBIS-AMI



- › If we add an option to IBIS-AMI to support distribution data for parameters as an average/mean and a variation/sigma.
- › If we feel we can not assume a standard distribution we could even add support for other distributions.
- › These parameters could be used in DOE analysis scenarios and could help us predict confidence intervals for our products as well as DPM (Defect Per million) predictions.



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CONCLUSION



- › Our design work is moving beyond *Best Case, Worst Case* analysis.
- › We need to start working on an infrastructure both in modeling and tool support for statistical analysis.
- › We need to ensure that we can get the correct information from IC and PCB vendors on parameter distributions.
- › SI/PI statistical analysis is the next step to ensure our product quality.


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Characterizing and Modeling of a Clamped Non-Linear CTE/AGC

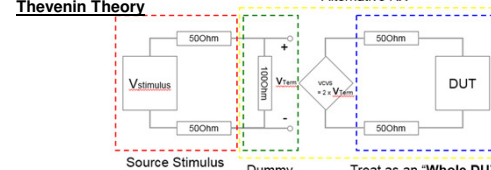
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Characterize a Linear CTE or CTE+AGC

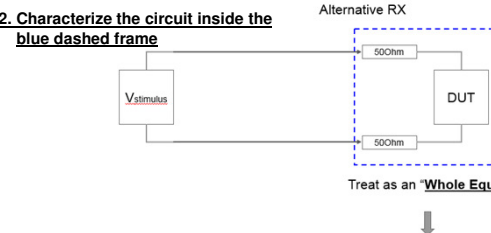
In 2017 IBIS Summit, we deliver an easy but accurate methodology of characterizing a linear CTE (or even CTE+AGC, as long as the linearity is met.)

1. Derive an equivalent circuit using Thevenin Theory




Source Stimulus Dummy Buffer Alternative RX Treat as an "Whole DUT"

2. Characterize the circuit inside the blue dashed frame




Alternative RX Treat as an "Whole Equalizer"

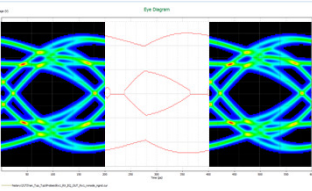



Characterizing and Modeling of a Linear CTE

Skipper Liang
Asian IBIS Summit
Taipei, ROC
November 15, 2017



3. Correlate the result of AMI in Channel analysis with the one of netlist in Transient analysis.

2 © 2018 Cadence Design Systems, Inc. All rights reserved.

Scale of Characterization Stimulus

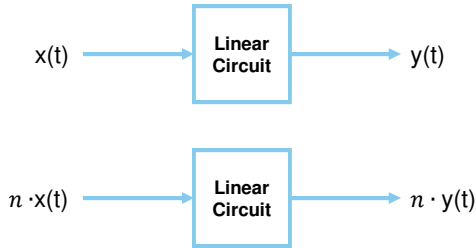
Scale of Characterization Stimulus is important as it will be a normalization factor in an AMI model.

```

RO_HyperCore
{
  CTE
  {
    cstim
    {
      ( file D:\Case_CDNS_20160616_IBIS_AMI\Modelize_RX\CTLE_TRAN_0_5
      ( scale 0
      ( input 0.57
    }
  }
  module_of 0
  case_file cstim.txt
  rx_file_rx cte_td_out.txt
  adapt_cte_file cte_out.txt
}
}

24 .subckt TX_500UT pos neg pwr in ngnd
25 R1
26 E1 pos ngnd volt *0.47+0.57*(in,ngnd)
27 E2 neg ngnd volt *1.04-0.57*(in,ngnd)
28 .
29 .ends
    
```

However, for a "Linear" RX EQ, we didn't pay too much focus on how much the scale of characterization stimulus should be because for a "Linear" RX EQ, it should meet the following:

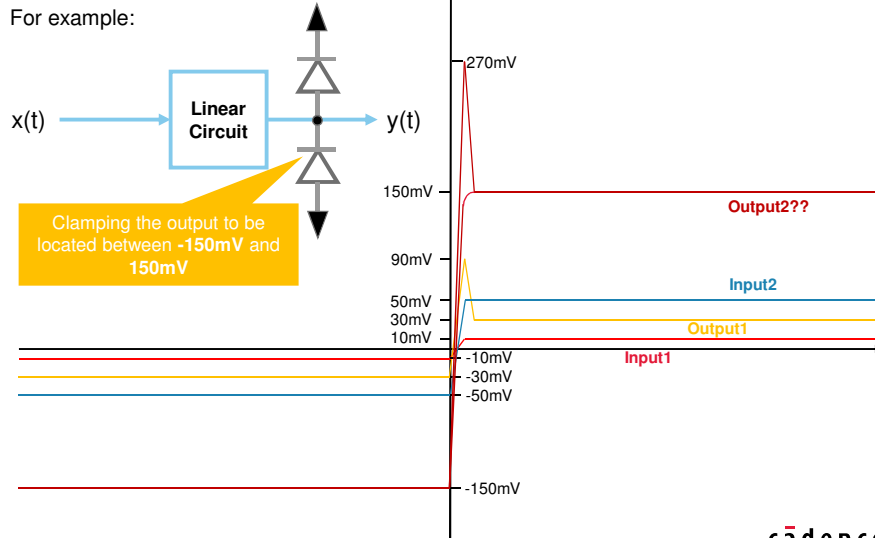


It means no matter how much the scale of characterization stimulus is, as long as the normalization factor is correct, the model will work close to the real circuit.

Characterize of Non-linear CTE/AGC

But most circuits are not linear as there are clamping diodes to protect the circuit.

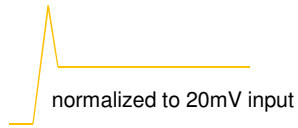
For example:



Characterize of Non-linear CTE/AGC

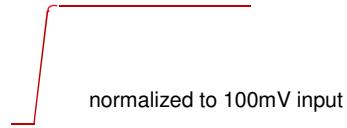
How to characterize such a non-linear circuit?

Approach 1.

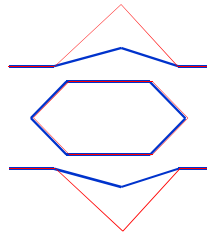


or

Approach 2.



If we characterize such a non-linear circuit with **Approach 1.**



Blue: Generated by SPICE netlist under Transient Analysis
Red: Generated by AMI model under Channel Analysis

"Small Signal" to characterize the CTLE:

1. You can capture the HF response of the CTLE
2. But you will miss the DC behavior of the stable logic high and low

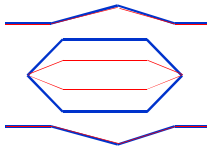
5

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Characterize of Non-linear CTE/AGC

If we characterize such a non-linear circuit with **Approach 2.**



Blue: Generated by SPICE netlist under Transient Analysis
Red: Generated by AMI model under Channel Analysis

"Large Signal" to characterize the CTLE:

1. You can capture the correct DC behavior of the stable logic high and low of the CTLE
2. But you will miss the HF response

For **Approach 1**, since the characterization can successfully capture the circuit's response at High Frequency range but miss the DC behavior, the model's simulation result can be well-correlated with SPICE transient analysis' result while a **Lossy Channel** is applied, which decays much more at High Frequency range.

For **Approach 2**, since the characterization can successfully capture the circuit's DC behavior but miss the response at High Frequency range, the model's simulation result can be well-correlated with SPICE transient analysis' result while a **Lossless Channel** is applied, which decays much less at High Frequency range.

How to have a model which can **accommodate all kinds of channels**?

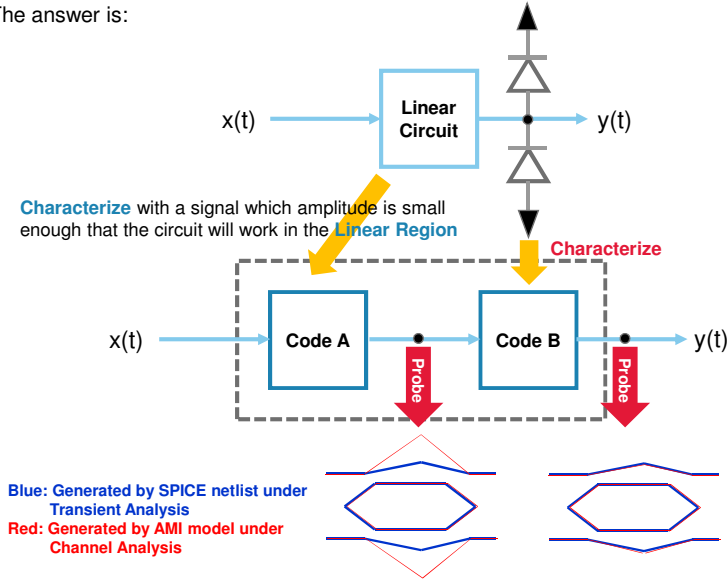
6

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Characterize of Non-linear CTE/AGC

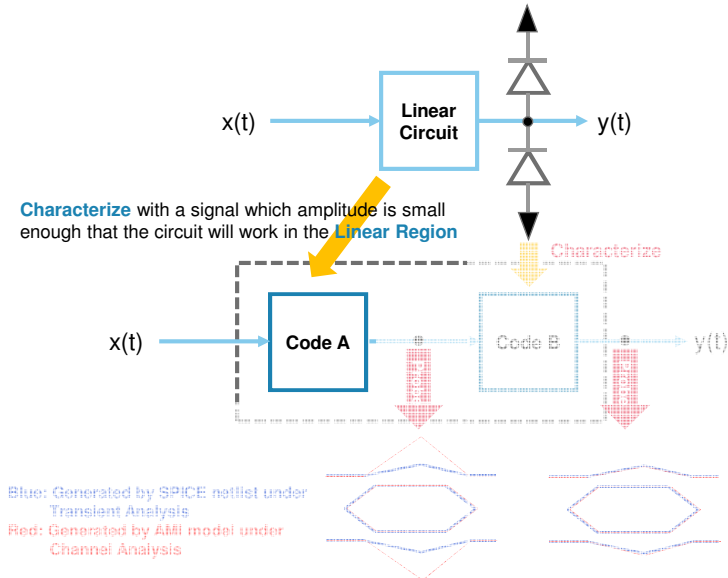
The answer is:



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Characterize the Linear Part - Linear Region



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Linear Region

How to know if I'm characterizing in the Linear Region?

1. Choose a input voltage level V_{in_lv1}

For example: Apply $V_{in_lv1} = 50mV$ to the circuit at the right.

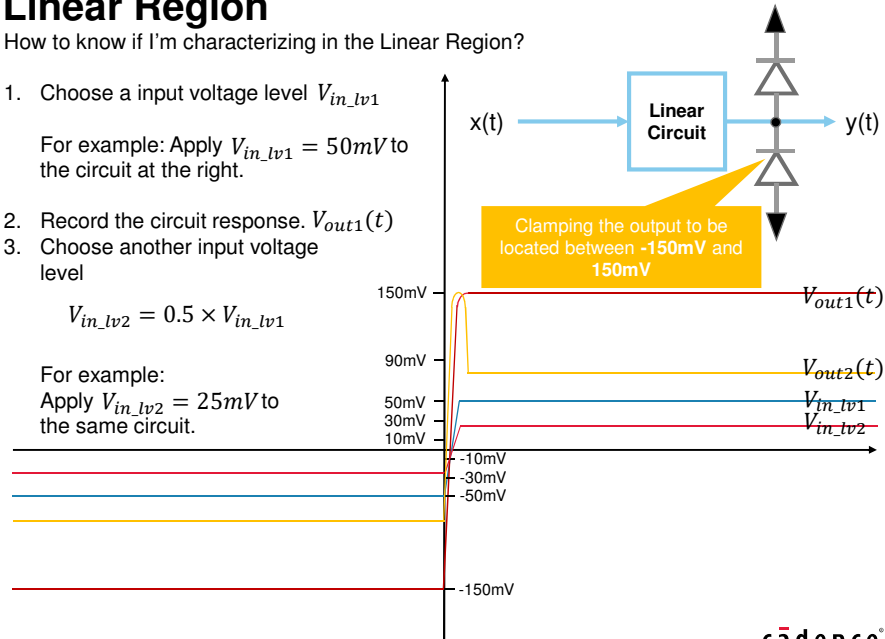
2. Record the circuit response. $V_{out1}(t)$

3. Choose another input voltage level

$$V_{in_lv2} = 0.5 \times V_{in_lv1}$$

For example:

Apply $V_{in_lv2} = 25mV$ to the same circuit.



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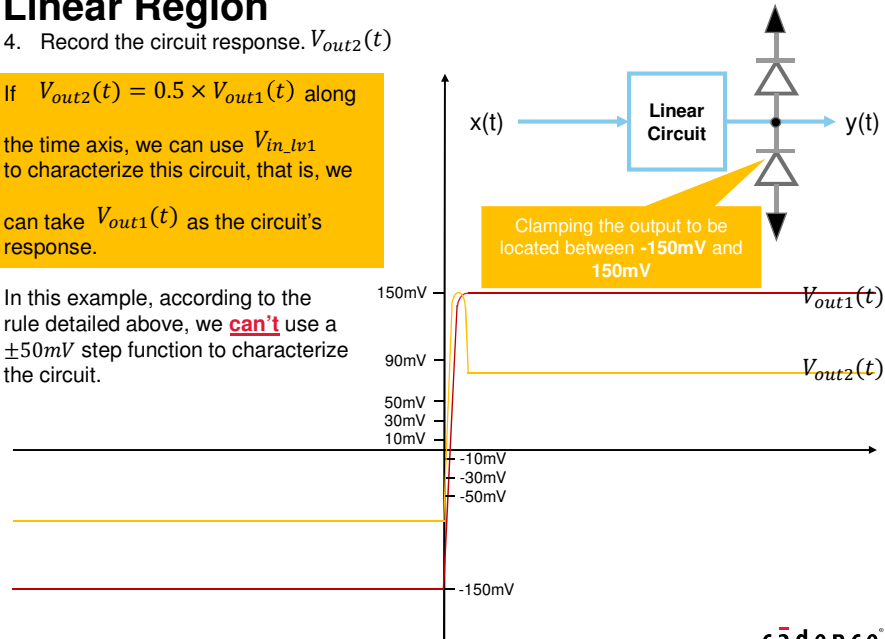
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Linear Region

4. Record the circuit response. $V_{out2}(t)$

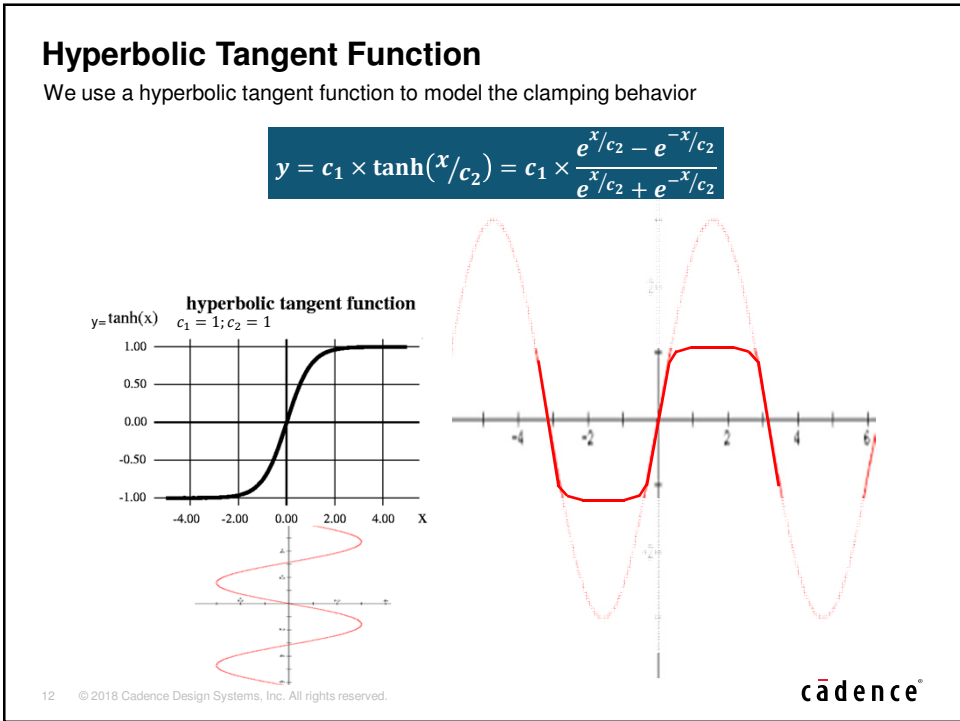
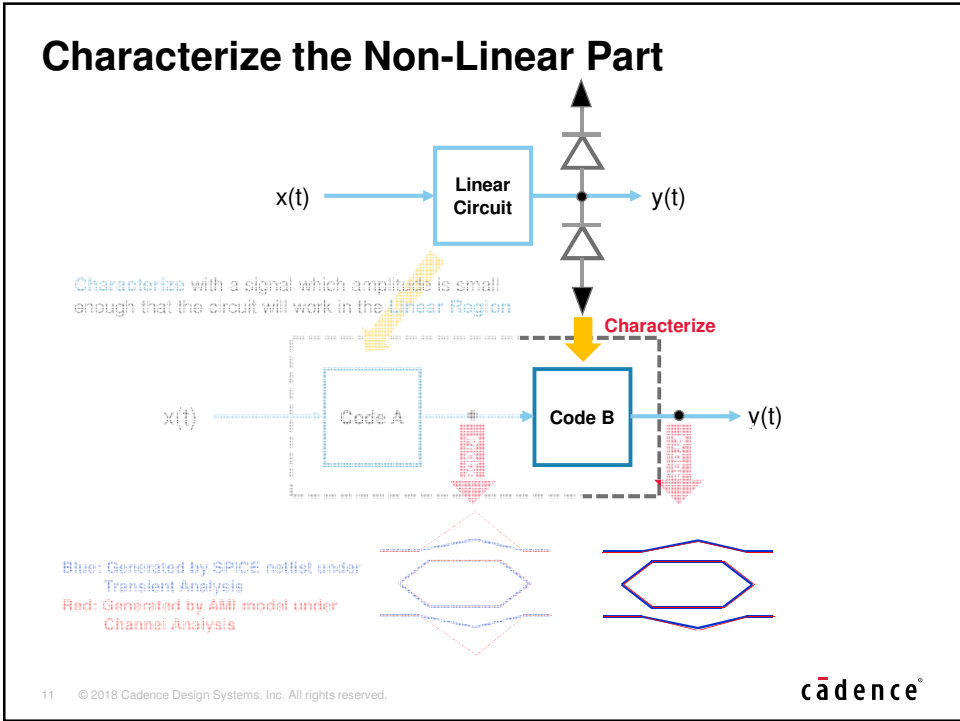
If $V_{out2}(t) = 0.5 \times V_{out1}(t)$ along the time axis, we can use V_{in_lv1} to characterize this circuit, that is, we can take $V_{out1}(t)$ as the circuit's response.

In this example, according to the rule detailed above, we **can't** use a $\pm 50mV$ step function to characterize the circuit.



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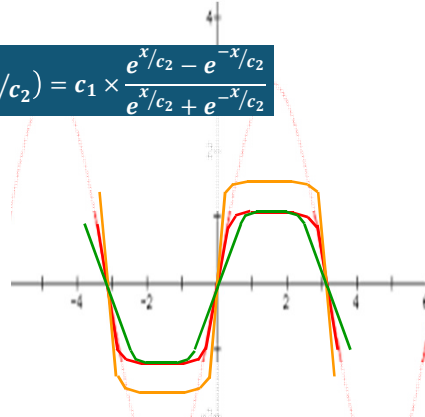
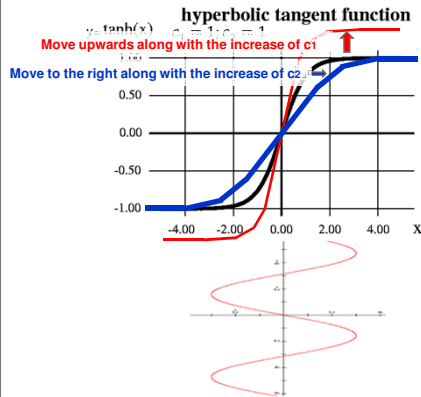
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Hyperbolic Tangent Function

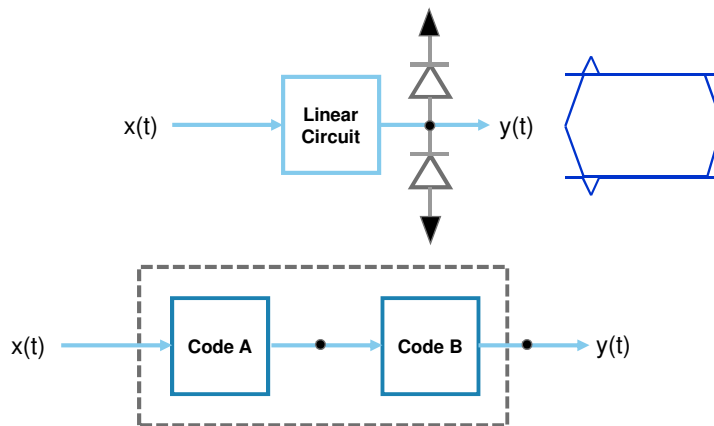
By adjusting parameters C1 and C2, we can customize the Hyperbolic Tangent function as close to the circuit's behavior as we want.

$$y = c_1 \times \tanh\left(\frac{x}{c_2}\right) = c_1 \times \frac{e^{x/c_2} - e^{-x/c_2}}{e^{x/c_2} + e^{-x/c_2}}$$



Increase of c1: Rising/Falling slew rate increase, upper/lower increase
 Increase of c2: Rising/Falling slew rate decrease, upper/lower remains the same
 The ratio C1/C2 represent the slope of the linear region of the hyperbolic tangent function and could be deemed as the amplification scale.

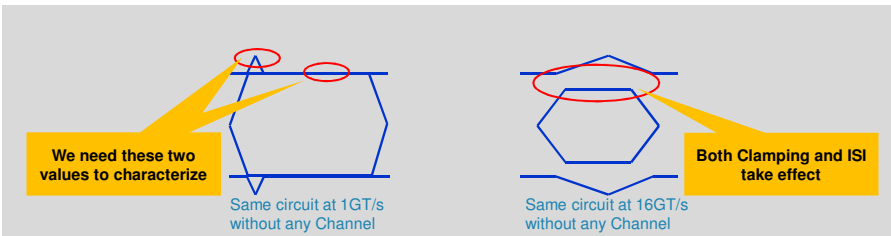
Characterization of $y=C1*\tanh(x/C2)$ – C1 and C2



Step 1: Transient analysis over the transistor netlist.

Note: Set the amplitude of x(t) to be the **regular** input voltage level of the RX circuit. Don't use small signals.
 Set the bit rate slow enough that almost no ISI will happen, no matter how much bit rate the RX circuit will be applied to in practical usage. For example: 1GT/s

Characterization of $y=C1*\tanh(x/C2)$ – C1 and C2



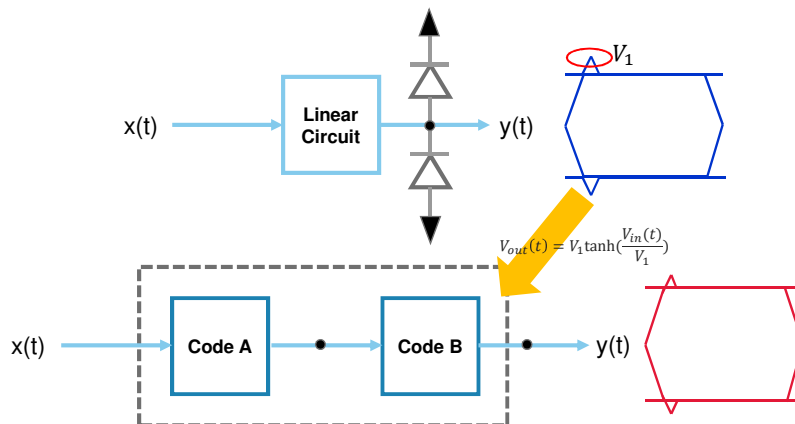
The reason to set the bit rate slow enough, no matter how much bit rate the RX circuit will be applied is:

1. We need the outer and inner contour of the eye which can tell us how much the clamping takes effect and only the clamping takes effect.
2. An eye folded from a slow transition waveform can guarantee the amplitude of the outer and inner contour of the eye is only affected by the clamping but **free from ISI**.
3. Even without any Channel applied, it's impossible to get rid of ISI effect once the circuit is operated under a fast transmission rate

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Characterization of $y=C1*\tanh(x/C2)$ – C1 and C2



Step 2: Start from the value of the outer contour of the eye generated by folding the waveform of transient analysis over the transistor netlist -> Take the value V_1 to replace the C_1 and C_2 in the hyperbolic tangent function, that is,

$$V_{out}(t) = V_1 \tanh\left(\frac{V_{in}(t)}{V_1}\right)$$

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Characterization of $y=C1*\tanh(x/C2)$ – C1 and C2

Step 3: Overlap the two eye diagrams or record the value of the inner contours of these two eye diagrams.

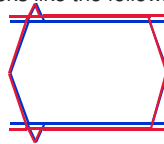
If the eye diagram of **the model under channel analysis** has **higher inner** contour than the eye diagram of **the transistor netlist under transient analysis** -> **Increase C_2** with **increment = 0.25** until the two eyes' inner contours meet each other.

$$V_{out}(t) = V_1 \tanh\left(\frac{V_{in}(t)}{V_1}\right) \uparrow$$

If the eye diagram of **the model under channel analysis** has **lower inner** contour than the eye diagram of **the transistor netlist under transient analysis** -> **Decrease C_2** with **increment = 0.25** until the two eyes' inner contours meet each other.

$$V_{out}(t) = V_1 \tanh\left(\frac{V_{in}(t)}{V_1}\right) \downarrow$$

For example, if the comparison looks like the following, you should **Increase C_2**



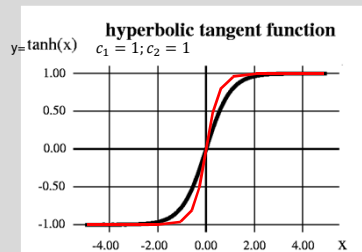
Blue: Generated by SPICE netlist under Transient Analysis
Red: Generated by AMI model under Channel Analysis

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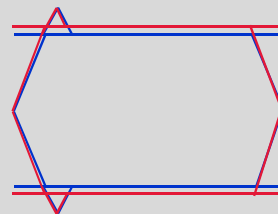
Characterization of $y=C1*\tanh(x/C2)$ – C1 and C2

The reason to cause “**the model under channel analysis** has **higher inner** contour than the eye diagram of **the transistor netlist under transient analysis**” is:



Black: The characteristics of the transistor netlist

Red: The characteristics of the model while applying V_1 to be C_1 and C_2 of the hyperbolic tangent function



Blue: Generated by SPICE netlist under Transient Analysis

Red: Generated by AMI model under Channel Analysis

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Characterization of $y=C1*\tanh(x/C2)$ – C1 and C2

Step 4: Overlap the two eye diagram or record the value of the outer contour of these two eye diagram.

If the eye diagram of **the model under channel analysis** has **higher outer** contour than the eye diagram of **the transistor netlist under transient analysis** -> **Decrease C_1** with **increment = 0.25** until the two eyes' **outer** contour meet each other.

$$V_{out}(t) = V_1 \tanh\left(\frac{V_{in}(t)}{V_2}\right)$$

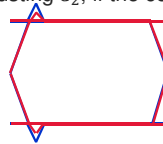
↓

If the eye diagram of **the model under channel analysis** has **lower outer** contour than the eye diagram of **the transistor netlist under transient analysis** -> **Increase C_1** with **increment = 0.25** until the two eyes' **outer** contour meet each other.

$$V_{out}(t) = V_1 \tanh\left(\frac{V_{in}(t)}{V_2}\right)$$

↑

In our previous example, after adjusting C_2 , if the comparison looks like the following, you should **Increase C_1**



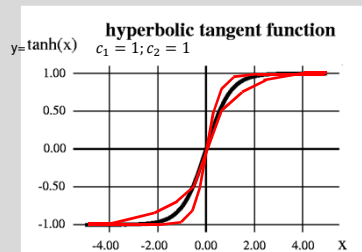
Blue: Generated by SPICE netlist under Transient Analysis
Red: Generated by AMI model under Channel Analysis

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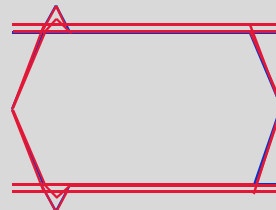
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Characterization of $y=C1*\tanh(x/C2)$ – C1 and C2

The reason to cause "**the model under channel analysis** has **Lower outer** contour than the eye diagram of **the transistor netlist under transient analysis**" **after adjusting C_2** is:



Black: The characteristics of the transistor netlist
Red: The characteristics of the model after adjusting C_2 to make the inner contour of the model meet with the inner contour of the transistor netlist



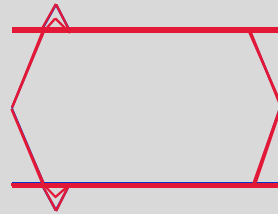
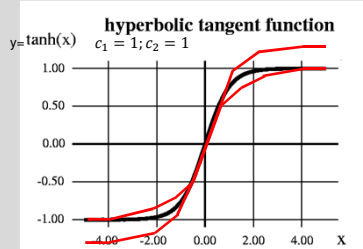
Blue: Generated by SPICE netlist under Transient Analysis
Red: Generated by AMI model under Channel Analysis

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Characterization of $y=C1*\tanh(x/C2)$ – C1 and C2

And **after adjusting C_1** to make the outer contour of the model meet with the outer contour of the transistor netlist:



Black: The characteristics of the transistor netlist

Red: The characteristics of the model after adjusting C_1 to make the outer contour of the model meet with the outer contour of the transistor netlist

Blue: Generated by SPICE netlist under Transient Analysis

Red: Generated by AMI model under Channel Analysis

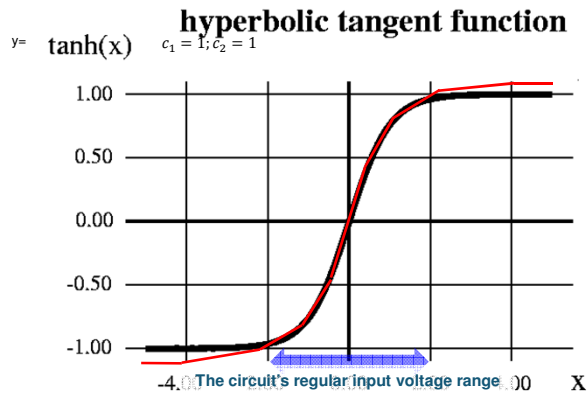
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Characterization of $y=C1*\tanh(x/C2)$ – C1 and C2

Step 5: Go back to Step 3 & Step 4 and keep iterating until you reach a satisfied result.

At the end when you reach a satisfied result, it doesn't imply that we have a hyperbolic tangent function which perfectly overlaps with the circuits characteristics but means that in the circuit's regular input voltage range, we have a hyperbolic tangent function which gets as close to the circuit's characteristics as we wish.



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AMI_GetWave()

- **Does a Hyperbolic Tangent Function have a corresponding frequency response?**

Ans: **Almost impossible** because one of the criteria for a function to be Fourier transformable is

$$\int_{-\infty}^{\infty} |f(x)| dx < \infty$$

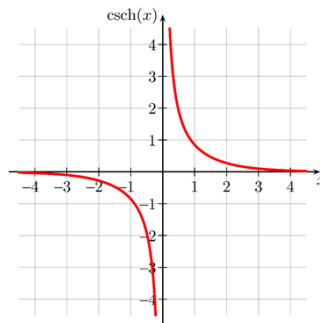
(Absolutely Integrable)

And obviously, Hyperbolic Tangent function fails this criteria. However, just like we can mathematically deduce the Fourier Transform of a unit step function ($F\{u(t)\} = \frac{1}{j\omega} + \pi\delta(\omega)$), we can also mathematically have Hyperbolic Tangent function Fourier Transformed as:

$$F\{\tanh(t)\} = j\sqrt{\frac{\pi}{2}} \cdot \operatorname{csch}\left(\frac{\pi\omega}{2}\right)$$

But what does a Hyperbolic Cosecant function look like?

AMI_GetWave()



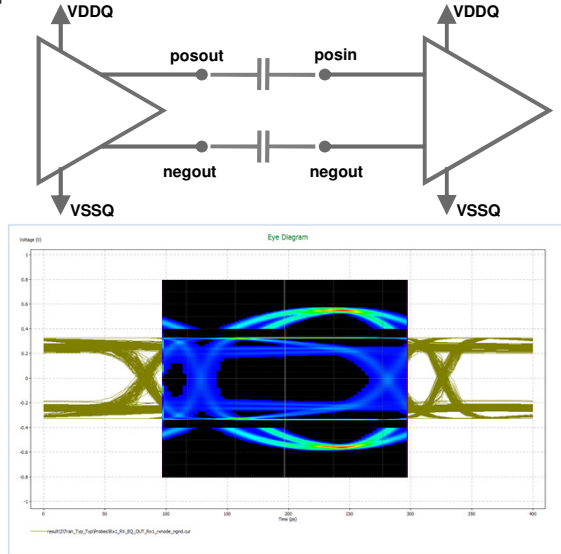
=> What's the value at DC and LF range?

- **The most intuitive way to model a Hyperbolic Tangent function is to implement it in AMI_GetWave()**

```
for (t=0; t<end_time; t++)
{
    Vout[t] = C1*tanh(Vin[t]/C2);
}
```


Example 1

- An USB 3.0 IP, Transmission Rate = 5Gbps, No Channel between Tx and Rx but only a pair of AC Caps:

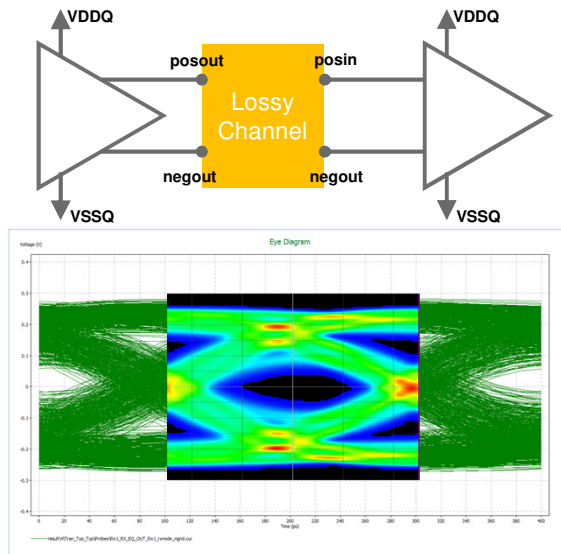


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Example 1 (Cont'd)

- An USB 3.0 IP, Transmission Rate = 5Gbps, Lossy Channel:



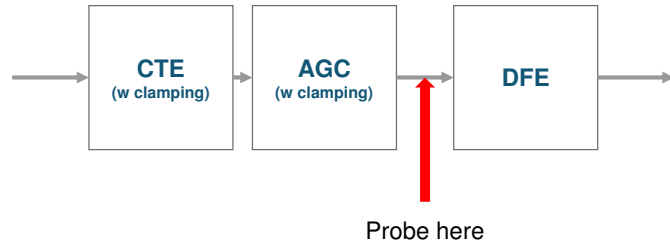
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Example 2

- A PCIe Gen 4.0 IP, Transmission Rate = 16Gbps, M31 published on CDNLive Taiwan 2018

Rough Block Diagram of RX EQ:

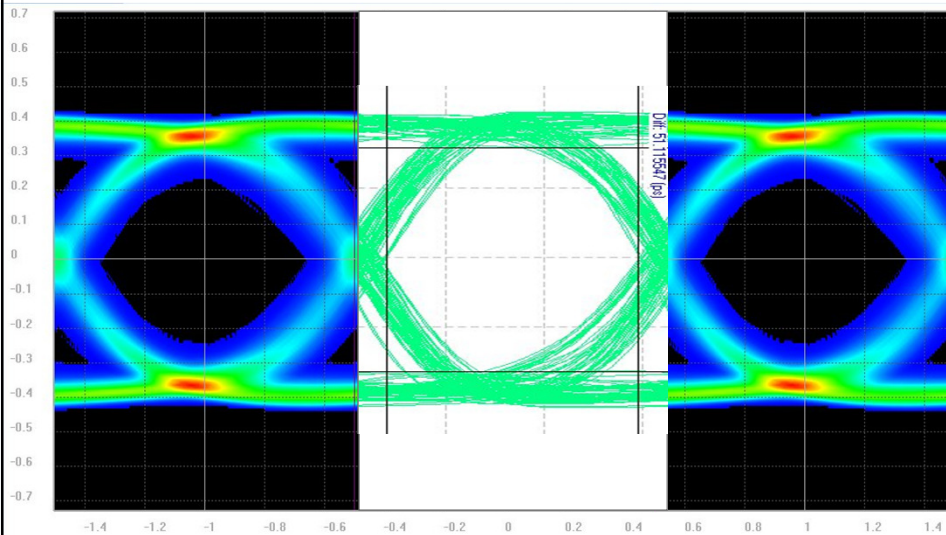


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Example 2 (Cont'd)

- Short Channel – Loss= -10dB

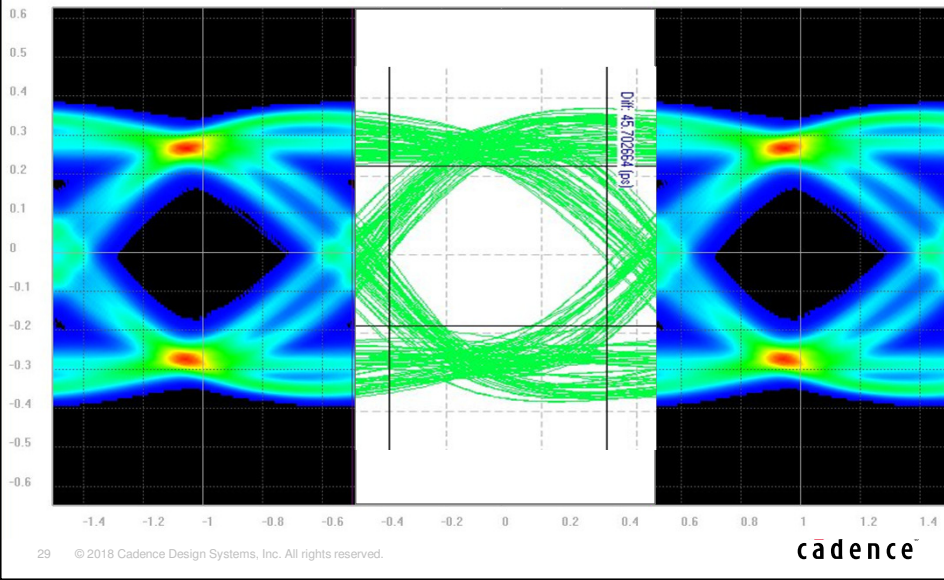


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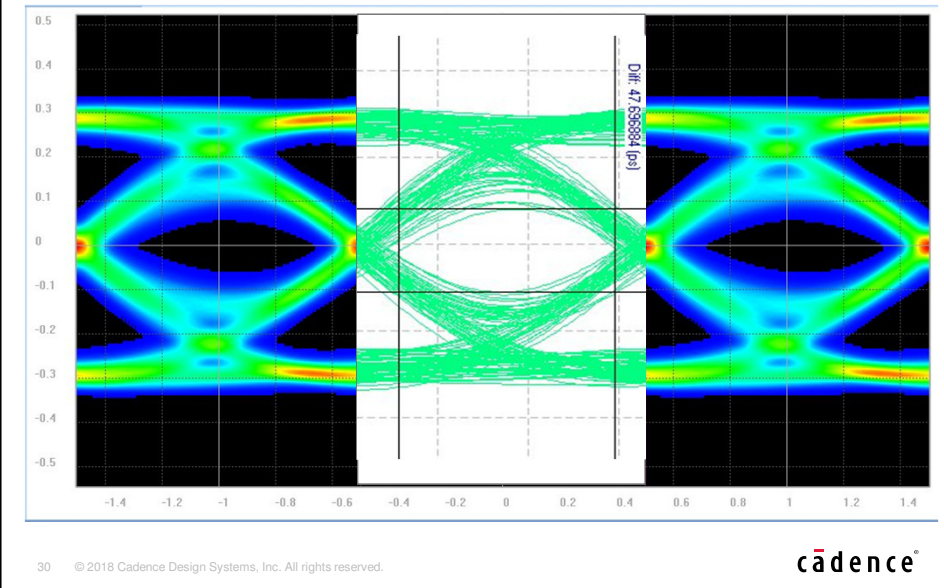
Example 2 (Cont'd)

- Mid Channel – Loss= -18dB



Example 2 (Cont'd)

- Long Channel – Loss= -28dB



Conclusion

- Clamping diodes or circuits with similar behaviors are deemed as protection means and so common to be in most designs which makes most designs to be **Non-Linear**.
- We suggest **Hyperbolic Tangent Function** to be the optimal choice to describe such nonlinearity of circuits.
- We suggest a methodology with which model engineer can approach a nonlinear clamping behavior ultimately.
- Hyperbolic Tangent Function is hard to be implemented in AMI_Init() due to its nature but can be easily and intuitively implemented in **AMI_GetWave()**, for this we even suggest a simplified code.
- According to the description above, this implementation will limit the so-compiled AMI model to work properly in a "Time Domain Analysis" channel simulator but **fail to behave as we desire in a "Statistical" channel simulator**.
- Correlations against SPICE transient analysis are provided and it proves models generated by the methodology we proposed here can accommodate all kinds of channels.

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See you on IBIS Summit 2019

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MODEL CORRELATION FOR IBIS-AMI

Asian IBIS Summit, Taipei, Taiwan, November 16, 2018

Authors:

Wenyan Xie, Guohua Wang, David Zhang, Anders Ekholm

AGENDA



- › Why IBIS-AMI correlation
- › Correlation methodology for TX
- › Correlation methodology for RX
- › Correlation criteria
- › Question and suggestion

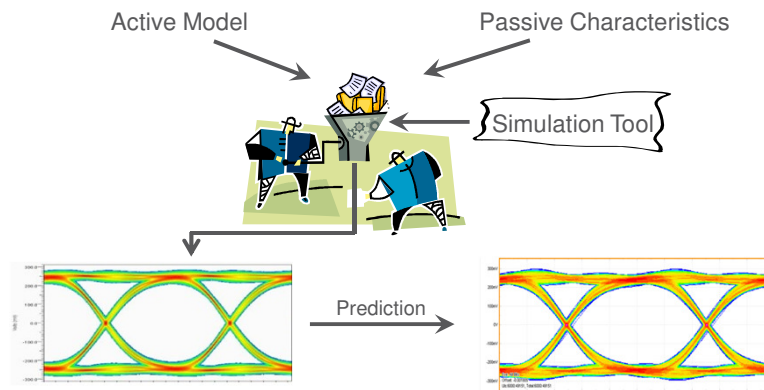
AGENDA



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- › Question and suggestion

Model Correlation for IBIS-AMI | Ericsson Presentation | © Ericsson AB 2018 | November 2018 | Page 3 (30)

WHY CORRELATION FOR IBIS-AMI

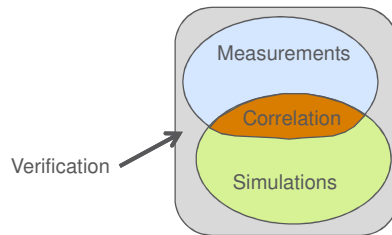


Model Correlation for IBIS-AMI | Ericsson Presentation | © Ericsson AB 2018 | November 2018 | Page 4 (30)

WHY CORRELATION FOR IBIS-AMI



- › Correlation not only can verify simulation model's accuracy, but also can increase the verification coverage once model is matched to real tests. With the correlation, the simulation results can be the part of verification to cover some cases that measurement can not touch.



Model Correlation for IBIS-AMI | Ericsson Presentation | © Ericsson AB 2018 | November 2018 | Page 5 (30)

AGENDA



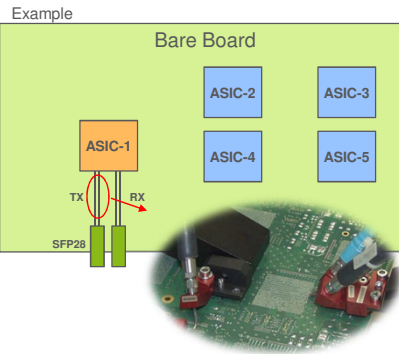
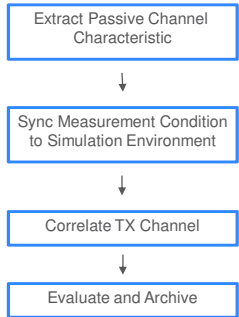
- › Why IBIS-AMI correlation
- › Correlation methodology for TX
- › Correlation methodology for RX
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- › Question and suggestion

Model Correlation for IBIS-AMI | Ericsson Presentation | © Ericsson AB 2018 | November 2018 | Page 6 (30)

CORRELATION METHODOLOGY FOR TX



> Procedure

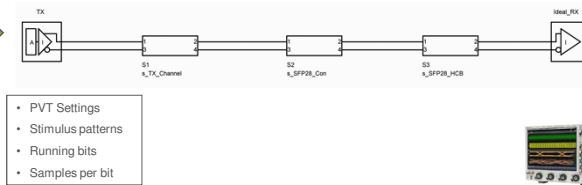
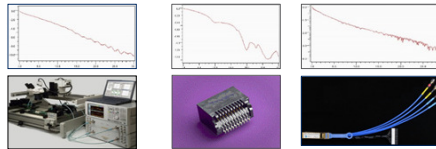
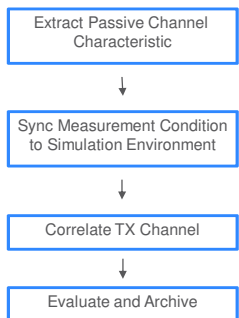


Model Correlation for IBIS-AMI | Ericsson Presentation | © Ericsson AB 2018 | November 2018 | Page 7 (30)

CORRELATION METHODOLOGY FOR TX



> Procedure

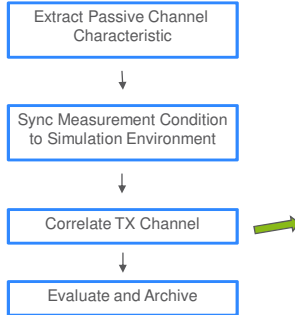


Model Correlation for IBIS-AMI | Ericsson Presentation | © Ericsson AB 2018 | November 2018 | Page 8 (30)

CORRELATION METHODOLOGY FOR TX



Procedure



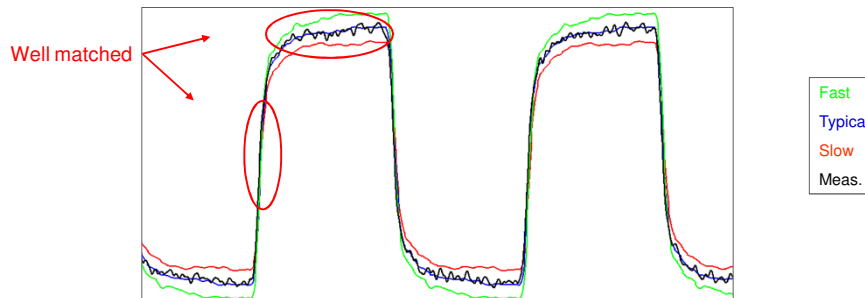
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Case1	0	0	0	0	slow	slow	Case1	0	0	0	0	slow	slow
Case2	1	0	0	0	slow	slow	Case2	1	0	0	0	slow	slow
Case3	2	0	0	0	slow	slow	Case3	2	0	0	0	slow	slow
Case4	3	0	0	0	slow	slow	Case4	3	0	0	0	slow	slow
Case5	4	0	0	0	slow	slow	Case5	4	0	0	0	slow	slow
Case6	5	0	0	0	slow	slow	Case6	5	0	0	0	slow	slow
Case7	6	0	0	0	slow	slow	Case7	6	0	0	0	slow	slow
Case8	7	0	0	0	slow	slow	Case8	7	0	0	0	slow	slow
Case9	8	0	0	0	slow	slow	Case9	8	0	0	0	slow	slow
Case10	9	0	0	0	slow	slow	Case10	9	0	0	0	slow	slow
Case11	10	0	0	0	slow	slow	Case11	10	0	0	0	slow	slow
Case12	11	0	0	0	slow	slow	Case12	11	0	0	0	slow	slow
Case13	12	0	0	0	slow	slow	Case13	12	0	0	0	slow	slow
Case14	13	0	0	0	slow	slow	Case14	13	0	0	0	slow	slow
Case15	14	0	0	0	slow	slow	Case15	14	0	0	0	slow	slow
Case16	15	0	0	0	slow	slow	Case16	15	0	0	0	slow	slow
Case17	8	5	0	0	slow	slow	Case17	8	5	0	0	slow	slow
Case18	8	10	0	0	slow	slow	Case18	8	10	0	0	slow	slow
Case19	8	20	0	0	slow	slow	Case19	8	20	0	0	slow	slow
Case20	8	5	5	5	slow	slow	Case20	8	5	5	5	slow	slow
Case21	8	0	10	10	slow	slow	Case21	8	0	10	10	slow	slow
Case22	8	0	20	20	slow	slow	Case22	8	0	20	20	slow	slow
Case23	8	0	5	5	slow	slow	Case23	8	0	5	5	slow	slow
Case24	8	0	10	10	slow	slow	Case24	8	0	10	10	slow	slow
Case25	8	0	20	20	slow	slow	Case25	8	0	20	20	slow	slow
Case26	8	0	5	5	slow	slow	Case26	8	0	5	5	slow	slow
Case27	8	5	5	5	slow	slow	Case27	8	5	5	5	slow	slow
Case28	8	5	10	10	slow	slow	Case28	8	5	10	10	slow	slow
Case29	8	10	5	5	slow	slow	Case29	8	10	5	5	slow	slow
Case30	8	10	10	10	slow	slow	Case30	8	10	10	10	slow	slow

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CORRELATION RESULTS FOR TX



Slow Clock Pattern – Edge and Amplitude Voltage

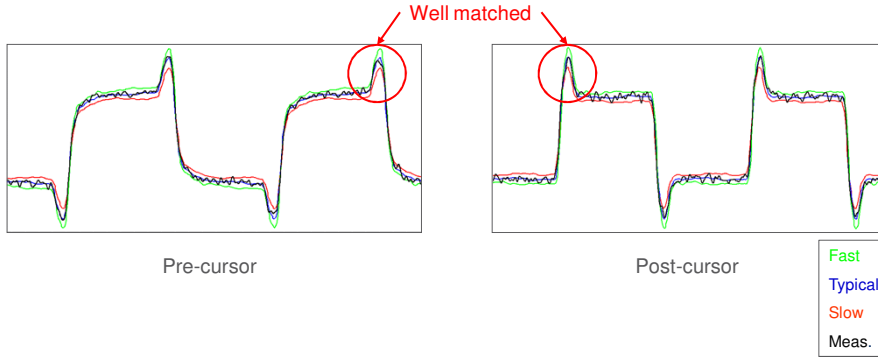


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CORRELATION RESULTS FOR TX



› Slow Clock Pattern – FFE Taps

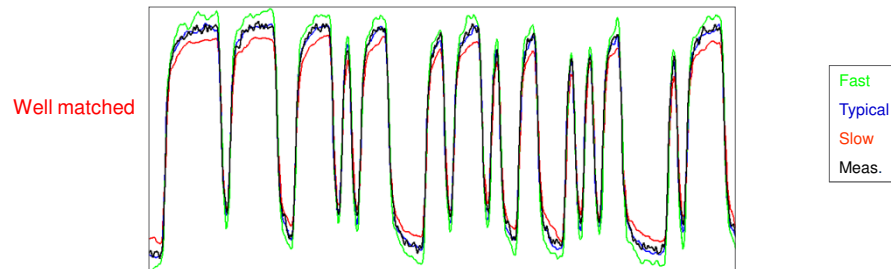


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CORRELATION RESULTS FOR TX



› PRBS7 Pattern – Fast Response

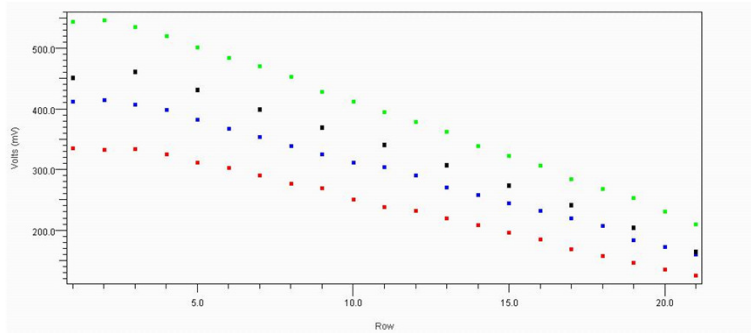


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TREND CORRELATION FOR TAP



Time Domain Eye Height – Precursor Sweep



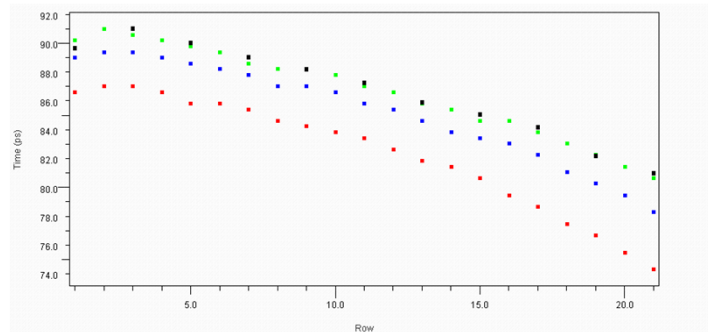
Fast
Typical
Slow
Meas.

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TREND CORRELATION FOR TAP



Time Domain Eye Width – Precursor Sweep



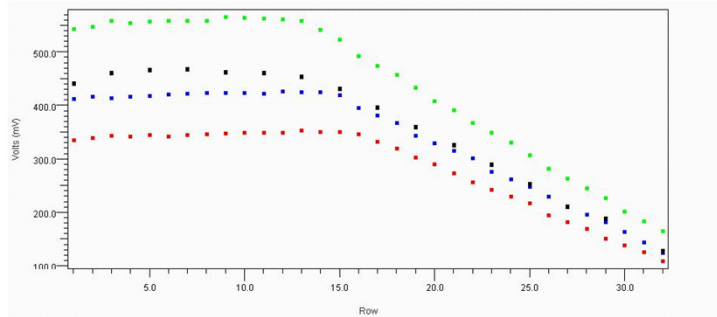
Fast
Typical
Slow
Meas.

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TREND CORRELATION FOR TAP



Time Domain Eye Height – Postcursor Sweep



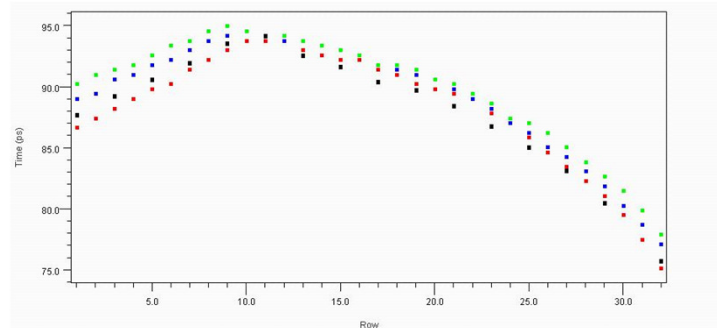
Fast
Typical
Slow
Meas.

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TREND CORRELATION FOR TAP



Time Domain Eye Width – Postcursor Sweep



Fast
Typical
Slow
Meas.

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AGENDA



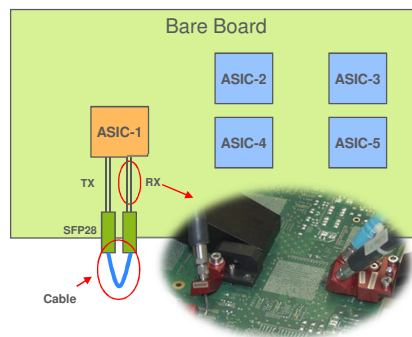
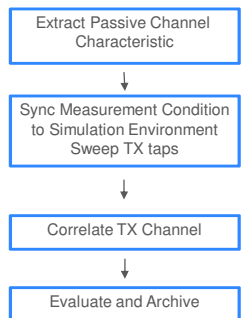
- › Why IBIS-AMI correlation
- › Correlation methodology for TX
- › Correlation methodology for RX
- › Correlation criteria
- › Question and suggestion for

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CORRELATION METHODOLOGY FOR RX



› Procedure

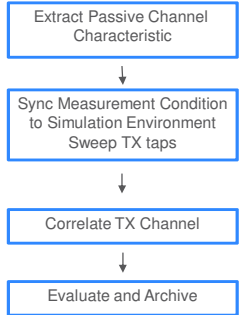


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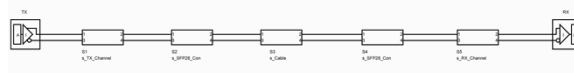
CORRELATION METHODOLOGY FOR RX



Procedure



- Cable Length:
 - 0.6m
 - 1.0m
 - 1.8m
 - 3.0m
 - 5.0m



- PVT Settings
- Stimulus patterns
- Running bits
- Samples per bit
- Taps sweep

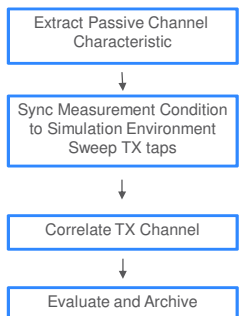
- RX CTLE adapt
- RX CTLE and DFE adapt

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CORRELATION METHODOLOGY FOR RX



Procedure



Item	TXDFPCTRL[3:0]	TXPRECURSOR[4:0]	TXPOSTCURSOR[4:0]	RX Equalization	Pattern	Output
Case1	8	0	0	CTLE Adapt Only	prb27	Internal eye
Case2	8	5	0	CTLE Adapt Only	prb27	Internal eye
Case3	8	10	0	CTLE Adapt Only	prb27	Internal eye
Case4	8	15	0	CTLE Adapt Only	prb27	Internal eye
Case5	8	20	0	CTLE Adapt Only	prb27	Internal eye
Case6	8	0	5	CTLE Adapt Only	prb27	Internal eye
Case7	8	0	10	CTLE Adapt Only	prb27	Internal eye
Case8	8	0	15	CTLE Adapt Only	prb27	Internal eye
Case9	8	0	20	CTLE Adapt Only	prb27	Internal eye
Case10	8	0	25	CTLE Adapt Only	prb27	Internal eye
Case11	8	0	31	CTLE Adapt Only	prb27	Internal eye
Case12	8	5	5	CTLE Adapt Only	prb27	Internal eye
Case13	8	5	10	CTLE Adapt Only	prb27	Internal eye
Case14	8	10	5	CTLE Adapt Only	prb27	Internal eye
Case15	8	10	10	CTLE Adapt Only	prb27	Internal eye
Case16	8	0	0	DFE&CTLE Adapt	prb27	Internal eye
Case17	8	5	0	DFE&CTLE Adapt	prb27	Internal eye
Case18	8	10	0	DFE&CTLE Adapt	prb27	Internal eye
Case19	8	15	0	DFE&CTLE Adapt	prb27	Internal eye
Case20	8	20	0	DFE&CTLE Adapt	prb27	Internal eye
Case21	8	0	5	DFE&CTLE Adapt	prb27	Internal eye
Case22	8	0	10	DFE&CTLE Adapt	prb27	Internal eye
Case23	8	0	15	DFE&CTLE Adapt	prb27	Internal eye
Case24	8	0	20	DFE&CTLE Adapt	prb27	Internal eye
Case25	8	0	25	DFE&CTLE Adapt	prb27	Internal eye
Case26	8	0	31	DFE&CTLE Adapt	prb27	Internal eye
Case27	8	5	5	DFE&CTLE Adapt	prb27	Internal eye
Case28	8	5	10	DFE&CTLE Adapt	prb27	Internal eye
Case29	8	10	5	DFE&CTLE Adapt	prb27	Internal eye
Case30	8	10	10	DFE&CTLE Adapt	prb27	Internal eye

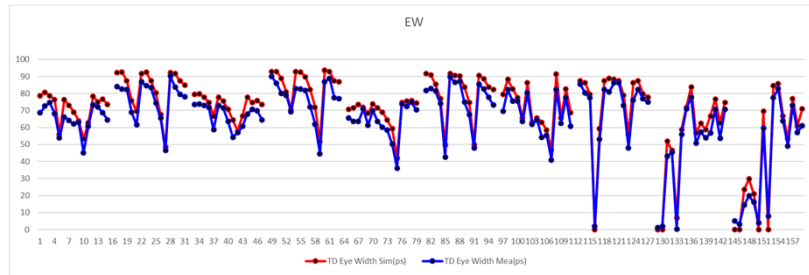
- Sweep Cable Length:
 - 0.6m
 - 1.0m
 - 1.8m
 - 3.0m
 - 5.0m

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CORRELATION RESULTS FOR RX



› Trend Correlation – Time Domain Eye Width



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AGENDA



- › Why IBIS-AMI correlation
- › Correlation methodology for TX
- › Correlation methodology for RX
- › Correlation criteria
- › Question and suggestion for

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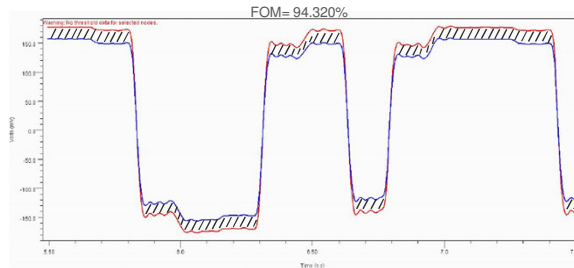
CORRELATION CRITERIA



Figure of Merit (FOM)

$$FOM = 100 \cdot \left[1 - \frac{\sum_{i=1}^N |X_i(\text{golden}) - X_i(\text{DUT})|}{\Delta X \cdot N} \right]$$

FOM Value	Qualitative Metric
> 99%	Excellent
> 95%	Very Good
> 90%	Good
< 90%	Poor



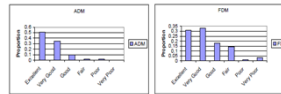
CORRELATION CRITERIA



Feature Selective Validation (FSV)

The Feature Selective Validation (FSV) method is one of the candidate techniques for the **quantitative validation** of computational electromagnetics (CEM), particularly within electromagnetic compatibility (EMC) and Signal Integrity (SI).

It is based on the decomposition of the original data into two parts: **amplitude (ADM) data** and **feature data (FDM)**. The former will account for the slowly varying data across the data set and the latter will account for the sharp peaks and troughs.



FSV value (quantitative)	FSV interpretation (qualitative)
Less than 0.1	Excellent
Between 0.1 and 0.2	Very good
Between 0.2 and 0.4	Good
Between 0.4 and 0.8	Fair
Between 0.8 and 1.6	Poor
Greater than 1.6	Very poor

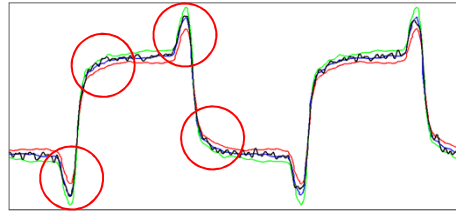
Reference
 1. Roy Leventhal, "Correlation of Model Simulations and Measurements", Leventhal Design & Communications Presented June 5, 2007 IBIS Summit Meeting, San Diego, California
 2. D.Di Febo, F.de Paulis, A.Orlandi "Feature Selective Validation- A new approach for new Engineers" European IBIS Summit Naples, May11, 2011

CORRELATION CRITERIA



› More metrics to correlate

- Besides 5 metrics "high level, low level, rise time, fall time, and duty cycle", more metrics are necessary: slew rate, cursor pillars..and the metrics should have different weight in final score calculation.



Reference
1. David Banas, "IBIS-to-Spice Correlation a story of 5 metrics", Presented June 5, 2007 IBIS Summit San Diego, California

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AGENDA



- › Why IBIS-AMI correlation
- › Correlation methodology for TX
- › Correlation methodology for RX
- › Correlation criteria
- › Question and suggestion

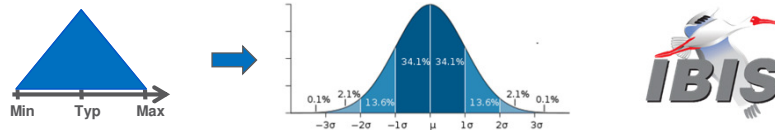
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QUESTION AND SUGGESTION



- › In the paper, Measurement is on Typical corner. No Fast and Slow corners measurement data. So,
Can we trust the Fast and Slow corners simulation data, even though Typical correlates very well?
How much do the corners of AMI model match the real silicon's behavior?
99.99%...? It is a statistical problem.

- › We need to introduce the statistical distribution for Fast/Typical/Slow corners of IBIS.



- › We need more metrics for correlation evaluation. Some are proposed in this paper.

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ERICSSON

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Study of DDR Asymmetric Rt/Ft in Existing IBIS-AMI Flow

Asian IBIS Summit
Taipei, Taiwan
November 16th, 2018

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Wei-hsing.Huang@spisim.com
Wei-kai Shih, SPISim
Wei-kai.Shih@spisim.com

1



Agenda:

- Motivation
- Background
- Asymmetric Rt/Ft
- AMI_Init
- AMI_GetWave
- Summary
- Q & A

2



Motivation

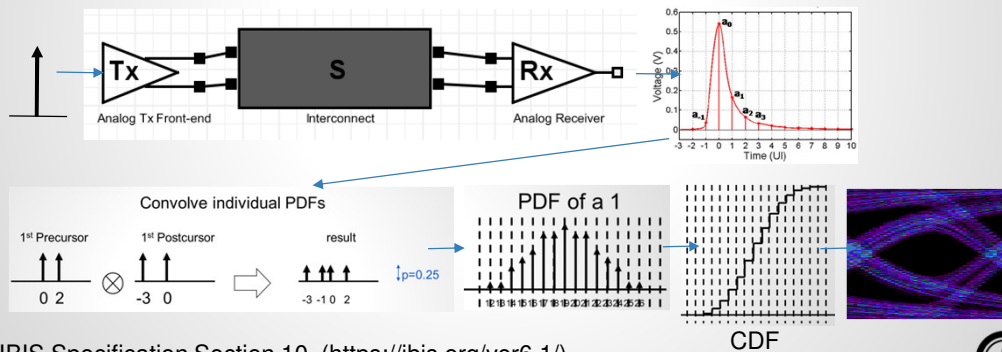
- IBIS-AMI analysis flows:
 - Statistical: use impulse response and AMI_Init
 - Time-domain: use convolution and mainly AMI_GetWave
- Existing applications focused on SERDES
 - Differential, centered around $V = 0.0$
 - Symmetric rise-time (Rt) /fall-time (Ft)
- How DDR may work in existing AMI flow?
 - Single-ended e.g. DQ
 - Asymmetric Rt/Ft

3



Background 1/2

- Statistical AMI flow: [*]
 - Impulse Response for analog + channel (Linear Time Invariant, LTI)
 - Samples -> PDF -> CDF -> BER/Eye



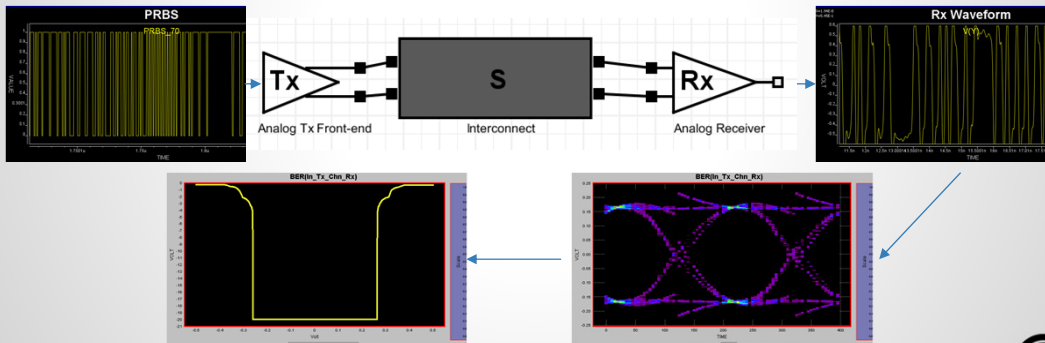
[*] IBIS Specification Section 10. (<https://ibis.org/ver6.1/>)

4



Background 2/2

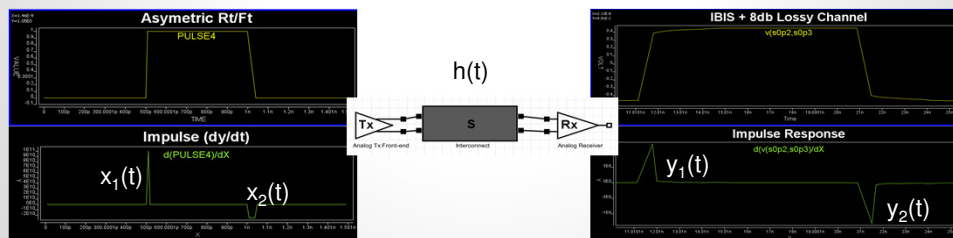
- Time-domain AMI flow:
 - Analog + channel's responses to one block of bit-sequence
 - Convolve with Tx/Rx's AMI_GetWave respectively



5

Asymmetric Rt/Ft to Impulse:

- Linear transform between Rt/Ft:
 - Rise: $y_1(t) = x_1(t) * h(t)$ Fall: $y_2(t) = x_2(t) * h(t)$
 - Fall: $x_2(t) = x_1(t) * Xform(t) \Rightarrow y_2(t) = y_1(t) * Xform(t)$
 - Simulator knows y_1 & y_2 , thus $Xform(t)$. It can then reconstruct either y_1 or y_2 from y_2 or y_1 used in AMI_Init
 - DC info disappeared during differentiation (to get impulse response). **Has gap!**
Need specification change or new parameter to convert to single-ended.



6

Example:

- Matlab/Octave pseudo-code:

```

% Generate rise and fall ramp of different slew rates
clc;
clear;
time1 = (-1:1:5)';
ustp1 = time1>=0;
xstp = time1.*ustp1;

time = (-1:1:2)';
ustp = time>=0;
ystp = time.*ustp;

m1en = 10;
rstp = ones(m1en, 1);
rstp(1:size(xstp,1), 1) = xstp / 5;

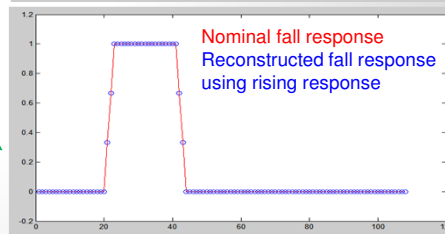
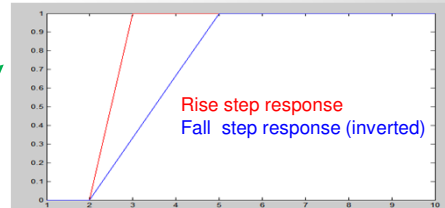
f1stp = ones(m1en, 1);
f1stp(1:size(ystp,1), 1) = ystp / 3;

% Convert to impulse
r1imp = diff(rstp);
f1imp = diff(f1stp);

% Nominal rise and fall pulse response
pulse=zeros(100,1);
pulse(20:40,1)=1;
rpuls=conv(r1imp, pulse);
fpuls=conv(f1imp, pulse);

% Reconstruct fall pulse using XForm
plen =size(rpuls, 1);
xpuls=real(1/fft(fft(rpuls, plen) ./ fft(rimp, plen) .* fft(rpuls)));

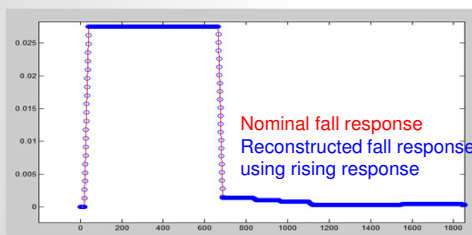
% Plot them together
time=[1:plen];
plot(time, fpuls, 'r-', time, xpuls, 'bo');
    
```



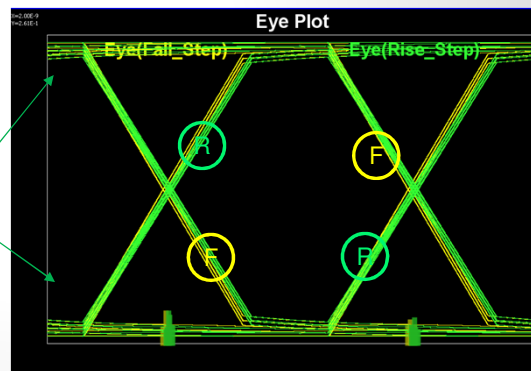
7

Asymmetric Rt/Ft to Eye:

- Construct different eyes portions using eyes generated by rise response and fall response (different slew rate)
 - Eye will be asymmetric as well.



Real case: (IBIS + Lossy Channel)



8

ISI Eye Construction with a Tree Structure

3	2	1	Cursor (0)	-1	
0	0	0	1	0	
1					
0	1	1		1	1
1					
0	0	1	1		1
1					
0	1	1		1	1
1					

Let $V_n(ab)$ be the contribution of ISI from the n th pre-cursor edge when the n th pre-cursor= a and $(n-1)$ th pre-cursor= b , i.e. the n th pre-cursor edge is an $a \rightarrow b$ transition

When 2nd pre-cursor logic value = 0, cursor logic value = 1, all possible values for the accumulated ISI from 2nd and 1st pre-cursors can be put into a row vector: $[V_2(00) + V_1(01), V_2(01) + V_1(11)]$. There are two elements in the vector due to two possible values of the 1st pre-cursor

Extending to the 3rd pre-cursor: When 3rd pre-cursor = 0, there are 4 possible accumulated ISI values

$[V_3(00) + V_2(00) + V_1(01), V_3(00) + V_2(01) + V_1(11)]$ and $[V_3(01) + V_2(10) + V_1(01), V_3(01) + V_2(11) + V_1(11)]$

9



Recursive Algorithm for ISI Eye Construction

n	n-1	1 ... n-2	Cursor (0)				
0	0	xxxxxxxx	1				
1							
0	1			xxxxxxxx	1		
1							

$W_n(ab)$: row vector consisting all possible values of the accumulated ISI from the n th pre-cursor to cursor when logic value of the n th pre-cursor is a and logic value at cursor is b

$$\begin{aligned}
 W_1(01) &= [V_1(01)] \\
 W_1(11) &= [V_1(11)] \\
 W_2(01) &= [V_2(00) + V_1(01), V_2(01) + V_1(11)] \\
 W_2(11) &= [V_2(10) + V_1(01), V_2(11) + V_1(11)] \\
 &\dots \dots \dots \\
 W_n(01) &= [V_n(00) + W_{n-1}(01), V_n(01) + W_{n-1}(11)] \\
 W_n(11) &= [V_n(10) + W_{n-1}(01), V_n(11) + W_{n-1}(11)]
 \end{aligned}$$

10



PDF Computation for ISI Eye

Waveform value	PDF of the waveform value	Notes
$V_n(ab)$	$P_{V_n(ab)}(V) = \delta(V - V_n(ab))$	
$W_1(01)$	$P_{W_1(01)} = P_{V_1(01)} \quad P_{W_1(11)} = P_{V_1(11)}$	
$W_n(01)$	$P_{W_n(01)} = \frac{1}{2} P_{W_{n-1}(01)} \otimes P_{V_n(00)}(V) + \frac{1}{2} P_{W_{n-1}(11)} \otimes P_{V_n(01)}$	
$W_n(11)$	$P_{W_n(11)} = \frac{1}{2} P_{W_{n-1}(01)} \otimes P_{V_n(10)}(V) + \frac{1}{2} P_{W_{n-1}(11)} \otimes P_{V_n(11)}$	

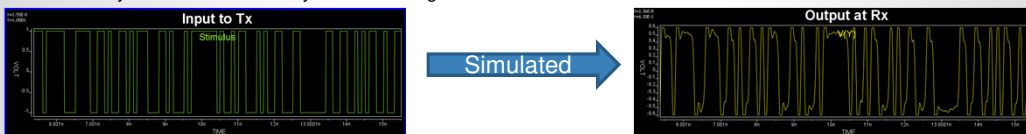
This is a Dirac delta when there is no jitter (ISI takes discrete value without jitter)
 With jitter the Dirac delta will spread out into a continuous distribution. But the recursive relation remains same

11

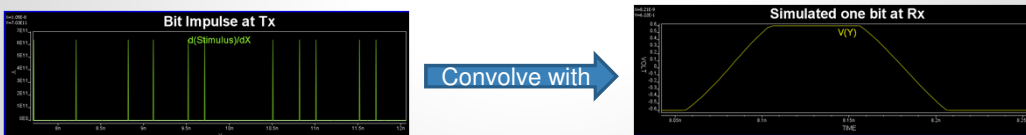


Asymmetric Rt/Ft to GetWave:

- Result will be OK if:
 - Bit-sequence waveform at Rx is simulated result from bit-sequence input at Tx
 - This may not be the case mostly as it takes longer to run.



- Result will have errors if:
 - Final waveform at Rx is from one bit simulated Rx response convolved with bit-sequence impulse at Tx

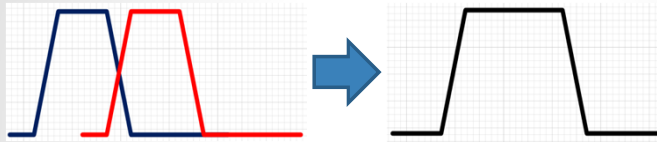


12



Asymmetric Rt/Ft to GetWave:

- Bit 011 using convolution with symmetric Rt/Ft



- Glitch will happen for asymmetric Rt/Ft



13



Asymmetric Rt/Ft to GetWave:

- Matlab/Octave pseudo-code:

```
% Generate one-bit pulse of different Rt/Ft
clc;
clear;
time = (0:1:2)';
ustp = time>=0;
xstp = time.*ustp;

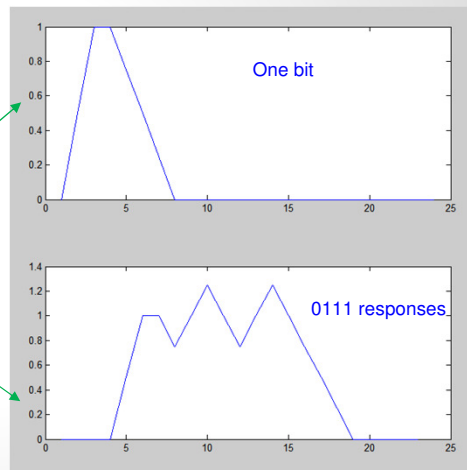
time1 = (0:1:4)';
ustp1 = time1>=0;
ystp = time1.*ustp1;

xlen = size(xstp, 1);
ylen = size(ystp, 1);
mlen = xlen + ylen;
bit1 = ones(mlen, 1);
bit1(1:xlen, 1) = xstp / 2;
bit1(xlen + 1:xlen + ylen, 1) = 1 - ystp / 4;

% Bit sequence 0111
u1 = size(bit1, 1) / 2;
blen = 4 * u1;
bseq = zeros(blen, 1);
bseq(1 * u1) = 1;
bseq(2 * u1) = 1;
bseq(3 * u1) = 1;

% Form responses using convolution
resp = conv(bit1, bseq);

% Plot them together
subplot(2,1,1);
plot(padarray(bit1, blen, 'post'));
subplot(2,1,2);
plot(resp);
```



14



Summary:

- Existing IBIS-AMI flow:
 - Can be used for driver with asymmetric Rt/Ft.
 - Asymmetric effects can be handled within EDA tools/Simulator.
 - Assuming AMI model does not behave differently to rise/fall responses.
- Statistical flow:
 - Linear transform between rise/fall can be applied to model's response.
 - Use rise and fall response to construct eye.
 - Tree/sequence based superposition will eliminate these glitches.
- Time-domain flow:
 - Convolution using one bit pulse will have errors.
 - Using step response based superposition may avoid such errors.

15



16 SPISim is an InSync member.

