WELCOME FROM RANDY WOLFF, IBIS OPEN FORUM

Ladies and Gentlemen,

As chair of the IBIS Open Forum it is my pleasure to welcome you to the 2019 Asian IBIS Summit in Shanghai and to thank you for your presentations and participation. We are grateful to our sponsors Huawei Technologies, ANSYS, Cadence Design Systems, Keysight Technologies, Synopsys, and ZTE Corporation, for making this event possible.

Since 1993, IBIS has provided the digital electronics industry with specifications to make signal, timing, and power integrity analyses much easier and faster. With the introduction of IBIS-AMI in 2008, the IBIS community generated new energy for high speed electronic design. IBIS is now known by engineers worldwide and is a required technology for many applications. IBIS Version 7.0 was released in 2019, adding enhancements for IBIS-AMI and supporting advanced interconnect modeling.

Support for IBIS in Asia has been strong, and the IBIS Open Forum looks forward to continued innovation and contributions from technology companies in Asia.

Thank you!

Randy Wolff
Micron Technology
Chair, IBIS Open Forum

WELCOME FROM RANDY WOLFF, IBIS OPEN FORUM

女士们先生们，

作为 IBIS 开放论坛的主席，我高兴地欢迎您参加 2019 年上海亚洲 IBIS 峰会，感谢您的介绍和参与。我们非常感谢我们的赞助商华为技术有限公司，ANSYS，Cadence Design Systems，Keysight Technologies, Synopsys，为此事件做出了可能。

自 1993 年以来，IBIS 为数字电子行业提供了使信号，时序和电源完整性分析更容易和更快速的规范。随着 IBIS-AMI 在 2008 年的推出，IBIS 社区为高速电子设计创造了新的能量。 IBIS 现在已被世界各地的工程师所了解，是许多应用所需的技术。2019 年，新的 IBIS 7.0 版本包含了更多的 IBIS-AMI 模型和互联接口模型的定义及提升。

IBIS 在亚洲的支持一直很强，IBIS 开放论坛期待着亚洲技术公司的不断创新和贡献。

谢谢!

Randy Wolff (兰迪·沃尔夫)
Micron Technology 公司
主席，IBIS 开放论坛

WELCOME FROM HANG YAN, HUAWEI TECHNOLOGIES

Ladies and Gentlemen,

On behalf of Huawei Technologies, welcome to the 15th annual Asian IBIS Summit (China). I would like to express my appreciation to IBIS Open Forum and all the sponsors for co-organizing this event.

Since 2005, IBIS Asian Summit in China has been the top-level international conference in high speed digital design society in China. I am looking forward to working with IBIS members in China, and to expand our participation in the region. With the demands of high speed design, modeling and simulation technology will still be the key to find the solution. Accuracy, efficiency and complexity are the challenge we are facing now. Intelligence and digitization will be the trend.

Huawei has been actively involved in all IBIS society's events. We hope to resolve high speed link issues with IBIS Open Forum, EDA vendors and IC vendors. Your comments and suggestions will be deeply appreciated! And any suggestion for China region technical discussion and activity are also welcome!

Welcome all of you to Shanghai! Hope you will enjoy all the technical discussions and sharing throughout the meeting, and have a nice journey!

Thank you!
Hang Yan
Huawei Technologies

WELCOME FROM HANG YAN, HUAWEI TECHNOLOGIES

各位专家，各位来宾：

我代表华为公司，欢迎大家来参加第 15 洲 IBIS 技术研讨会，衷心地感谢 IBIS 协会组织本次会议。

自从 2005 年以来，IBIS 技术研讨会已经成为了中国高速设计领域的一次盛会。我很高兴有机会与 IBIS 协会一起促进和扩大在该领域的分享。在未来的高速设计中，模型和仿真技术仍将是解决问题的重要手段，准确度、速度和复杂度是我们面临的挑战，智能化和数字化是未来的方向。

华为积极参与各项 IBIS 活动，希望与 IBIS 协会、EDA 软件、芯片公司一道来共同解决许多高速链路设计上的挑战，欢迎大家会上讨论。同时也欢迎大家对我们中国区在 IBIS 技术讨论和组织上提出建议。

欢迎 IBIS 专家来到上海，希望你们能够喜欢所有的技术讨论和会议分享，度过美好一天。

谢谢大家
华为公司 严航

AGENDA AND ORDER OF THE PRESENTATIONS

(The actual agenda might be modified)

I B I S S U M M I T M E E T I N G A G E N D A

9:00 **SIGN IN**
- Vendor Tables Open at 8:30

9:30 **WELCOME**
- Yan, Hang (Paul)
  (Huawei Technologies, China)
- Wolff, Randy (Chair, IBIS Open Forum)
  (Micron Technology, USA)

9:40 **IBIS Chair's Report** **7**
Wolff, Randy (Micron Technology USA)

10:00 **How to Obtain Buffer Impedance from IBIS** **15**
Wang, Lance (Zuken, USA)

10:20 **C-PHY SI Simulation with IBIS Model** **24**
Zhang, Bailing (ANSYS, China)

10:35 **BREAK** (Refreshments and Vendor Tables)

10:55 **Innovations in DDR Memory Simulation** **28**
Slater, Stephen (Keysight Technologies, USA)
[Presented by Zhao, Jiajie (Keysight Technologies, China)]

11:20 **IBIS-AMI & COM Co-design for 25G Serdes** **40**
Hou* Nan; Zhang# Amy, Wang#, Guohua; Zhang##, David;
Ekholm##, Anders (Ericsson, #China, ##Sweden)
[Presented by Hou, Nan (Ericsson, China)]

12:00 **FREE BUFFET LUNCH** (Hosted by Sponsors)
- Vendor Tables

AGENDA AND ORDER OF THE PRESENTATIONS (Continued)

13:30 **How To Fix a Short Channel Problem With AMI and COM Simulation . . . 55**
Ye, Dongdong; Zhu Shunlin (ZTE Corporation, China)
[Presented by Ye, Dongdong (ZTE Corporation, China)]

14:00 **Celestica 112G SI Channel Study for 800G Switch 64**
Shi, Bowen; Feng, Sophia (Celestica, China)
[Presented by Shi, Bowen (Celestica, China)]

14:30 **Channel Simulation Over DDR4/5 and Above 72**
Keshavan#, Kumar; Varma#, Ambrish; Willis#, Ken;
Liang##, Skipper
(Cadence Design Systems, #USA, ##China)
[Presented by Liang, Skipper (Cadence Design Systems, China)]

15:05 **CONCLUDING ITEMS**

15:10 **END OF IBIS SUMMIT MEETING**

15:10 **BREAK** (Refreshments and Vendor Tables))

15:30 **VENDOR PRESENTATIONS, MODERATOR**
- Wang, Lance (Vice-chair, IBIS Open Forum)
(Zuken, USA)

17:30 **END OF VENDOR PRESENTATIONS**

IBIS Chair's Report

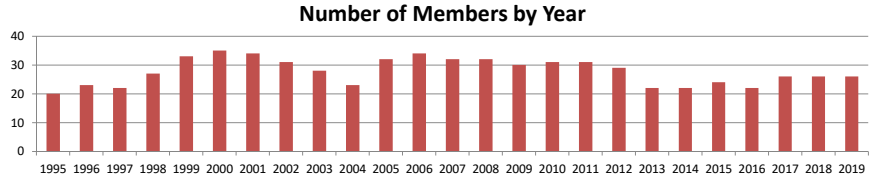
Randy Wolff
Micron Technology
Chair, IBIS Open Forum

2019 Asian IBIS Summits
Shanghai, China
November 1, 2019

http://www.ibis.org/

Organization

26 IBIS Members



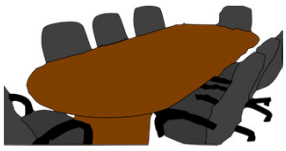
Organization

IBIS Officers 2019-2020

Chair:	*Randy Wolff, Micron Technology*
Vice-Chair:	*Lance Wang, Zuken USA*
Secretary:	*Curtis Clark, ANSYS*
Treasurer:	*Bob Ross, Teraspeed Labs*
Librarian:	*Anders Ekholm, Ericsson*
Postmaster:	*Mike LaBonte, SiSoft (MathWorks)*
Webmaster:	*Steve Parker, GlobalFoundries*

Organization

IBIS Meetings



- Weekly teleconferences
  - Quality Task Group (Tuesdays)
  - Advanced Technology Modeling Task Group (Tuesdays)
  - Interconnect Task Group (Wednesdays)
  - Editorial Task Group (some Fridays)
- IBIS Open Forum teleconference every 3 weeks
  - 502 meetings so far
- IBIS Summit meetings: DesignCon, IEEE SPI, Shanghai, Taipei, Tokyo

Organization

SAE ITC

- SAE Industry Technologies Consortia is the parent organization of the IBIS Open Forum
- IBIS is assisted by SAE employees José Godoy, Phyllis Gross, Laurie Strom
- SAE ITC provides financial, legal, and other services
- http://www.sae-itc.org/

Organization

Task Groups

- Interconnect Task Group
  - Chair: Michael Mirmak, Intel
  - http://ibis.org/interconn_wip/
  - Develop on-die/package/module/connector interconnect modeling BIRDs
- Advanced Technology Modeling Task Group
  - Chair: Arpad Muranyi, Mentor, A Siemens Business
  - http://ibis.org/atm_wip/
  - Develop most other technical BIRDs
- Quality Task Group
  - Chair: Mike LaBonte, SiSoft (MathWorks)
  - http://ibis.org/quality_wip/
  - Oversee IBISCHK parser testing and development
- Editorial Task Group
  - Chair: Michael Mirmak, Intel
  - http://ibis.org/editorial_wip/
  - Produce IBIS Specification documents

BIRD = Buffer Issue Resolution Document

Specification Development

IBIS Milestones

I/O Buffer Information Specification

- 1993-1994 **IBIS 1.0-2.1**:
  - Behavioral buffer model (fast simulation)
  - Component pin map (easy EDA import)
- 1997-1999 **IBIS 3.0-3.2**:
  - Package models
  - Electrical Board Description (EBD)
  - Dynamic buffers
- 2002-2006 **IBIS 4.0-4.2**:
  - Receiver models
  - AMS languages
- 2007-2012 **IBIS 5.0-5.1**:
  - IBIS-AMI SerDes models
  - Power aware
- 2013-2015 **IBIS 6.0-6.1**:
  - PAM4 multi-level signaling
  - Power delivery package models
- 2019 **IBIS 7.0**:
  - Back-channel support
  - Interconnect modeling using IBIS-ISS and Touchstone

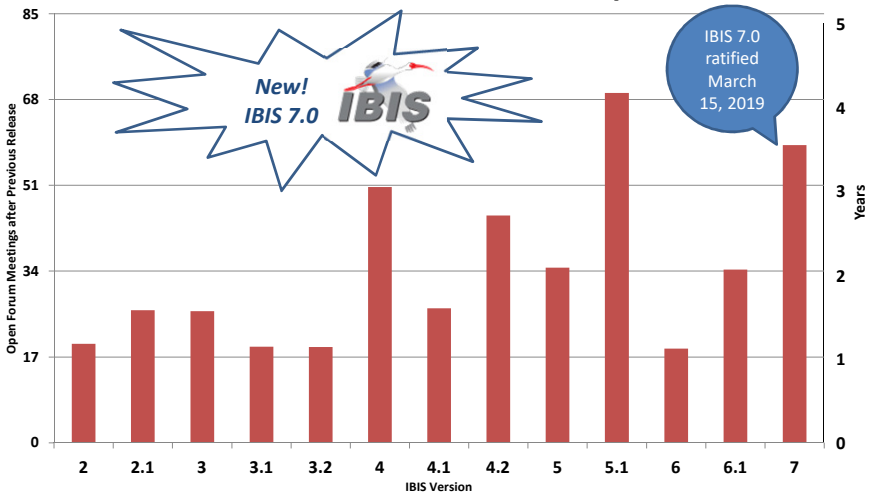
Other Work

- 1995: **ANSI/EIA-656**
  - IBIS 2.1
- 1999: **ANSI/EIA-656-A**
  - IBIS 3.2
- 2001: **IEC 62014-1**
  - IBIS 3.2
- 2003: **ICM 1.0**
  - Interconnect Model Specification
- 2006: **ANSI/EIA-656-B**
  - IBIS 4.2
- 2009: **Touchstone 2.0**
- 2011: **IBIS-ISS 1.0**
  - Interconnect SPICE Subcircuit specification

2019 Asian IBIS Summits - IBIS Chair's Report 7

Specification Development

IBIS Version Development



2019 Asian IBIS Summits - IBIS Chair's Report 8

Specification Development

IBISCHK7 Version 7.0.0

- Executables available at www.ibis.org/ibischk7/
  - Interconnect Model syntax
  - Subdirectory references
  - Bus_label definitions
  - Etc.
- Contact treasurer@ibis.org for Source Code License purchase ($3,000)

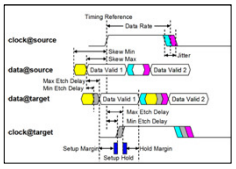
Beyond IBIS 7.0

- Currently 5 BIRDs in discussion
  - 2 about redriver flow (BIRD166.4, BIRD190)
  - 1 editorial (BIRD181.1)
  - 1 to support single-ended IBIS-AMI (BIRD197.4)
  - 1 for on-die PDN modeling (BIRD198)
- EBD update supporting IBIS-ISS and Touchstone
  - Improved module and multi-chip package modeling
- BIRD200 approved: C_comp model supporting IBIS-ISS and Touchstone
- BIRD195.1 approved: [Rgnd] and [Rpower] for IBIS-AMI Input models
- What other new ideas do you have for IBIS?

What Else Could IBIS Be Used For?

- IBIS is nominally about I/O buffers, used to:
  - Solve signal quality problems like loss, inter-symbol interference (ISI) and crosstalk
  - Generate waveforms used in timing analysis
- But engineers also:
  - Insure proper timing between pins
  - Insure sufficient power distribution
  - Include optical links in analyses
  - Analyze channel operating margin (COM), forward error correction (FEC), etc.
  - Comply with any other new requirements posed by JEDEC, etc.
- What other data might IBIS formats convey?

New Directions for IBIS?

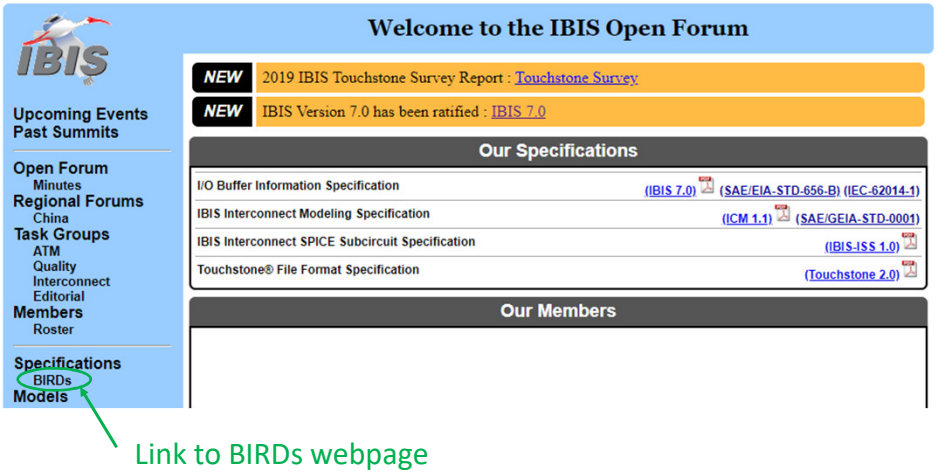


- IBIS VRM models
- IBIS chip power models
- IBIS timing models
- IBIS waveform analysis language
- Data probability distributions (or at least more than 3 corners)
- IBIS-ISS [Test Load], external [Test Data]
- Optical Model_type(s) for Vertical Cavity Surface Emitting Laser (VCSEL), etc.

Submitting Your Idea – BIRD Process

- BIRD – Buffer Issue Resolution Document
  - Official method for submitting a proposed change to the IBIS specification
- BIRD Template found on IBIS website
  - Standardized method to describe your idea
- Submit BIRD to chair@ibis.org
- BIRDs discussed in Open Forum meetings
  - Eventual vote by members for approval
- Idea not ready for an official BIRD?
  - Join an IBIS Task Group meeting for technical discussion

BIRD Link on IBIS Website



BIRD Template Link on the BIRD Webpage

Buffer Issue Resolution Documents (BIRD)

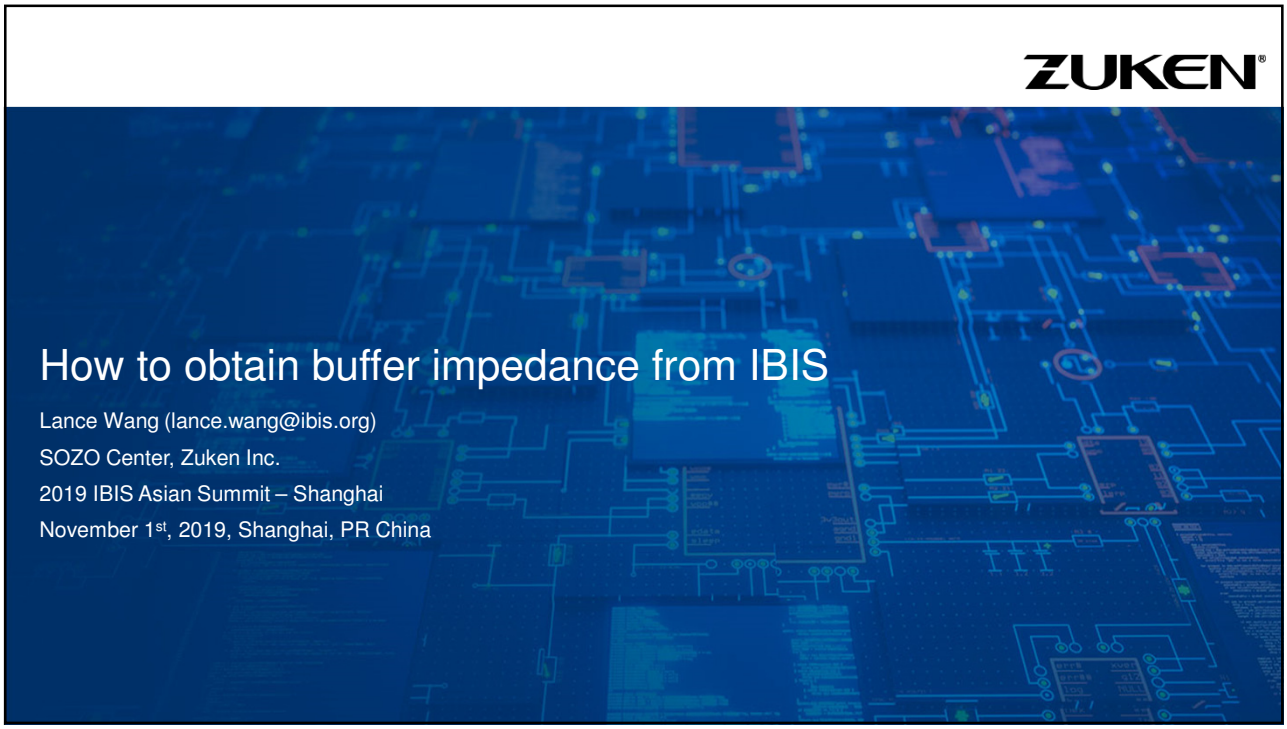
To submit a BIRD to the IBIS Open Forum, please use the BIRD Template, Rev. 1.3

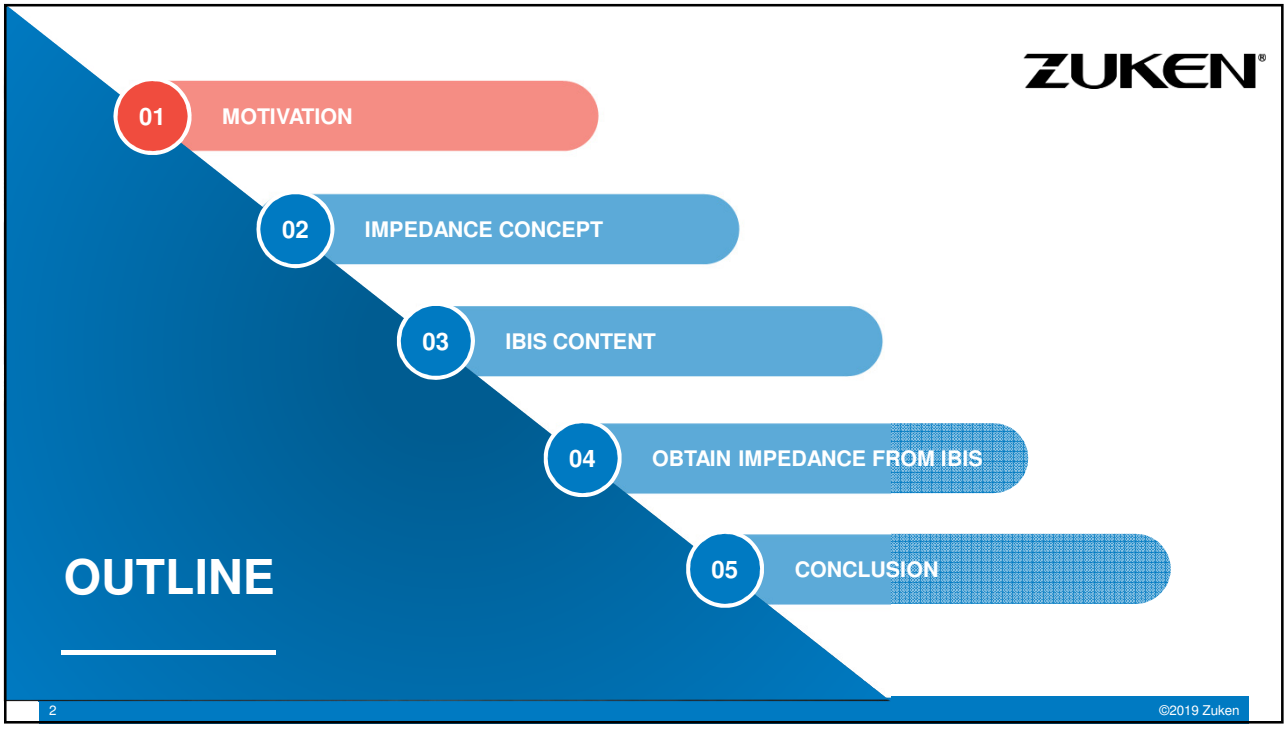
ID#	Issue Title	Requester	Date Submitted	Date Accepted	Supporting Version
200	C_comp Model Using IBIS-ISS or Touchstone	Randy Wolff, Micron Technology, Inc. Walter Katz, Signal Integrity Software, Inc.	July 9, 2019	September 27, 2019	
199	Fix Rx_Receiver_Sensitivity Inconsistencies	Arpad Muranyi, Mentor a Siemens Business	March 19, 2019	June 7, 2019	
198	Keyword additions for On Die PDN (Power Distribution Network) Modeling	Kazuki Murata; Ricoh Co., Ltd.; Miyoko Goto; Ricoh Co., Ltd.; Kazuyuki Sakata; Renesas Electronics Corporation; Kazunori Yamada; Renesas Electronics Corporation; Kouji Ichikawa; Denso Corporation; Atsushi Tomishima; Toshiba Electronic Devices & Storage Corporation; Takashi Hasegawa; Sony LSI Design Inc.; Koichi Seko, Panasonic Industrial Devices Systems and Technology Co., Ltd.; Toshiki Kanamoto; Hirosaki University Megumi Ono; Socionext Inc.	March 11, 2019		
197.4	New AMI Reserved Parameters DC_Offset and NRZ_Threshold	Walter Katz, SiSoft, Ambrish Varma, Cadence Design Systems, Randy Wolff, Micron Technology, Justin Butterfield, Micron Technology, Fangyi Rao, Keysight Technologies	November 27, 2018, December 4, 2018, January 15, 2019, June 25, 2019, July 23, 2019		
196.1	Prohibit Periods at the End of File Names	Arpad Muranyi, Mentor Graphics, A Siemens Business	September 25, 2018, October 12, 2018	October 12, 2018	7.0
195.1	Enabling [Rgnd] and [Rpower] Keywords for Input Models	Michael Mirmak, Intel Corp.	June 19, 2018, June 29, 2018	August 31, 2018	

[Thank You]

IBIS Open Forum:
Web: http://www.ibis.org
Email: ibis-info@freelists.org

We welcome participation by all IBIS model makers, EDA tool vendors, IBIS model users, and interested parties.


ZUKEN
How to obtain buffer impedance from IBIS
Lance Wang (lance.wang@ibis.org)
SOZO Center, Zuken Inc.
2019 IBIS Asian Summit – Shanghai
November 1st, 2019, Shanghai, PR China


ZUKEN
01 MOTIVATION
02 IMPEDANCE CONCEPT
03 IBIS CONTENT
04 OBTAIN IMPEDANCE FROM IBIS
05 CONCLUSION
OUTLINE
2
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Motivation

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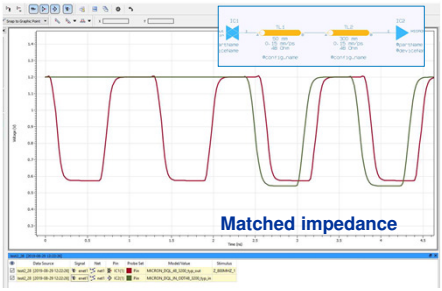
- Impedance matching is the biggest task for Signal Integrity engineer and high-speed PCB/PKG designers.
  - Unmatched impedance may cause unpredictable reflection that reduces the signal quality for high-speed circuit design.
- Interconnects, such as, trace, via, connector, package, etc., are under our radar already.
  - Field Solver helps
- Interconnect impedance also needs to match buffer Output/Input impedance in order to keep good signal quality **How to obtain I/O buffer impedance?**



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OUTLINE

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Impedance Concept

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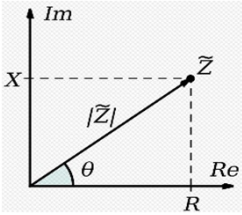
- The impedance of a two-terminal circuit element is represented as a complex quantity Z. The polar form conveniently captures both magnitude and phase characteristics as $Z = |Z|e^{j\,arg(Z)}$
- where the magnitude $|Z|$ represents the ratio of the voltage difference amplitude to the current amplitude, while the argument $arg(Z)$ (commonly given the symbol θ gives the phase difference between voltage and current). j is the imaginary unit and is used instead of i in this context to avoid confusion with the symbol for electric current.
- In Cartesian form, impedance is defined as $Z = R + jX$
- where the real part of impedance is the resistance R and the imaginary part is the reactance X.



For a high-speed I/O buffer, the buffer inductance and capacitance are specially designed. It is close to minimum for the reactance X. So, in this case, the resistance R is the main factor for impedance matching.

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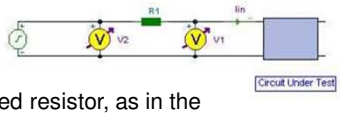
Measuring Impedance – Input Impedance

ZUKEN

- From the AC impedance triangle, the input or output impedance of a two terminal network can be determined by measuring the small signal AC currents and voltages.
  - The voltage is measured across the input terminals and the current measured by inserting the meter in series with the signal generator.



  - An easy way to measure small input currents, is to use a fixed resistor, as in the diagram above. Measure the AC voltage at points V1 and V2, then the input current, I_{in} becomes:

$$I_{in} = \frac{V_2 - V_1}{R_1}$$

  - The input impedance Z_{in} of the circuit under test is then found by:

$$Z_{in} = \frac{V_1}{I_{in}}$$

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Measuring Impedance – Output Impedance

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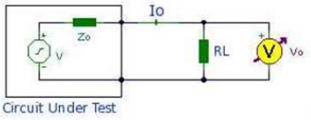
- Output impedance may also be determined using a similar technique. A fixed load resistor is used, and the output voltage is measured first with full load, then without the load.



- Z_0 is the internal output impedance of the network to be measured.
- To find the output impedance the output voltage is measured first with no load resistor, then with a fixed load (purely resistive).
- First, the load resistor R_L is removed and output voltage (V) measured and recorded. Then R_L is placed back in circuit and the output voltage under load (V_L). The output impedance, Z_0 is now found by Ohm's Law for AC circuits. As the load is purely resistive $Z=V/I$, where *"V"* is voltage drop across the output impedance: (V - V_L), and *"I"* the output current, V_L/R_L. Thus:

$$Z_0 = \frac{(V - V_L)}{V_L/R_L} = \frac{R_L(V - V_L)}{V_L}$$

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OUTLINE

01 MOTIVATION

02 IMPEDANCE CONCEPT

03 IBIS CONTENT

04 OBTAIN IMPEDANCE FROM IBIS

05 CONCLUSION

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IBIS model contents

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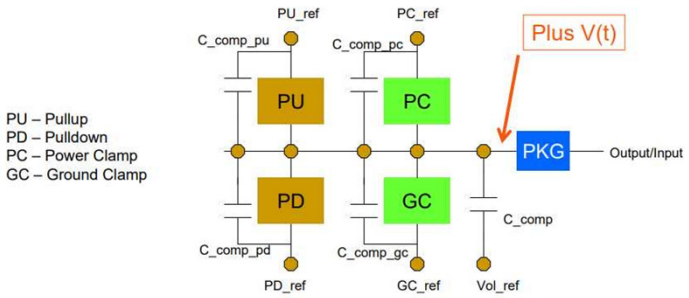
IBIS Buffer Structure



All curve data are independent with own voltage references

- I/O type
  - 4 static curve data sets
    - Pullup
    - Pulldown
    - Power Clamp
    - Ground Clamp
- Output type
  - 2 static curve data sets
    - Pullup
    - Pulldown
- Input type
  - 2 static curve data sets
    - Power Clamp
    - Ground Clamp

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IBIS model contents

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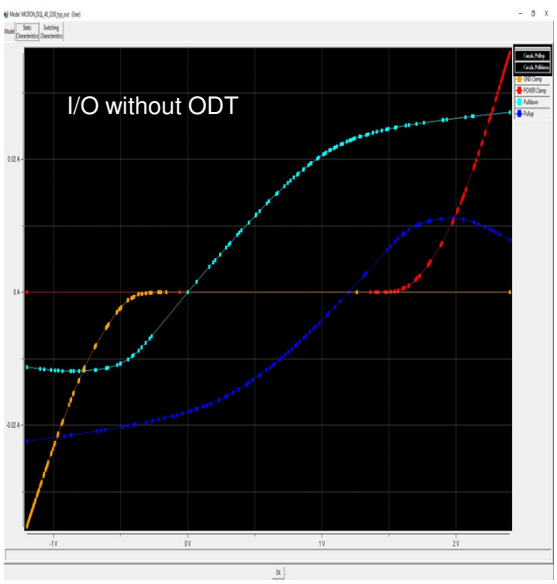

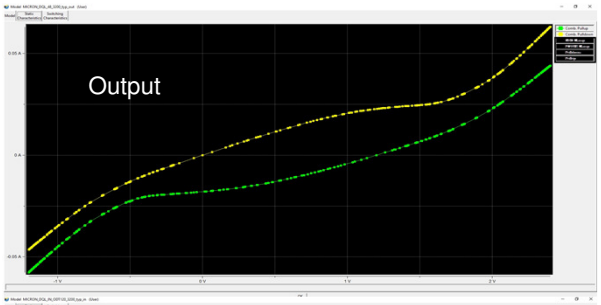

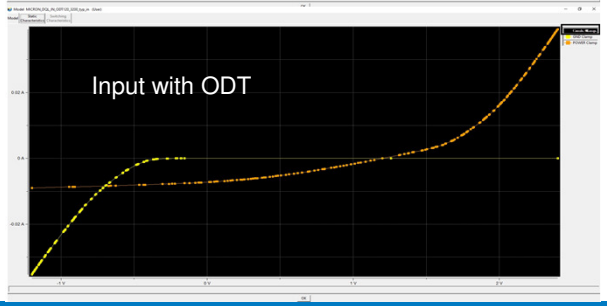

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IBIS model contents

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IBIS MODELING COOKBOOK
For IBIS Version 4.0

Prepared By:
The IBIS Open Forum

Approved September 15, 2005

Senior Editor:
Michael Mirmak, Intel Corporation

Contributors:
John Angulo, Mentor Graphics Corporation
Ian Dodd, Mentor Graphics Corporation
Lynne Green, Green Streak Programs
Syed Huq, Cisco Systems
Arpad Muranyi, Intel Corporation
Bob Ross, Teraspeed Consulting Group

From an original by Stephen Peters published 1997

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3.1 Extracting I-V Data from Simulations

The first step to extracting the required I-V tables is understanding the buffer's operation. Analyze the buffer schematic and determine how to put the buffer's output into a logic low, logic high and (if applicable) high impedance (3-state) state. As mentioned above, the schematic should include any ESD or protection diodes. Also, understand the buffer's power supply voltage reference ("Vcc") requirements and connections. The schematic should also indicate if the power clamp and/or ground clamp diode structures are tied to voltage rails (voltage references) different from those used by the pullup and/or pulldown transistors.

3.1.1 Simulation Setup

A typical I-V table simulation setup for an output or I/O buffer is shown in Figure 3.1 below. For this example, the buffer being analyzed is a standard 3-state buffer with a single push-pull output stage. The buffer uses electrostatic discharge protection devices in addition to its parasitic driver diodes. The buffer's clamp supplies are assumed identical to its driver supply (Vcc hereinafter).

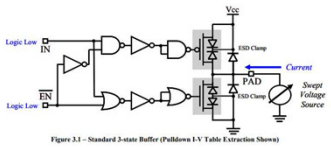

Figure 3.1 – Standard 3-state Buffer (Pulldown I-V Table Extraction Shown)

All measurements are made at the output node (pad) as shown above. Remove all package lead (R_pin, L_pin, and C_pin) parasitics. However, any series resistances present between the pad and the pullup/pulldown transistors should be included (these are not shown in Figure 3.1).

The output buffer is connected to an independent voltage source. Set the buffer's input(s) so that the desired output state (low, high, off) is obtained, then using a DC or "transfer function" analysis sweep the voltage source over the sweep range -Vcc to 2*Vcc while recording the current into the buffer. An alternative method is to perform a "transient analysis". The voltage source in this case should be linear ramp function driving the output node, slow enough that the current measurement at each time point is effectively DC, without reactive aspects of the design affecting the result. The current flow into the pad is measured (by IBIS convention, current flow into the die pad is positive), as is the voltage at the node with respect to a reference, then the resulting I-T and V-T data is combined into a single I-V table. Note that a transient function analysis may require post-simulation data manipulation.

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OUTLINE

01 MOTIVATION

02 IMPEDANCE CONCEPT

03 IBIS CONTENT

04 OBTAIN IMPEDANCE FROM IBIS

05 CONCLUSION

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Obtain impedance from IBIS curves

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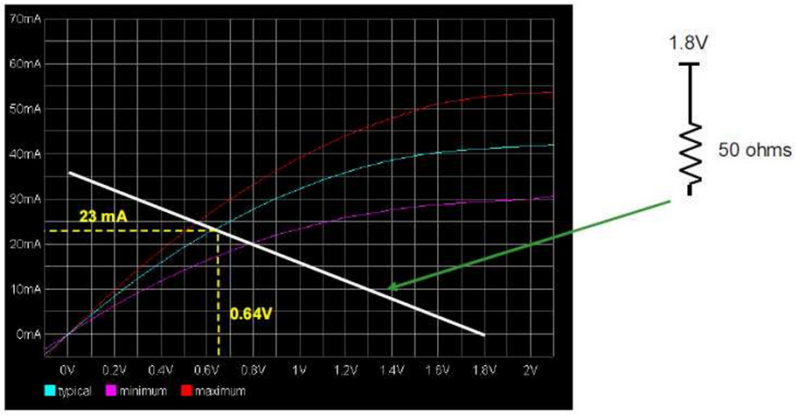

Picture from Todd W. 2005 DAC IBIS Summit

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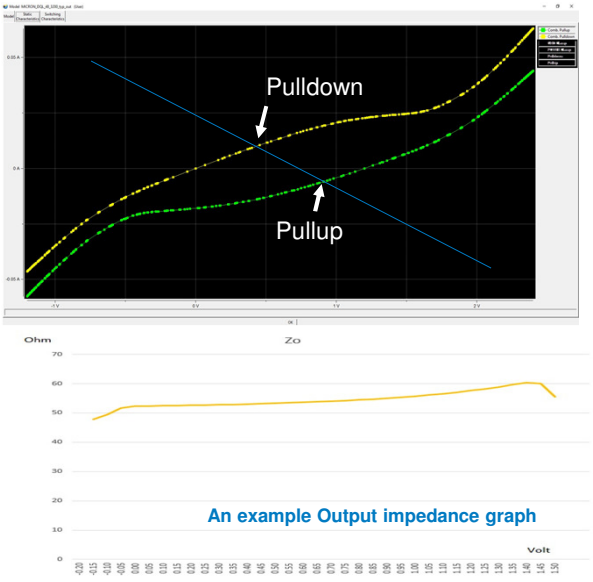
Obtain Output type buffer impedance from IBIS

ZUKEN

- Need to use Combined Pullup/Pulldown curves
  - Pullup + Clamps
  - Pulldown + Clamps
- Load line / Crossing Point
- To avoid numerical errors

$$Z_0 = \frac{dV}{dI} \text{ @ } R_L$$



An example Output impedance graph

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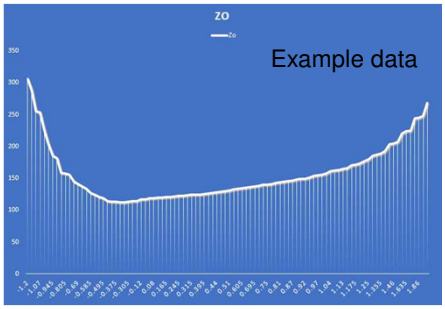
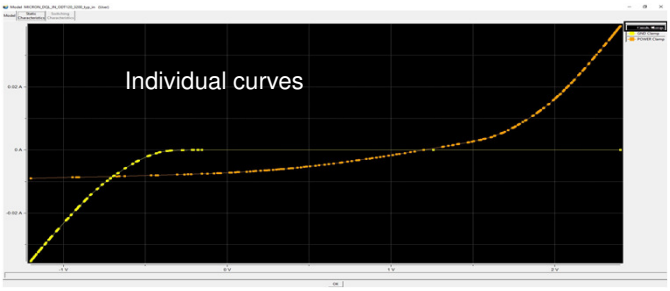
Obtain Input type buffer impedance from IBIS

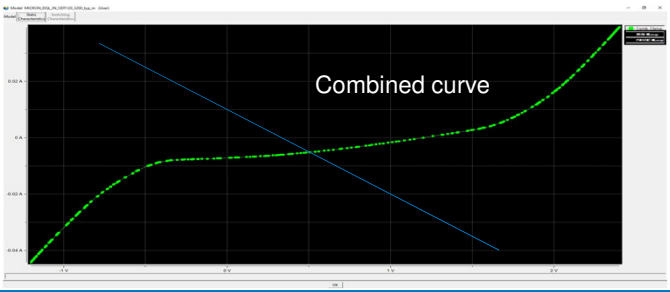
ZUKEN

- Use the Combined Clamp data
- To avoid numerical errors

$$Z_0 = \frac{dV}{dI} @ R_L$$







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01 MOTIVATION

02 IMPEDANCE CONCEPT

03 IBIS CONTENT

04 OBTAIN IMPEDANCE FROM IBIS

05 CONCLUSION

OUTLINE

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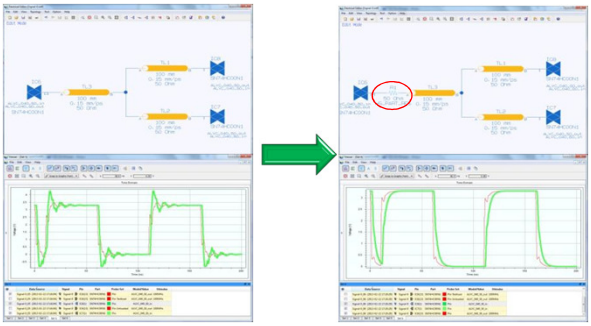
Conclusion

ZUKEN

- Impedance matching is important for high-speed design
  - Not only for interconnect impedance, but also I/O buffer impedance should be counted in the big picture
- The I/O buffer impedance can be obtained from IBIS curve data
  - Obtain buffer driving impedance from IBIS combined Pullup/Pulldown curve data
  - Obtain buffer Input impedance from IBIS combined Power /Ground Clamps curve data
- I/O impedance maybe vary for different loads



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C-PHY SI SIMULATION WITH IBIS MODEL

Bailing Zhang 张百玲
ANSYS

Asian IBIS Summit
Shanghai, PRC
November 1, 2019

1

Outline

- C-PHY interface instruction
- How to use IBIS model to do the C-PHY SI simulation
- Check the simulation result
- Summary

2

C-PHY interface instruction

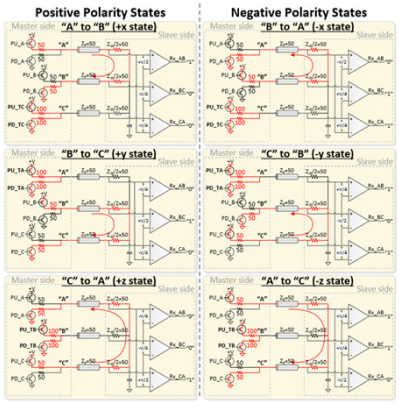


Figure 1 Six Physical Layer Wire States of C-PHY Encoding, Nominal Values Shown

The MIPI C-PHY uses a 3-phase symbol. Each symbol provides 2.28 bits, and transmits data on a 3-wire path with 3-state signals. Each 3-state symbol includes an embedded clock. C-PHY signals are single ended, and each has 3 levels. They are represented by lineA, lineB, and lineC. At any given timing point, no two signals will be at the same voltage level. The receiver uses differential sensing to produce four voltage levels: strong 1, weak 1, strong 0, and weak 0. However, the output of the receiver is logical 1 or logical 0.

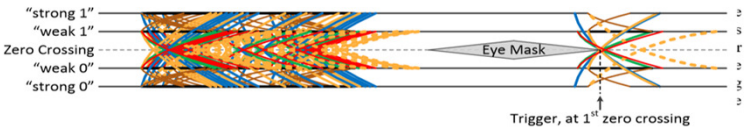
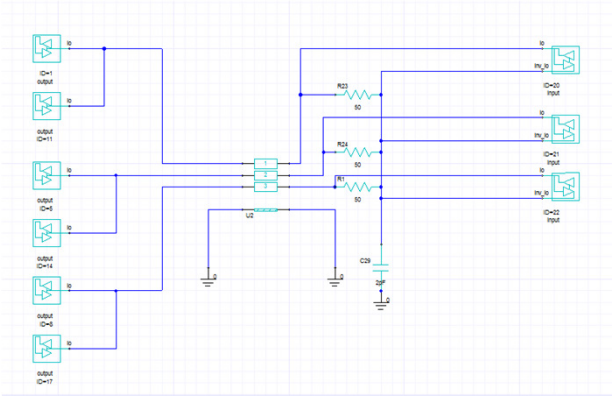


Figure 58 C-PHY Eye Pattern Example, Triggered Eye

3

How to use IBIS model do the C-PHY SI simulation



MIPI C-PHY using IBIS I/O drivers and differential receivers

4

Check the simulation result

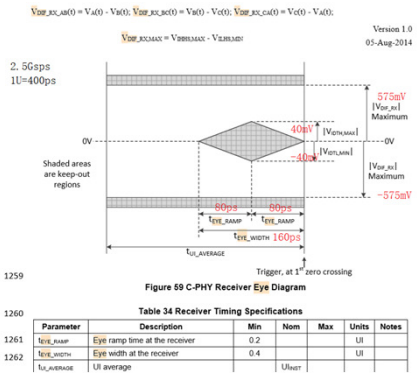
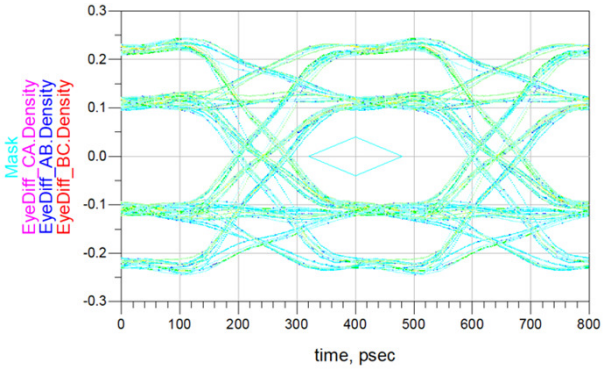


Figure 69 C-PHY Receiver Eye Diagram

Table 34 Receiver Timing Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
t_{EYE_RAMP}	Eye ramp time at the receiver	0.2			UI	
t_{EYE_WIDTH}	Eye width at the receiver	0.4			UI	
$t_{UI\_AVERAGE}$	UI average		UI_{INST}			



5

Summary

Use IBIS model to do the C-PHY SI simulation is very convenient, accurate and fast.

From the simulation we can best evaluate the quality of C-PHY signal and make the product successful.

6

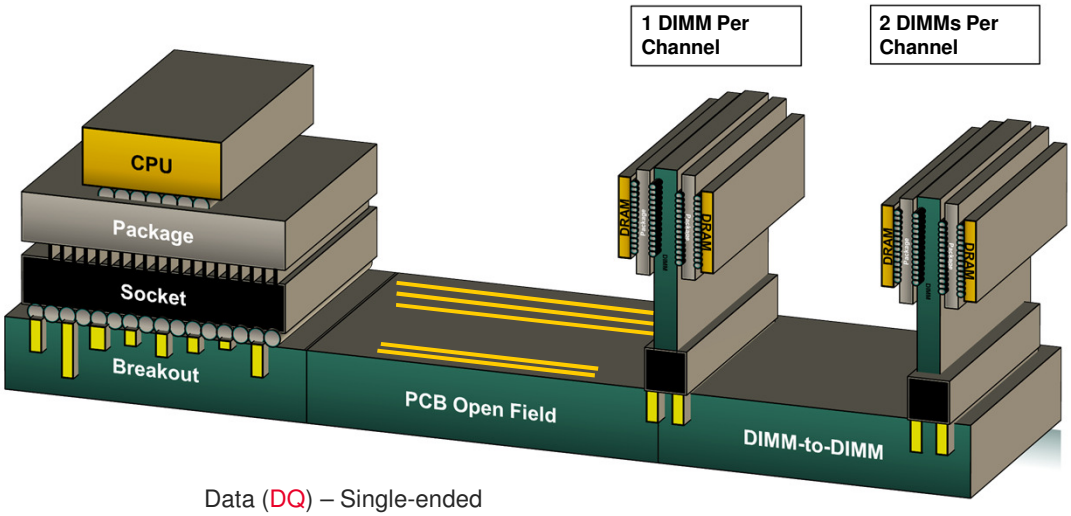
Thank you

Innovations in DDR Memory Simulation

Stephen Slater | NOVEMBER 1, 2019
Asian IBIS Summit, Shanghai, PRC

KEYSIGHT TECHNOLOGIES

A Typical DDR5 Application



Data (DQ) – Single-ended
Data Strobe (DQS) – Differential
Microstrip & Stripline

KEYSIGHT TECHNOLOGIES

2

What Does it Mean to Succeed?

THE MEASURE OF SUCCESS FOR A PRODUCT WITH DDR5

- No system failures, under stress
  - At Max and Min temperatures
  - Using multiple vendors' DIMMs
  - 1 DIMM slot and 2 DIMM slots filled
  - Running diagnostic software that stresses the memory access
  - Graceful performance degradation

"I can stop testing when I'm certain my manager is satisfied with the product quality risk"

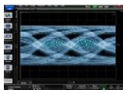
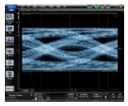
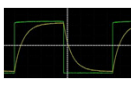
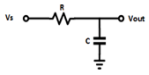
Source: Burn-in environment test chambers by EDA-Industries S.p.a

KEYSIGHT TECHNOLOGIES

3

How Did we Get to DDR5?

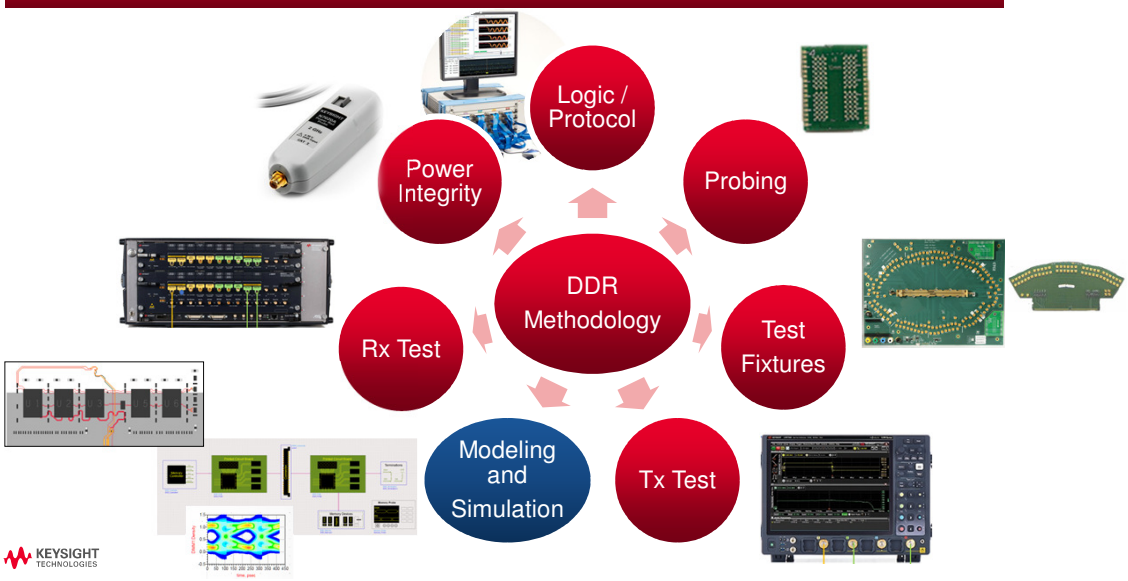
A ROAD PAVED BY INNOVATION

Signal	MT/s	Generation	Characteristics	Specification	Introduction
	4200 – 8000+	DDR5+	"Hyper Speed" • Eye collapses • Impulse response • BER Rj/Dj, Rn/Dn		2019
	1600 – 4200	DDR4	"Serial Speed" • Eye Diagrams • Rx Masks • Bit error rates		2014
	200 – 1600	DDR/2/3	"High Speed Digital" • Transmission lines • Ts / Th, Skew		2002
	33 – 133	SDRAM	"Low Speed" • Fanout • Capacitance		1961

KEYSIGHT TECHNOLOGIES

Ensuring First Pass Success - One Layer Deeper

ENSURING THE SYSTEM IS PERFORMANT AND RELIABLE



KEYSIGHT TECHNOLOGIES

5

Change, Challenges and Solutions

1. Crosstalk, Jitter and Bit-Error-Rate (BER) Specs
2. Closed eyes need equalization and training
3. Innovations in Simulation and Modeling of DDR5 & LPDDR5 systems

KEYSIGHT TECHNOLOGIES

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1. Crosstalk, Jitter and Bit-Error-Rate (BER) Specs

KEYSIGHT TECHNOLOGIES

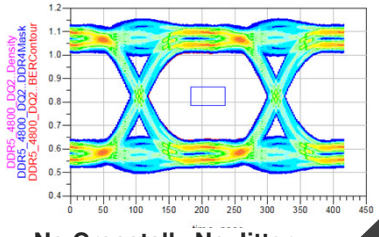
7

Electromagnetic (EM) Simulation

Crosstalk

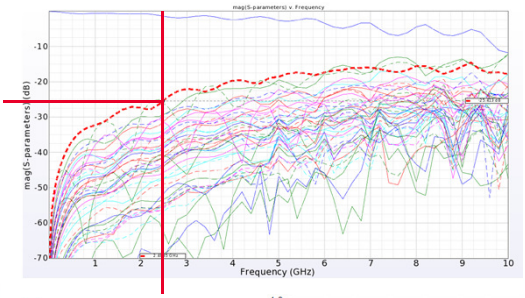
THE IMPORTANCE OF THE SIGNAL RETURN PATH

DDR5-4800



No Crosstalk, No Jitter –
Just ISI from Channel

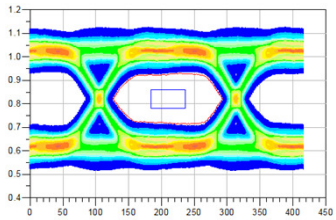
< -25dB



Nyquist

Signal Return Path –
through shared Ground
Pin

PCB Trace Routing of Victim +
Worst Aggressors



With Crosstalk

KEYSIGHT TECHNOLOGIES

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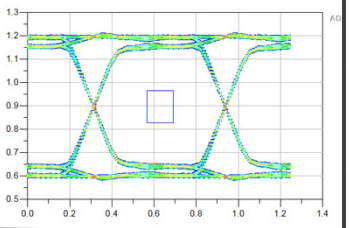
Jitter

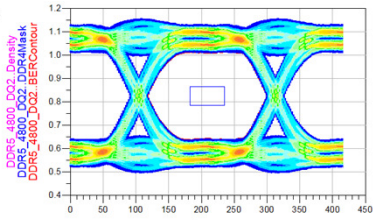
Jitter injected at Tx, and eye measured at the DRAM Solder-Ball (Rx Input)

BER CONTOUR AT 1E-16 TELLS US THE REAL MARGIN

DDR4-1600 | DDR5-4800

No Jitter – Just ISI from Channel



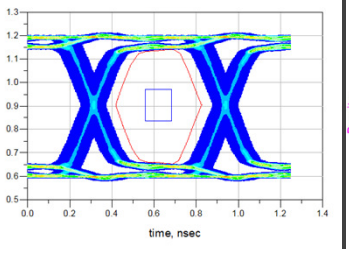


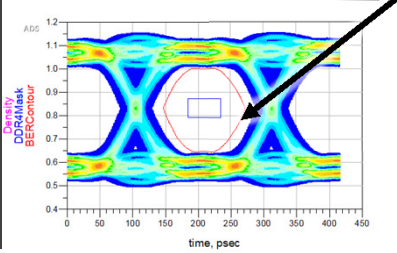
No Jitter – More ISI from Channel due to higher speed

47% Reduction in Timing Margin

(27ps less margin to mask)

Random Jitter = 0.02 UI Applied at Tx (2%)





KEYSIGHT TECHNOLOGIES

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Specs Becoming More Bit-Error-Rate Focused

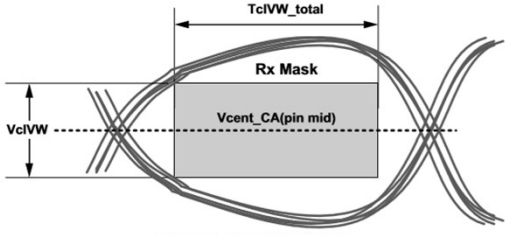

Figure 179 — CA Receiver (Rx) mask

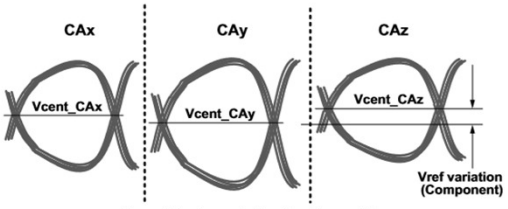

Figure 180 — Across pin V_{REF}CA voltage variation

- From the draft spec:
  - Maximum Jitter (Dj, Rj and DCD) specifications for Tx and Rx components
  - For Tx and Rx Voltage and Timing tests, system BER is e-16 and requires 5.3e9 minimum UIs for validation (99.5% confidence level)
  - New receiver stressed-eye tests for components and DIMMs

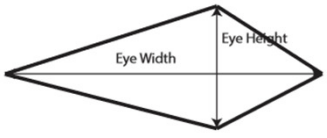

Figure 196 — Example of Rx Stressed Eye Height and Eye Width

Stressed Eye is calibrated to a specified height and width. The DIMM, DRAM or Memory Controller Rx must be able to receive to the system BER

KEYSIGHT TECHNOLOGIES

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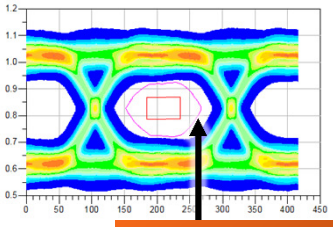
Crosstalk, Jitter & BER Specs

KEY INSIGHTS

- Jitter and Crosstalk are Very Significant
- Simulation must predict Eye closure due to Random Jitter down to the system BER (1e-16) in a practical time
- EM simulation must capture Crosstalk accurately

DDR5-4800

Jitter, crosstalk & Channel ISI



64% Reduction in Voltage Margin

63% Reduction in Timing Margin

KEYSIGHT TECHNOLOGIES

2. Equalization and Training

KEYSIGHT TECHNOLOGIES

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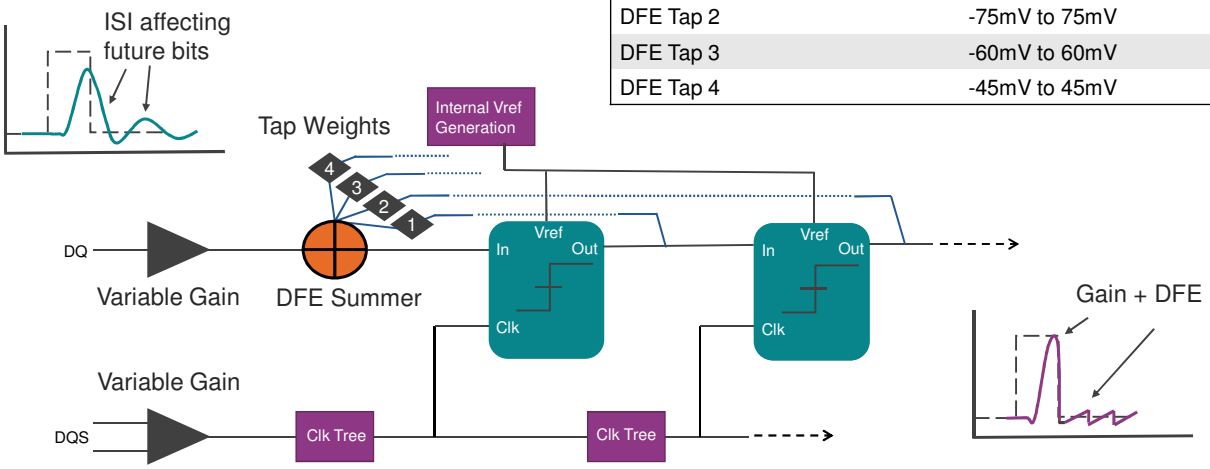
Rx Equalization

FIRST TIME TO HAVE DFE ON DRAM!

Mode Register Settings (per DQ)	*All values subject to change*
Variable Gain	-6dB to 6dB
VrefDQ	-3 to +3 Offset steps
DFE Tap 1	-200mV to 50mV
DFE Tap 2	-75mV to 75mV
DFE Tap 3	-60mV to 60mV
DFE Tap 4	-45mV to 45mV



KEYSIGHT TECHNOLOGIES

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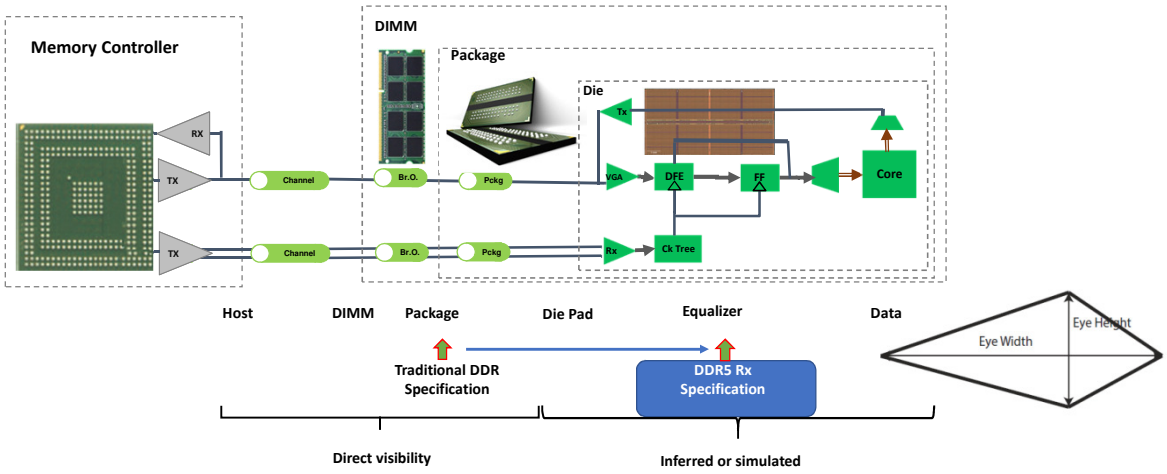
DDR5 Rx Specifications are Inside the Die



KEYSIGHT TECHNOLOGIES

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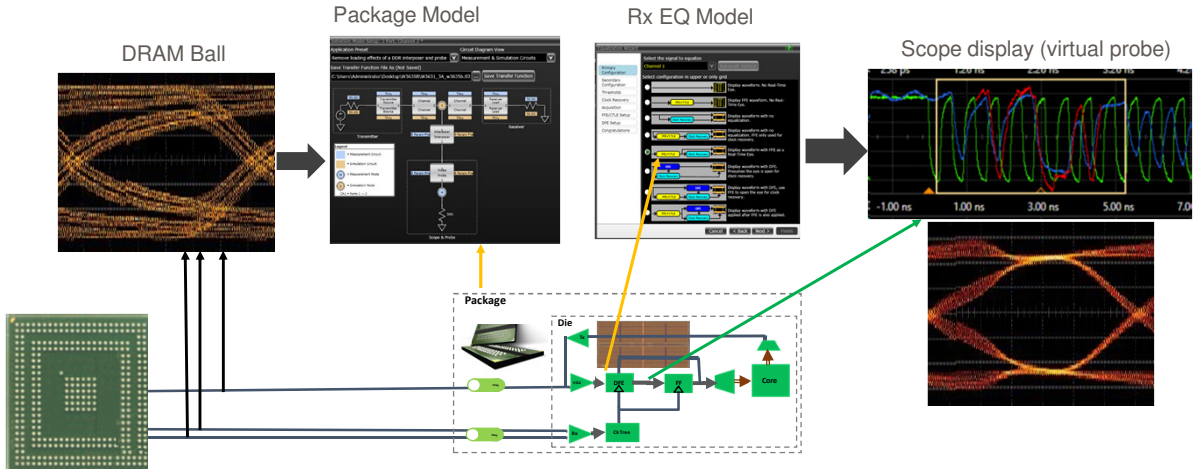
DDR5 Tx Test: New Methodology Needed

VIRTUAL PROBING INSIDE THE DIE



KEYSIGHT TECHNOLOGIES

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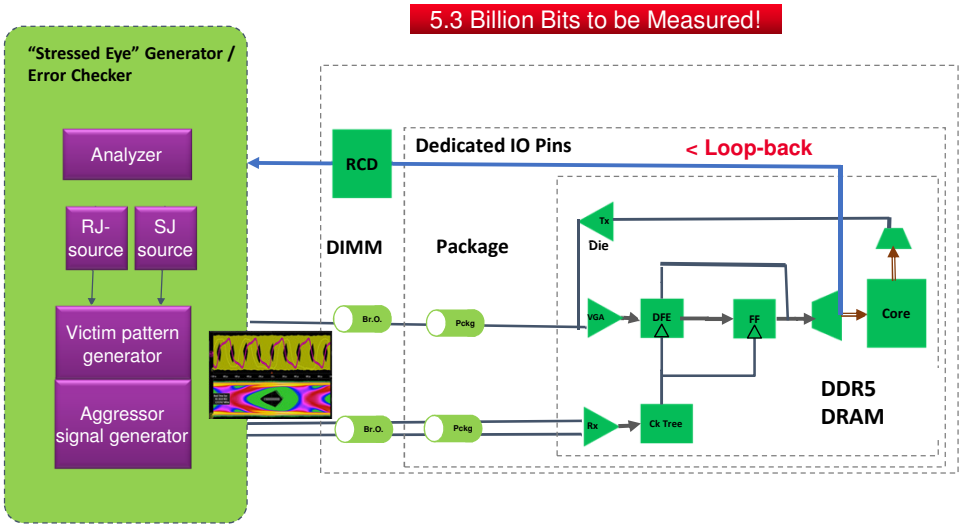
DDR5 Rx Test: New DRAM Feature - Loop-Back Mode

5.3 Billion Bits to be Measured!



KEYSIGHT TECHNOLOGIES

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Skew Adjustment with Write-Leveling

- Due to the fly-by topology of the clock for DDR4 & DDR5, the Clock (Clk) is inevitably skewed to the DQS at each of the independent DRAM

- The controller has ability to adjust skew between DQ's, DQS and the Clock signal.
- DQS is adjusted to match the Clk first, then internal alignment of each DQ is performed (via mode register) to remove DQ-to-DQS skew (due to the package and die)

KEYSIGHT TECHNOLOGIES

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Equalization and Training

KEY INSIGHTS

- **Possible to have a Closed eye at input to Rx**
- **Optimal Eye opening depends on:**
  - **Vref setting (per DQ)**
  - **Gain Setting (per DQ)**
  - **DFE Tap settings (4 taps per DQ)**
  - **Timing of DQS to DQ**
  - **Write-leveling (skew adjustment)**

KEYSIGHT TECHNOLOGIES

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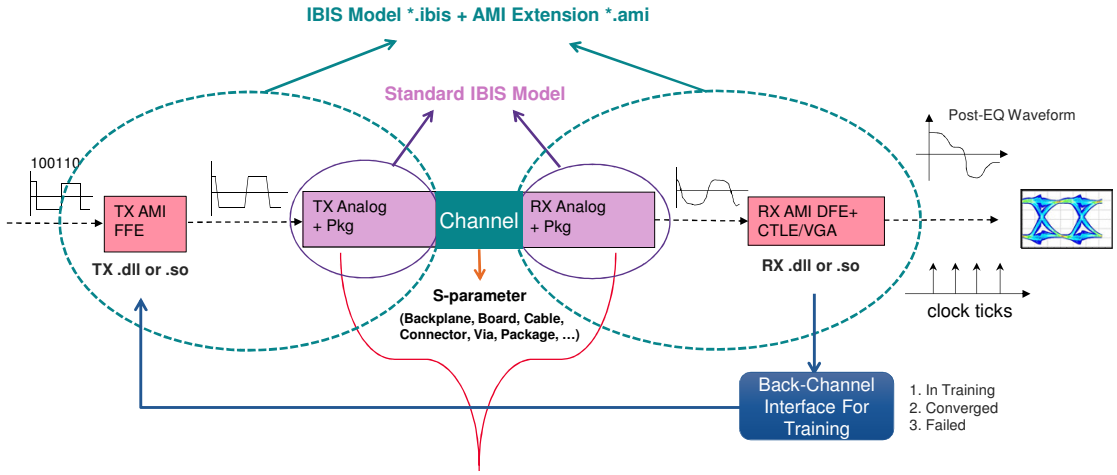
3. Innovations in Simulation and Modeling of DDR5 & LPDDR5 systems

Introducing IBIS AMI for DDR Signals

- EQ Necessary for TX: 3 Tap Pre-Emphasis (Feed Forward Equalization)
- EQ Necessary for RX: CTLE/VGA/DFE
- IBIS-AMI offers
  - Portability – One IBIS-AMI mode can run on many EDA tools
  - IP Protection – Digital signal processing behavior is concealed in model DLL/shared object
  - Interoperability - IC Vendor A←→IC Vendor B (AMI defines a common interface between the vendor model and the EDA channel simulator)
  - Non-linearity – As complex as the model vendor wishes the model to be
  - Performance – Ultra low BER simulations in seconds not days over the traditional SPICE simulation
- AMI has been widely adopted by IC, system and EDA companies for SerDes signals but this is the first application to DDR single-ended signals.

How Does Standard IBIS-AMI Work?

CHANNEL SIMULATION



Impulse response of a Linear Time Invariant Network

KEYSIGHT TECHNOLOGIES

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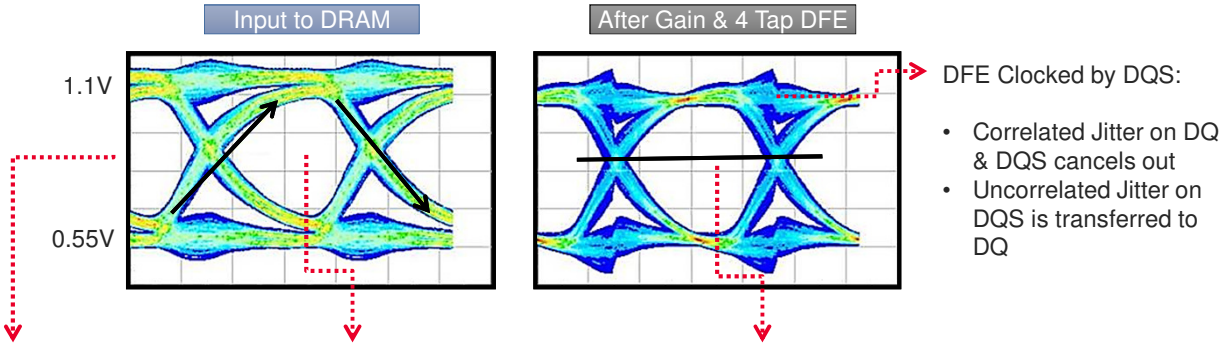
What Do We Need for DDR5 AMI To Work?

SUPPORTING PARALLEL, SINGLE-ENDED SIGNALS WITH EXTERNAL CLOCKS



DFE Clocked by DQS:

- Correlated Jitter on DQ & DQS cancels out
- Uncorrelated Jitter on DQS is transferred to DQ

Single-Ended Signal can have a DC Offset

Asymmetric Eye: Rise Time ≠ Fall Time

Asymmetric Eye: Crossing Points are shifted in the Equalized Eye

KEYSIGHT TECHNOLOGIES

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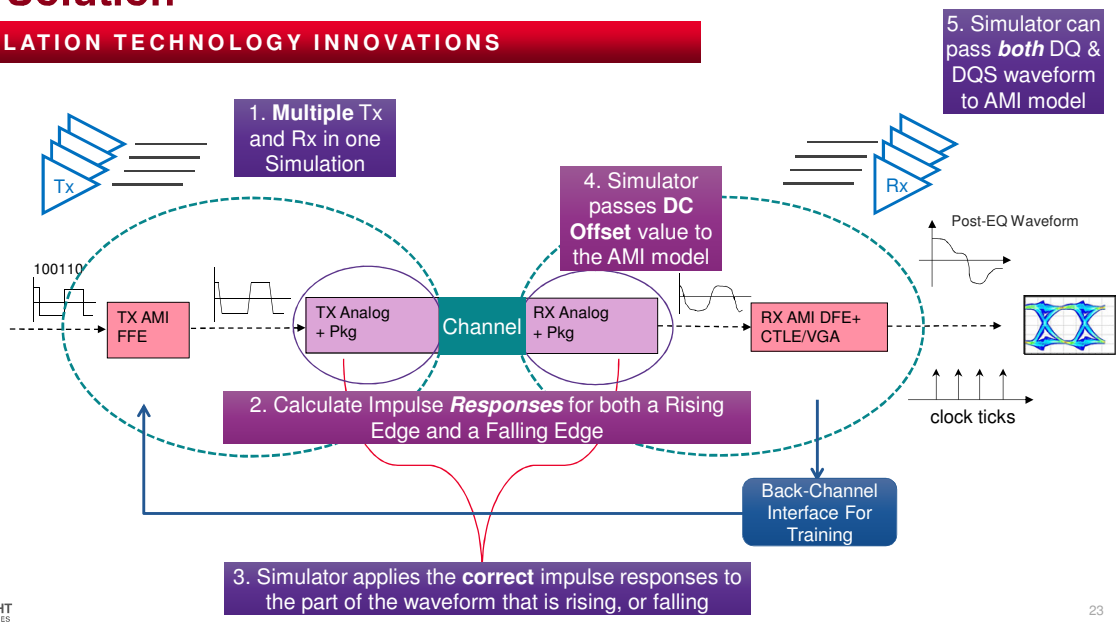
The Solution

SIMULATION TECHNOLOGY INNOVATIONS



KEYSIGHT TECHNOLOGIES

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KEYSIGHT TECHNOLOGIES

IBIS-AMI & COM Co-design for 25G Serdes

Asian IBIS Summit
Shanghai, PRC
November 1, 2019

Nan Hou, Amy Zhang, Guohua Wang, David Zhang, Anders Ekholm

AGENDA

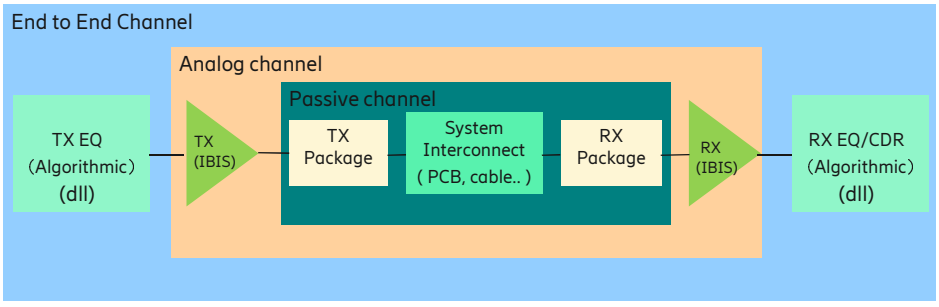
- Traditional IBIS-AMI
- COM Overview
- IBIS-AMI Co-design with COM for 25G
- Two example channels
- Co-simulation Conclusion
- Next Steps

AGENDA

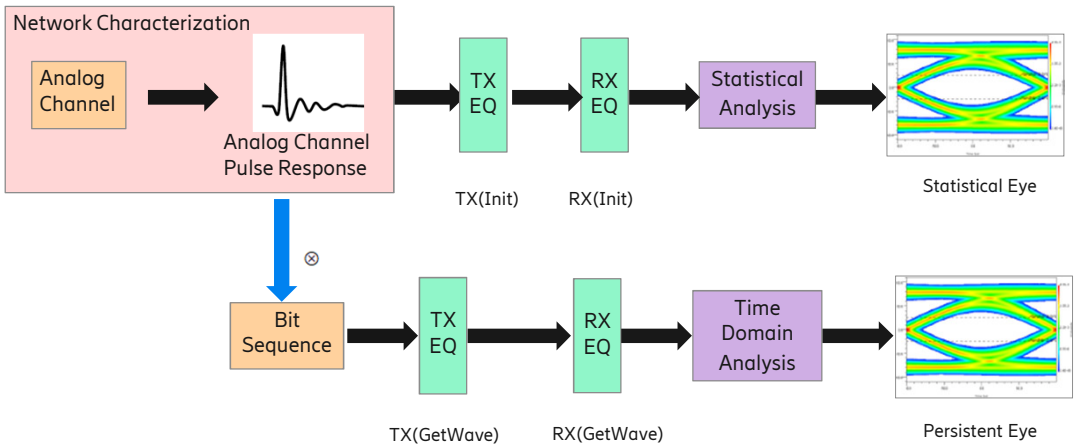
- Traditional IBIS-AMI
- COM Overview
- IBIS-AMI Co-design with COM for 25G
- Two example channels
- Co-simulation Conclusion
- Next Steps

IBIS-AMI OVERVIEW

- IBIS is Input/output Buffer Information Specification
- AMI stands for Algorithmic Modeling Interface
- Analog model: drive strength/amplitude, rise/fall time, impedance
- Algorithmic model: Equalizer (CTLE, FFE, DFE) , clock data recovery



IBIS-AMI FLOW



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AGENDA

- Traditional IBIS-AMI
- COM Overview
- IBIS-AMI Co-design with COM for 25G
- Two example channels
- Co-simulation Conclusion
- Next Steps

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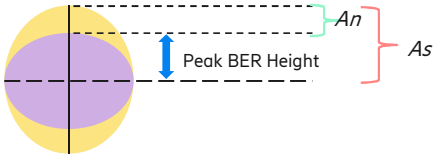
COM OVERVIEW

The Channel Operating Margin (COM) is a figure of merit for a channel derived from a measurement of its scattering parameters
COM is related to the ratio of a calculated signal amplitude to a calculated noise amplitude as defined by Equation

$$COM = 20 \times log10(As/An)$$



Where *As* is the signal amplitude, *An* is the noise amplitude
COM has been adapted by various standards:

- IEEE 802.3
- OIF CEI
- JEDEC 204C

An (Peak BER Noise) = *As* - Peak BER Height

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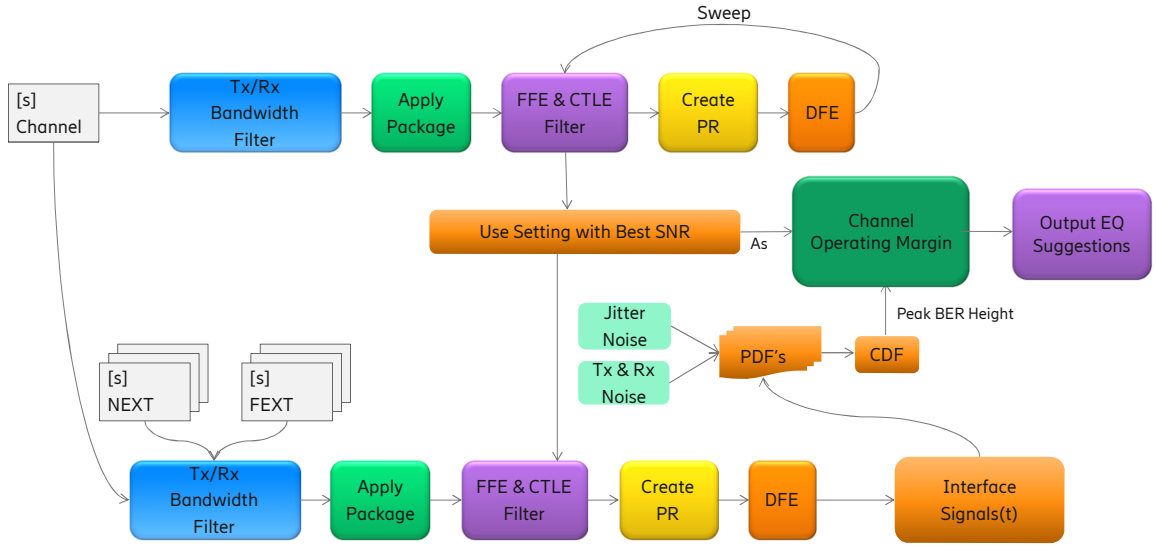
COM FLOW



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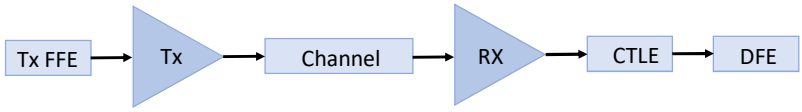
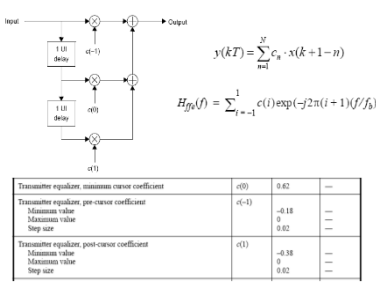
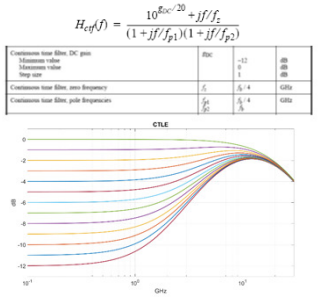
COM CHANNEL TRANSFER FUNCTION



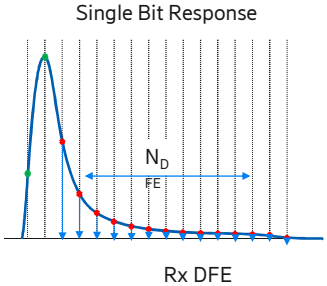
$$H(f) = H_{Tx}(f) \times H_{TxFFE}(f) \times H_{ch}(f) \times H_{Rx}(f) \times H_{RxCTLE}(f)$$



Tx FFE



Rx CTLE



Rx DFE

COM OPTIMAL EQ SETTINGS

- COM is a figure of merit (FOM), which calculates the ratio of peak signal level to the peak noise level at the receiver sampling latch, comprehending device Tx characteristics (i.e., driver filter, FFE filter, package S-parameters), channel characteristics (i.e., S-parameters) and receiver characteristics (i.e., Rx filter, CTLE filter, package S-parameters and DFE)
- Determine optimal equalization settings
  - An exhaustive search for the best SNR used as a FOM for finding the best FFE and CTLE setting
  - FFE and CTLE are optimized jointly
  - The DFE is only used to gate the SBR

$$FOM = 10log_{10}\left(\frac{A_S^2}{\sigma_{TX}^2 + \sigma_{ISI}^2 + \sigma_J^2 + \sigma_{XT}^2 + \sigma_N^2}\right)$$

A_S – peak signal amplitude
σ_{TX} - transmitter noise
σ_{ISI} - residual ISI
σ_J – jitter contribution to amplitude noise
σ_{XT} – peak crosstalk
σ_N – spectral noise at the ouput of CTLE

AGENDA

- Traditional IBIS-AMI
- COM Overview
- IBIS-AMI Co-design with COM for 25G
- Two example channels
- Co-simulation Conclusion
- Next Steps

IBIS-AMI COMBINE WITH COM

- Can we use COM to evaluate the channel margin in early design phase of a project?
- Are the COM recommended equalization parameters suitable for the Channel?
- How can we combine the advantages of COM with IBIS-AMI?

25G CO-SIMULATION PROCESS

- Extraction of passive S parameter model of the simulation channel
- Use S parameter to do COM simulation
- IBIS simulation using COM recommended EQ parameter
- IBIS simulation to sweep EQ parameter
- Comparing the eye diagram in time domain

AGENDA

- Traditional IBIS-AMI
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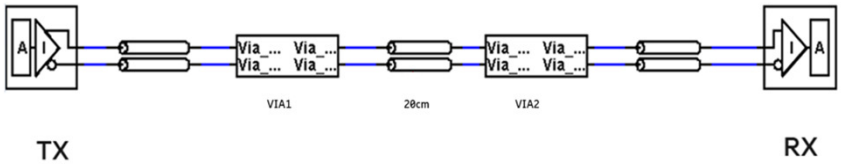
CASE1-SIMULATION TOPOLOGY

Simulation Topology Configuration

- Signal Rate: 25Gbps
- PCB Material: Mid-loss FR4
- PCB Channel Length: 20 cm



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COM SIMULATION CONFIGURATION

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	24.576	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[2.5e-4 2.5e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 30]	mm	[test cases]
z_p (NEXT)	[12 12]	mm	[test cases]
z_p (FEXT)	[12 30]	mm	[test cases]
z_p (RX)	[12 30]	mm	[test cases]
C_p	[1.8e-4 1.8e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[55 55]	Ohm	[TX RX]
f_r	0.75	*fb	
c(0)	0.62		min
c(-1)	[-0.18:0.02:0]		[min:step:max]
c(1)	[-0.38:0.02:0]		[min:step:max]
g_DC	[-12:1:0]	dB	[min:step:max]
f_z	6.144	GHz	
f_p1	6.144	GHz	
f_p2	24.576	GHz	
A_v	0.4	V	
A_fe	0.4	V	
A_ne	0.6	V	
L	2		
M	32		
N_b	0	UI	
b_max(1)	1		
b_max(2..N_b)	1		
sigma_RJ	0.01	UI	
A_DD	0.05	UI	
eta_0	5.20E-08	V^2/GHz	
SNR_TX	27	dB	
R_LM	1		
DER_0	1.00E-12		
Operational control			
COM Pass threshold	3	dB	
Include PCB	0	logical	

Table 93A-2 parameter		
Parameter	**Setting**	**Units**
package_tl_tau	6.141E-03	ns
package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
package_Z_c	78.2	Ohm

Table 92-C12 parameter		
Parameter	**Setting**	
board_tl_tau	6.191E-03	ns
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
board_Z_c	109.8	Ohm
z_bp (TX)	151	mm
z_bp (NEXT)	72	mm
z_bp (FEXT)	72	mm
z_bp (RX)	151	mm

All parameter come from IEEE 802.3bj

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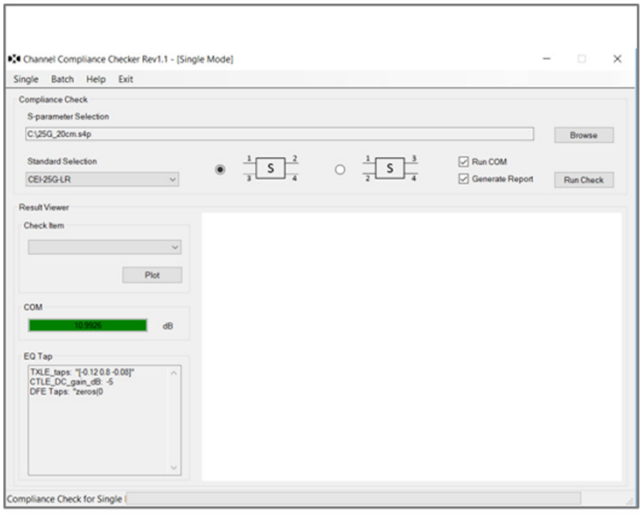
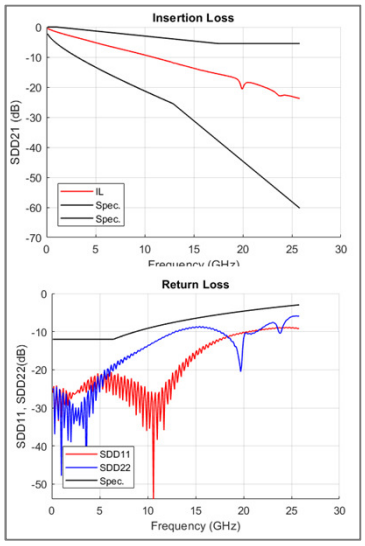
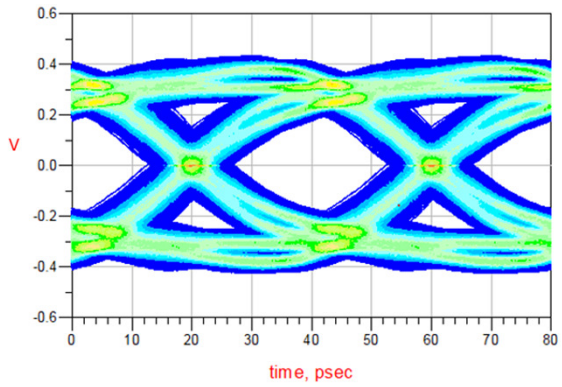
COM SIMULATION RESULT





IBIS-AMI SIMULATION WITH COM RECOMMENDED PARAMETER



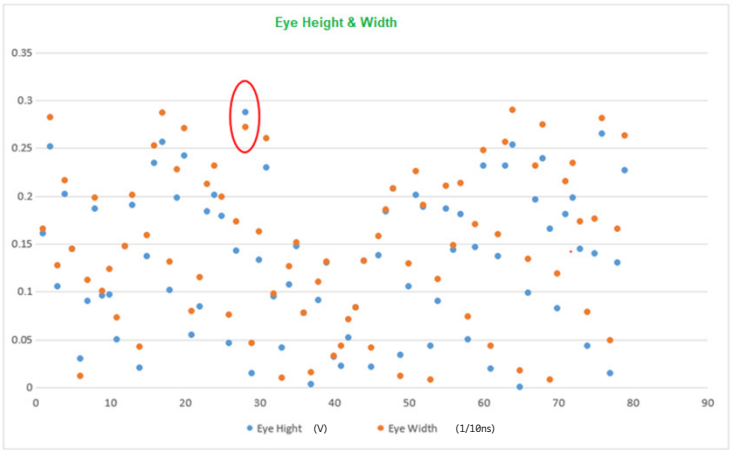
Eye Diagram after RX EQ

index	Width	Height
0.000	2.780E-11	0.289

EQ Parameters: COM Recommend

TX: C(-1)=-0.12
C(0)=0.8
C(1)=-0.08
RX: CTLE=-5
DFE off

IBIS-AMI SWEEP PARAMETERS RESULT



In the red circle is COM recommend EQ parameters

✓ COM recommended EQ parameters produce an acceptable eye opening, but possibly less optimal than the eye opening obtained by time domain simulation

Sweep parameter:
TX: C(-1),C(0),C(1)
RX: CTLE
Total case: 80
Time Domain Simulation

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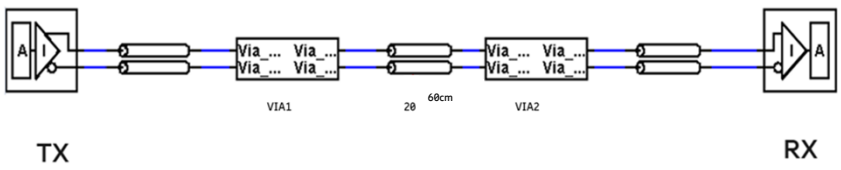
CASE2-SIMULATION TOPOLOGY

Simulation Topology Configuration

- Signal Rate: 25Gbps
- PCB Material: Mid-loss FR4
- PCB Channel Length: 60 cm



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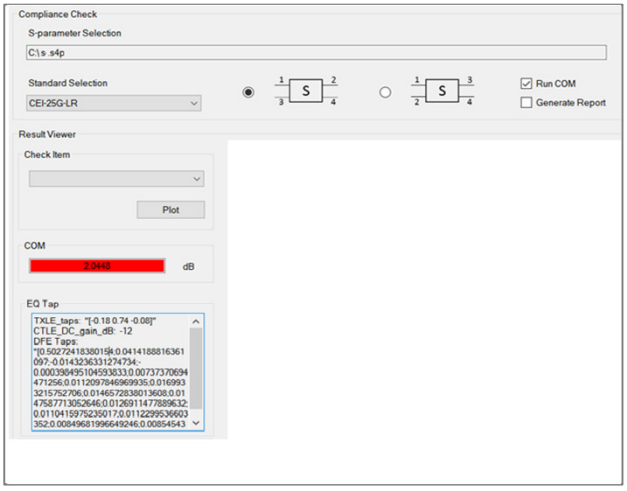
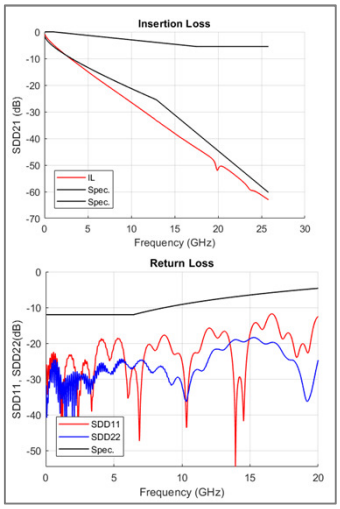
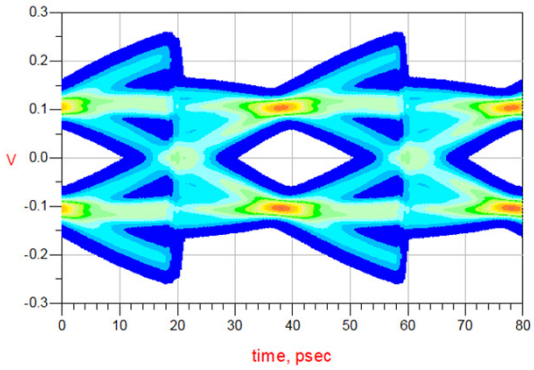
COM SIMULATION RESULT





IBIS-AMI SIMULATION WITH COM RECOMMENDED PARAMETER

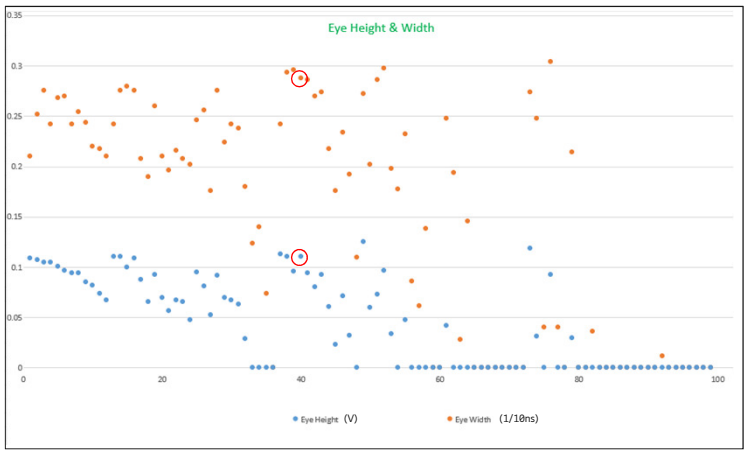


Eye Diagram after RX EQ

index	...robe1.Height)	...Probe1.Width)
0.000	0.109	2.100E-11

EQ Parameters: Use COM Recommended

IBIS-AMI SWEEP PARAMETERS RESULT



In the red circle is COM recommended EQ parameters

- ✓ COM recommended EQ parameters produce a good time domain eye diagram

Sweep parameter:
TX: C(-1),C(0),C(1)
RX: CTLE&DFE
Total case: 100
Time Domain Simulation

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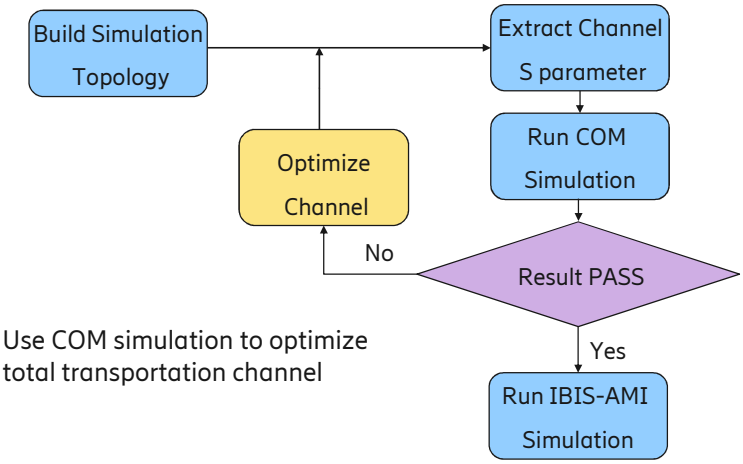
CO-DESIGN SIMULATION FLOW



Use COM simulation to optimize total transportation channel

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AGENDA

- Traditional IBIS-AMI
- COM Overview
- IBIS-AMI Co-design with COM for 25G
- Two example channels
- Co-simulation Conclusion
- Next Steps

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CO-SIMULATION CONCLUSION

- COM enables passive channel evaluation of high-speed signals at early design phase
- COM recommended EQ parameters are suitable for same channel in time domain simulation
- COM simulation is faster, making them more suitable for the post-layout phase of large designs to sweep EQ parameters

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AGENDA

- Traditional IBIS-AMI
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NEXT STEPS

- Model crosstalk in actual link
- Co-simulation for 56G PAM-4
- Accuracy of IBIS-AMI model
- Correlation of Co-simulation with measurement

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How To Fix a Short Channel Problem With AMI and COM Simulation

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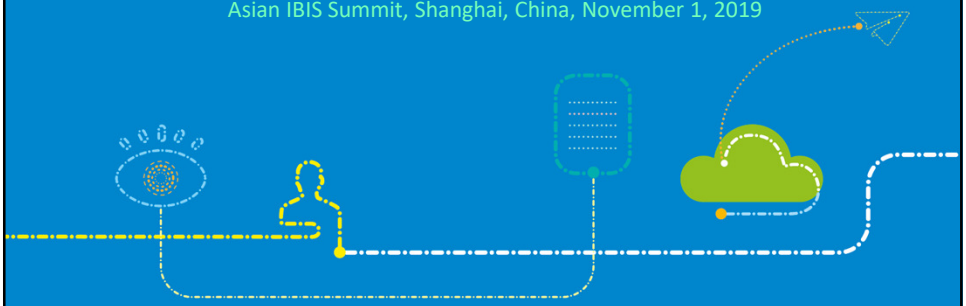
Asian IBIS Summit, Shanghai, China, November 1, 2019



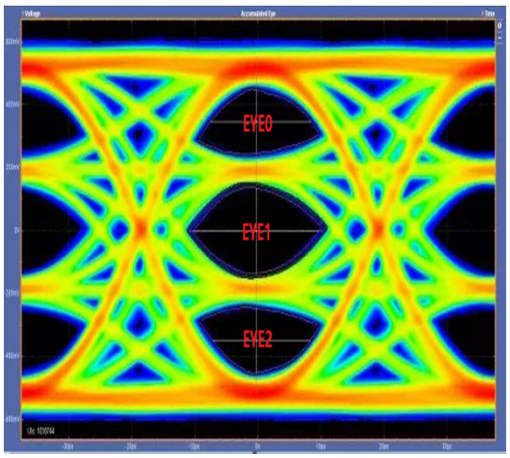
Agenda

- Overview
- Test Phenomenon
- AMI and COM Simulation
- Summary

Overview

- ➢ Channel active simulation
- Channel Operating Margin (COM)
- AMI

- ➢ Introduce
- The PAM4 signal has three eyes
- The quality of the signal should be determined by the smallest eye
- Eye width/height@BER



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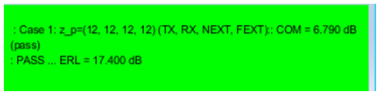
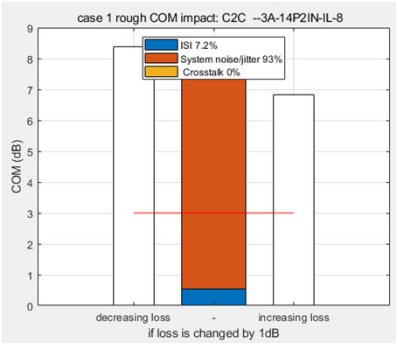
Overview

- ➢ Concerned parameters in COM simulation results
- COM
- ERL
- The percentage of interferences

....

- ➢ Concerned parameters in AMI simulation results
- Eye width@BER
- Eye height@BER





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Agenda

- Overview
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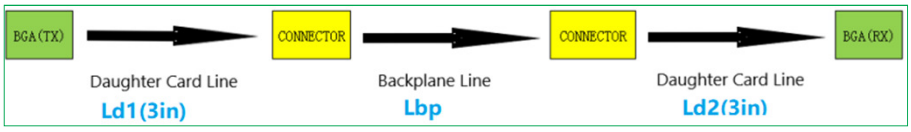
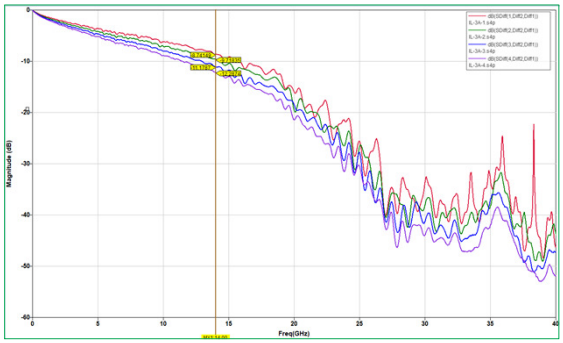
- Summary

Test Phenomenon



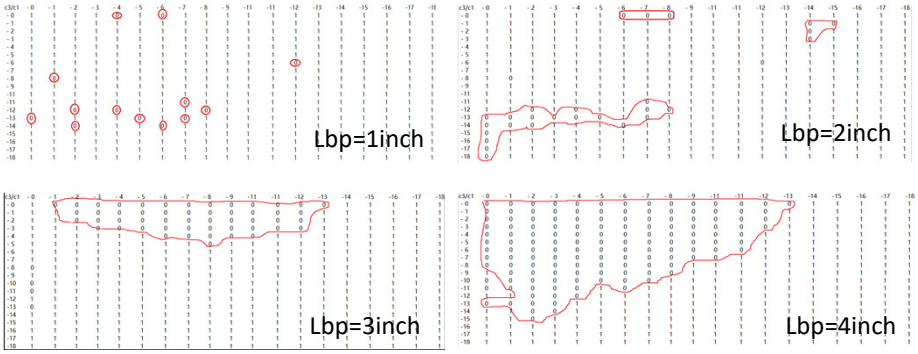
- System channel:
  CEI-56G-LR-PAM4
- Daughter card trace length
  Ld1，Ld2 (3inch)
- Backplane trace length
  Lbp (1inch/2inch/3inch/4inch)
- Without Crosstalk



Test Phenomenon

A group of results with varying parameters of the four channels are presented as follows.

- 0: pass,1: fail
- When the channel length is 1inch, only a few parameters meet the requirement of BER
- With the increase of channel length, the parameters that meet the requirements of BER increase, and the system margin increases as well



Agenda

- Overview
- Test Phenomenon
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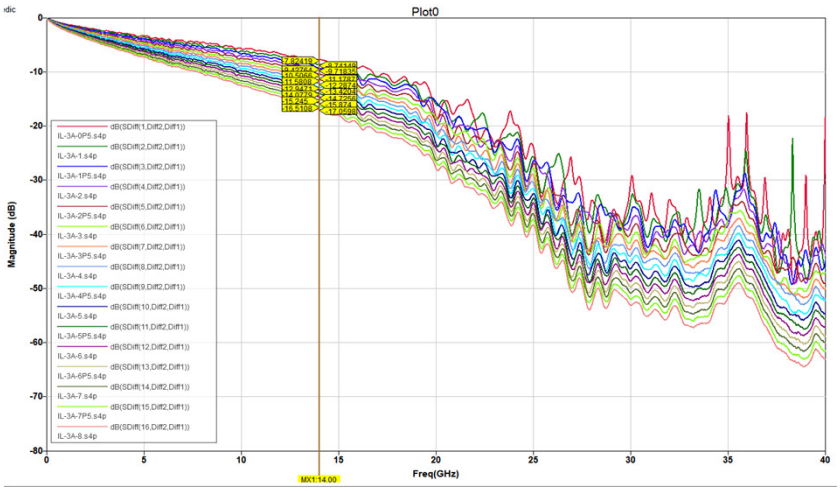
- Summary

AMI and COM Simulation

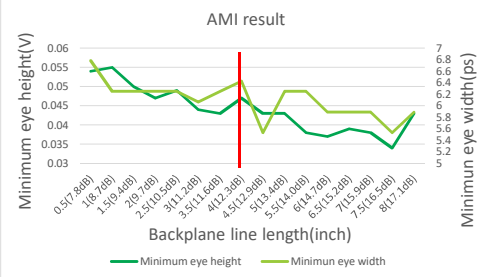
- Channel: 16 different simulation channels
- Without Crosstalk
- Backplane line length: Lbp [range: 0.5 to 8inch,step: 0.5inch]



AMI and COM Simulation

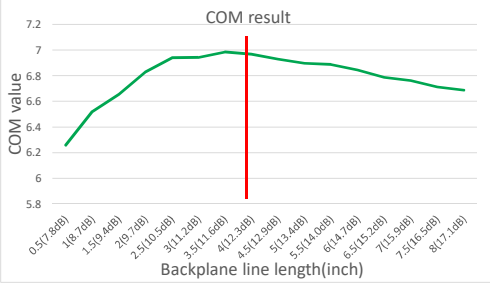
AMI Simulation Result

- Inconsistent with the trend of actual test results
- The eye width and height decrease with the increase of channel length, leading to a decay in system margin



COM Simulation Result

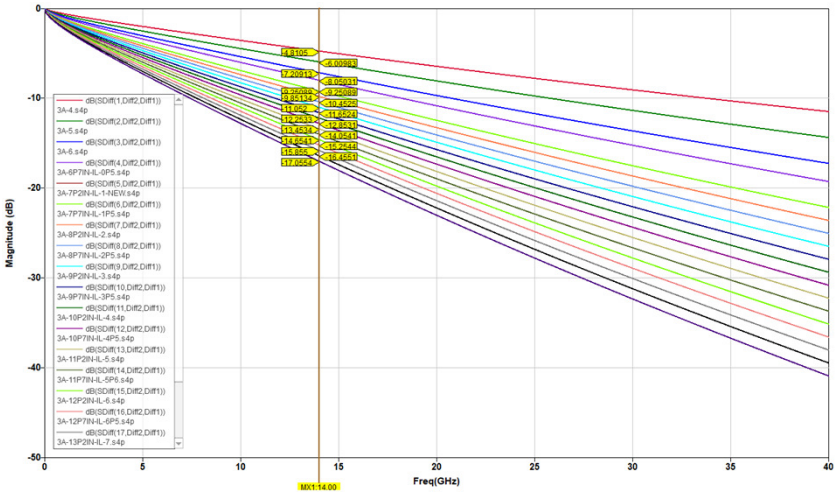
- Consistent with the trend of actual test results
- COM value increases with the increase of backplane line length at first.
- After peaking, COM value then starts to decrease while the backplane line length continues to increase



AMI and COM Simulation

Whether the above rules and differences are caused by the connector？

- Remove the connector and Footprint (excluding the impact of ILD, SKEW and RL)
- Use transmission line channel verification only



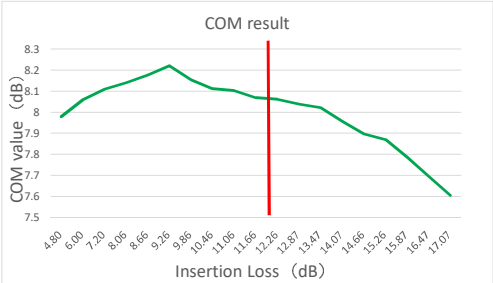
AMI and COM Simulation

AMI Simulation Result

- Trends become similar to COM results.
- The eye width and height increase with the loss increases at first
- The eye width and height then starts to decrease while the loss continues to increase

COM Simulation Result

- Consistent with the trend of actual test results
- COM value increase as loss increases at first
- After peaking, COM value then start to decrease while loss continues to increase



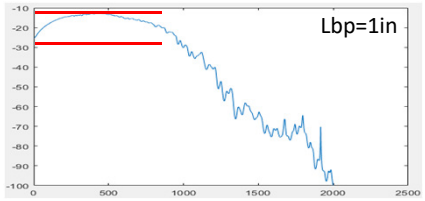
AMI and COM Simulation

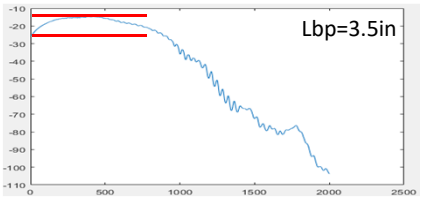
Why do such rules appear？

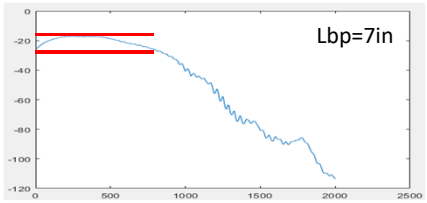
COM simulation can provide more information compared to AMI simulation

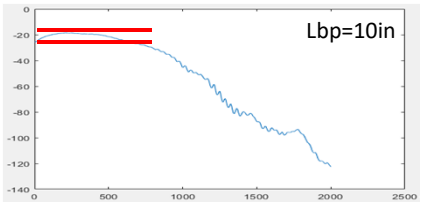
COM simulation tool supports to export insertion loss curve after CTLE

- For short channel, the compensation in insertion loss is too much at low frequency
- With the increase of channel length, the compensation in insertion loss at high and low frequency tends to balance









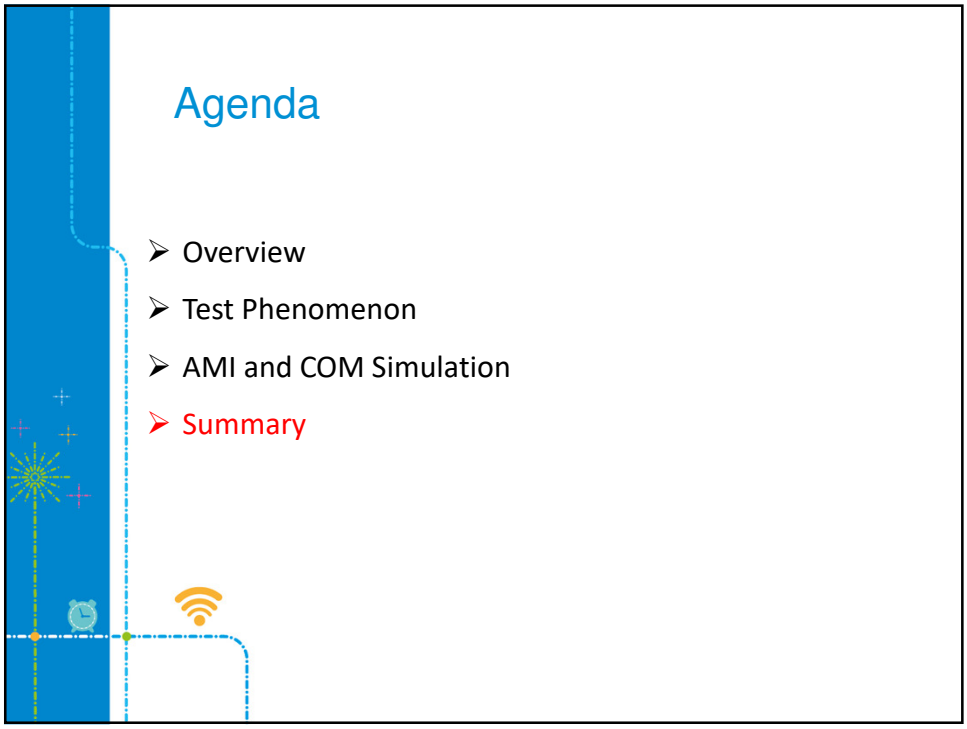
AMI and COM Simulation

The comparison of the influence of CTLE on channel is shown in the following table

- For short channel, CTLE has little influence on ISI
- For long channel, CTLE has a great influence on ISI
- When CTLE is operating, the proportion of ISI in short channel is greater than that of long channel

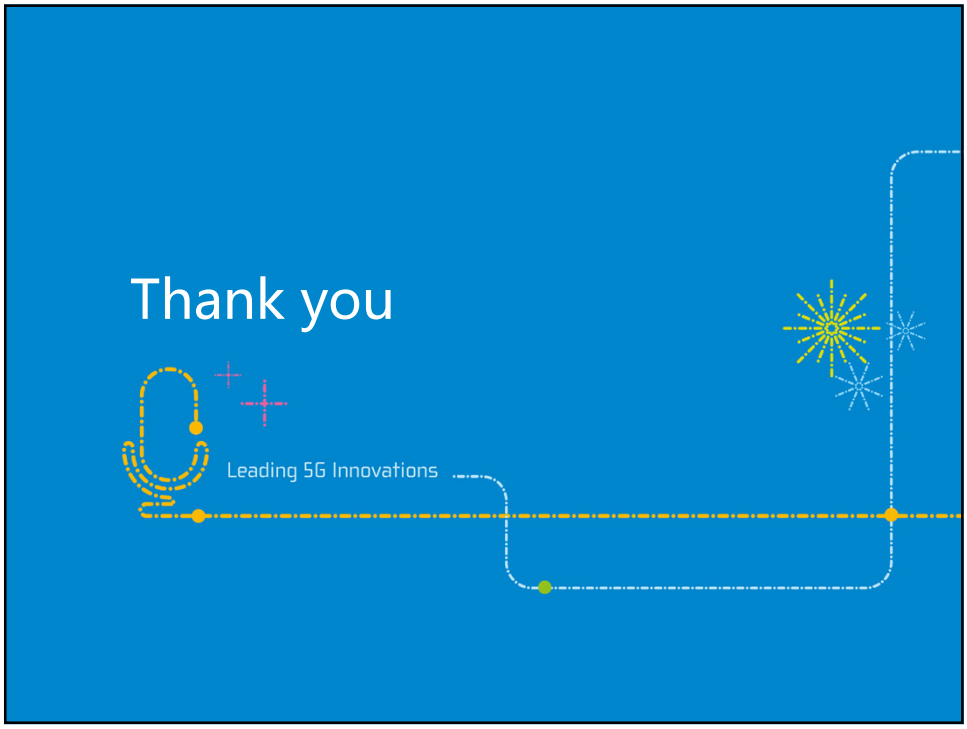
When the channel insertion loss is very small, CTLE compensates too much for the insertion loss at low frequency band, which is not conducive to reducing ISI

Length of line in Backplane	CTLE	COM12MM	FOM	ASV	seg_ISI	ISI/ASV
1in	off	6.2315	17.4946	35.9423	0.0028494	7.93%
	on	6.5206	17.7784	35.8026	0.0025736	7.19%
10in	off	4.8362	16.1031	15.4962	0.0016943	10.93%
	on	6.4419	17.6499	10.9379	0.00065234	5.96%



Summary

- When the channel insertion loss is very small, CTLE compensates too much for the insertion loss at low frequency band, which is not conducive to reducing ISI
- In high-speed design, the length of the channel should be designed meeting the requirements of a certain value
- During AMI simulation, it will be more helpful to find problem if more detailed information can be output (such as CTLE curve).
- When analyzing problems, it is recommended that both COM and AMI simulation should be done if possible.


Thank you
Leading 5G Innovations

Agenda

Think Bigger. Reach Further.

- 112G Passive Channel Modeling: C2M and CR loopback.
- COM Simulation for 100G-CR loopback channel.
- Conclusion

2

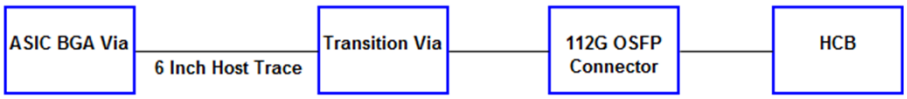
Think Bigger. Reach Further.

Passive Channel Modeling

3

Think Bigger. Reach Further.

802.3ck C2M Host Channel Modeling



Host board PCB is 26 Layers, total 4mm thickness, M7N level material.

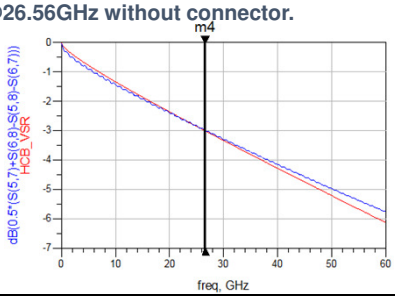
Host trace width/spacing is 8mil/10mil, 6inch of trace includes 0.8inch neck-down (4mil/4mil).

Vias stub modeled as 6mils, long via length, solution frequency up to 80GHz.

Referred to diminico_3ck_01a_0719, host channel insertion loss budget is 7dB@26.56GHz without connector.

HCB (Host compliance board) modeled using simulation tools, 3dB@26.56GHz.

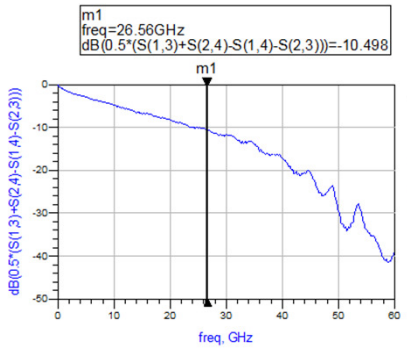
m4
freq=26.56GHz
HCB_VSR=-3.002
dB(0.5*(S(5,7)+S(6,8)-S(5,8)-S(6,7)))=-3.004



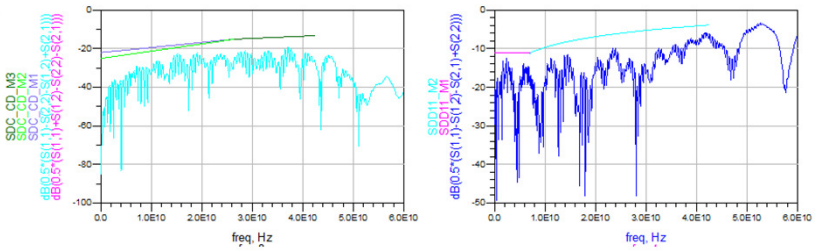
4

802.3ck 100G_C2M Host Channel Modeling

Think Bigger. Reach Further.



Host channel Insertion Loss

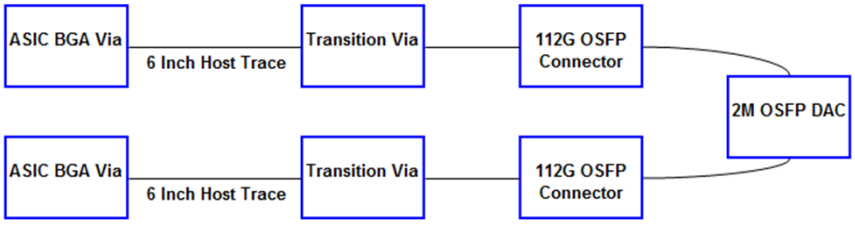


Host channel Return Loss

5

802.3ck 100G_CR Host Channel Modeling

Think Bigger. Reach Further.



Host board PCB is 26 Layers, total 4mm thickness, M7N level material.

Host trace width/spacing is 8mil/10mil, 6inchs trace included 0.8inch neck-down (4mil/4mil).

Vias stub modeled as 6mils, long via length, solution frequency up to 80GHz.

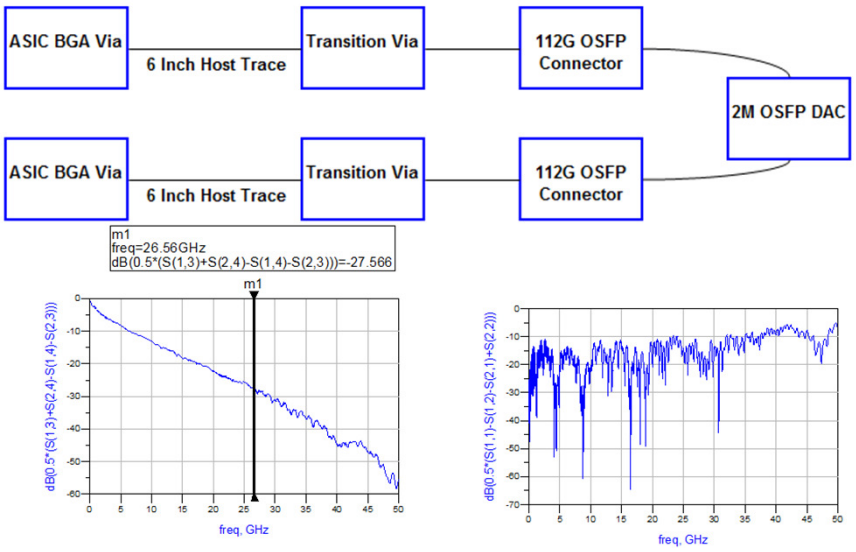
Referred to diminico_3ck_01a_0719, host channel insertion loss budget is 7dB@26.56GHz without connector.

End to end insertion loss target is less than 28.5dB@26.56GHz.

6

802.3ck 100G_CR Host Channel Modeling

Think Bigger. Reach Further.



7

Loopback channel Insertion loss

Loopback channel return loss

Think Bigger. Reach Further.

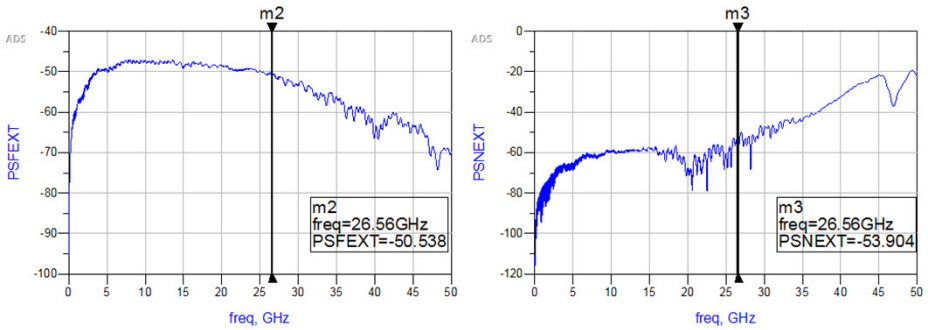
100G-CR COM Simulation

8

Think Bigger. Reach Further.

802.3ck_COM Simulation Results_100G-CR 2M OSFP Loopback

- The Channel Operating Margin (COM) has been defined in IEEE802.3ck, and the channel margin shall be greater than or equal to 3dB after COM calculation for 100G-CR/KR Channel. Note that the COM code is the draft version from IEEE802.3ck Task Force (**Code version: mellitz_3ck_02_0319_COM2p60, 3ck_KR_mellitz_06_12_2019_2**).
- 5 aggressor FEXT channel and 3 aggressor NEXT channel on both sides of victim channel are considered for the COM crosstalk analysis.
- The victim is the 27.56dB 2M OSFP loopback channel in the previous section.
- Crosstalk power sum results as follows:



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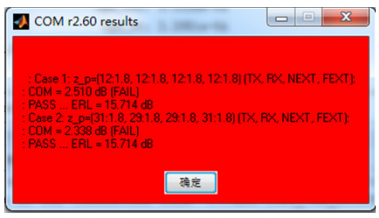
Think Bigger. Reach Further.

802.3ck_COM Simulation Results_100G-CR 2M OSFP Loopback

```
--- Testcase 2 results ---
                    code_revision: '2.60'
                          Z11est: 95.0632
                          Z22est: 95.0721
                           ERL11: 15.7669
                           ERL22: 15.7137
                             ERL: 15.7137
                           RxFFE: ''
                       RxFFEgain: ''
                     config_file: 'F:\112G Data\IBIS Submit\112_COM\mellitz
                      file_names: ''KR_eval_ --112G_CR_COM_VICTIM,KR_eval_
                          levels: 4
                      Pkg_len_TX: [31 1.8000 0 0]
                    Pkg_len_NEXT: [29 1.8000 0 0]
                    Pkg_len_FEXT: [31 1.8000 0 0]
                      Pkg_len_RX: [29 1.8000 0 0]
                       R_diepad: [45 45]
                         pkg_Z_c: [2x4 double]
                             C_v: [0 0]
                   baud_rate_GHz: 53.1250
                   f_Nyquist_GHz: 26.5625
                             BER: 1.0000e-04
                             FOM: 13.7052
                         sigma_N: 3.5284e-04
                        DFE4_RSS: 0.1715
                        DFE2_RSS: 0.3860
    channel_operating_margin_dB: 2.3381
available_signal_after_eq_mV: 3.1441
                peak_uneq_pulse_mV: 57.2731
                uneq_FIR_peak_time: 1.5612e-08
          steady_state_voltage_mV: 29.1113
                          FOM_ILD: 0.3399
```




```
Peak_ISI_XIK_and_Noise_interference_at_BER_mV: 2.4021
peak_ISI_XIK_interference_at_BER_mV: 1.6790
peak_ISI_interference_at_BER_mV: 1.2011
equivalent_ICI_sigma_assuming_PDF_is_Gaussian_mV: 0.3229
peak_MDXIK_interference_at_BER_mV: 1.1099
peak_MDNEXI_interference_at_BER_mV: 0.8709
peak_MDFEXI_interference_at_BER_mV: 0.5628
ICN_mV: 2.5886
MDNEXI_ICN_92_46_mV: 2.2679
MDFEXI_ICN_92_47_mV: 1.2479
equivalent_ICN_assuming_Gaussian_PDF_mV: 0.2984
SNR_ISI_XIK_normalized_1_sigma: 16.8577
SNR_ISI_est: 32.0779
Pmax_by_Vf_est: 0.4236
CILE_zero_poles: [2.1250e+10 5.3125e+10 2.1250e+10]
CILE_DC_gain_dB: -11
g_DC_HP: -3
HP_poles_zero: 664062500
IXLE_taps: [-0.0200 0.0800 -0.2800 0.6200 0]
DFE_taps: [24x1 double]
sgm_Ani__isi_xt_noise: 6.5327e-04
sgm_isi_xt: 4.6244e-04
sgm_isi: 3.3335e-04
sgm_xt: 3.2051e-04
sgm_noise__gaussian_noise_p_DD: 4.6142e-04
sgm_p_DD: 1.7776e-04
sgm_gaussian_noise: 4.2581e-04
sgm_G: 4.2643e-04
sgm_rjit: 8.9107e-05
sgm_N: 3.5284e-04
sgm_IX: 2.2228e-04
total_IL_wpkgs_dB_at_Fnq: 39.1631
IL_dB_channel_only_at_Fnq: 27.1907
```

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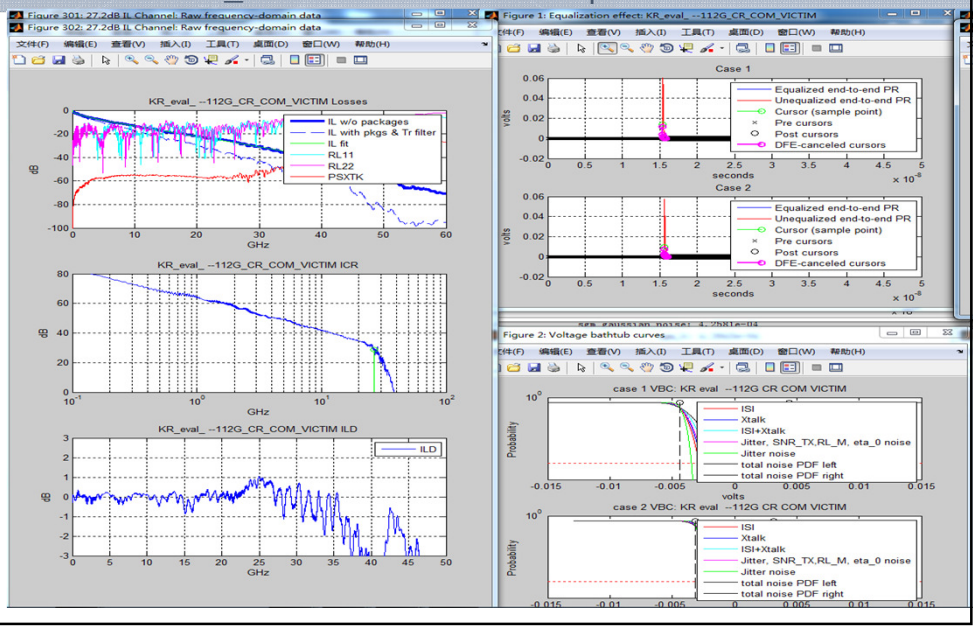
Think Bigger. Reach Further.

802.3ck_COM Simulation Results_100G-CR 2M OSFP Loopback

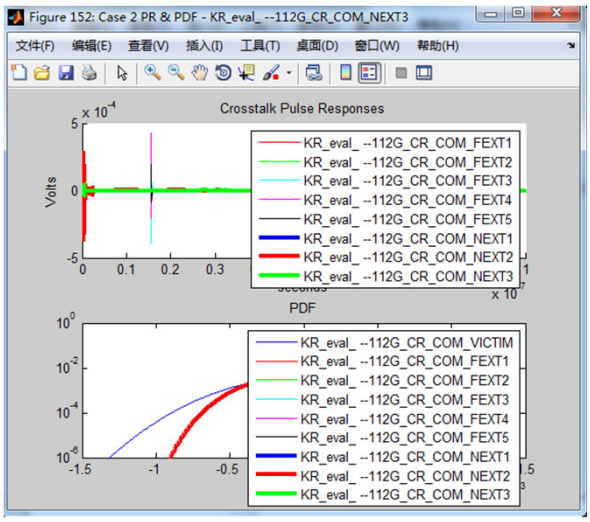
- 24 taps fixed DFE used in the COM simulation. Since the COM configuration is not finalized, it's currently difficult to pass the COM 3dB margin.

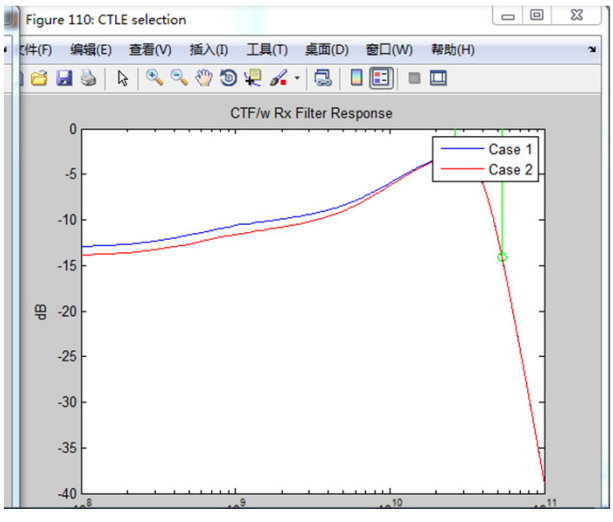


11

Think Bigger. Reach Further.

802.3ck_COM Simulation Results_100G-CR 2M OSFP Loopback





12

Think Bigger. Reach Further.

802.3ck_COM Simulation Results_100G-CR 2M OSFP Loopback

- Config_files:

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]
L_s	[0.12, 0.12]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[12 29; 1.8 1.8]	mm	[test cases]
z_p (FEXT)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (RX)	[12 29; 1.8 1.8]	mm	[test cases]
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 45]	Ohm	[TX RX]
A_v	0.39	V	vp/vf=.694
A_fe	0.39	V	vp/vf=.694
A_ne	0.578	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.5		min
c(-1)	[-0.3:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.12]		[min:step:max]
c(-3)	[-0.06:0.02: 0]		[min:step:max]
c(1)	[-0.2:0.05:0]		[min:step:max]
N_b	24	UI	
b_max(1)	0.85		
b_max(2..N_b)	0.3		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_KR_{date}\	
SAVE_FIGURES	1	logical
Port Order	[1 3 2 4]	
RUNTAG	KR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10	dB
DER_0	1.00E-04	
T_r	6.16E-03	ns
FORCE_TR	1	logical
Include PCB	0	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	3000	
beta_x	2.53E+09	
rho_x	**0.25**	
fixture delay time	0	s
TDR_W_TXPKG	0	
N_bx	24	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A? parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Table 92?2 parameters 5.2dB at 26.56GHz		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 0.000599 0.0001022]*	1.286 dB/in or 0.0506 dB/mm at 100 ohms
board_tl_tau	*6.200E-03*	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	*102.7*	mm
z_bp (NEXT)	*102.7*	mm
z_bp (FEXT)	*102.7*	mm
z_bp (RX)	*102.7*	mm

Floating Tap Control		
N_bg	**0**	**0 1 2 or 3 groups**
N_bf	*0*	taps per group
N_f	40	UI span for floating taps
bmaxg	0.1	max DFE value for floating taps

yellow indicates WIP

13

Think Bigger. Reach Further.

Conclusion

- **In the early stage of 112G product development, Celestica is preparing the channel modeling for IBIS-AMI simulation. Most 112G IBIS-AMI model will be available in 2020-Q1.**
- **PCB still can be an option for 112G switch, but the SI performance of the PCB need to be improved (M8 Level).**
- **In our simulation, the host channel trace length is only 6inch, it's difficult to improve the insertion loss performance to get better COM margin, so it has a higher expectation on Xtalk to improve the SNR (BER).**
- **Will continue update the 112G simulation.**

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Thank You

Celestica™

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Channel Simulation Over DDR4/5 and Above

Kumar Keshavan, Ambrish Varma, Ken Willis, Skipper Liang
Asian IBIS Summit
Shanghai, China
November 1, 2019

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Two Concerns:

- As the transmission rate of memory bus goes beyond 5Gbps, besides the well-known timing and overshoot/undershoot analysis, it requires BER prediction analysis and channel analysis
- Two additional concerns we need to face while using channel engine to deal with memory bus:
  - Asymmetric rising/falling edges

    Different from differential serial buses, single-ended memory buses will have non-symmetrical rising and falling edges due to the inherent difference between these two kinds of circuits
  - Strobes as timing reference

    While the sampling clock ticks in serial bus are recovered from the signal itself by CDR, the sampling clocks or the timing references in memory bus will be the strobes rather than any recoveries

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Asymmetric Rising and Falling Edges

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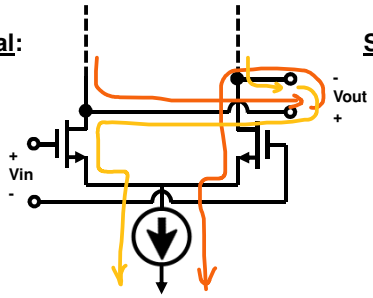
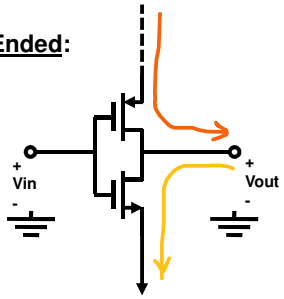
Circuits

Differential:

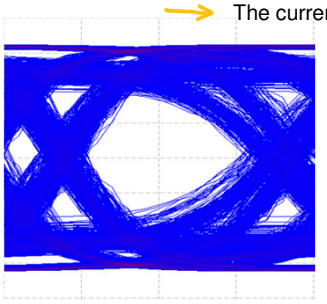


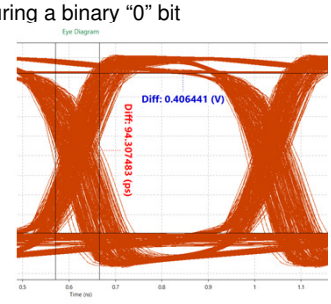
Single-Ended:



The current path during a binary “1” bit

The current path during a binary “0” bit





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Overview

- As channel simulation and IBIS-AMI modeling methods are adapted from serial link to DDR interface analysis, we encounter IBIS I/O models with asymmetric rising and falling edges
- This is different from the highly symmetric drivers we typically encounter with serial link analysis
- Traditional single-step response methods for impulse response generation may not reproduce circuit simulation results accurately enough
- These slides show how an EDA tool can handle this (without changes to the IBIS specification)
- All cases use **Micron**'s **y11a.ibs** file for 8Gbps DDR5

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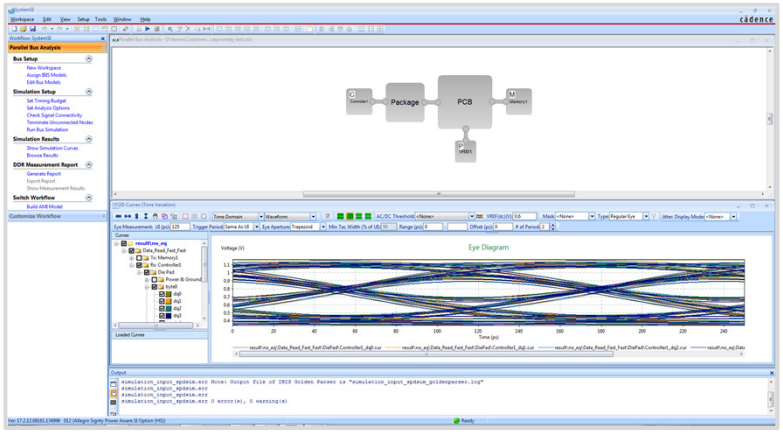
Testbench

- Package block uses an extracted RLCK SPICE model
- PCB block uses W-elements with 0.3 meter lengths



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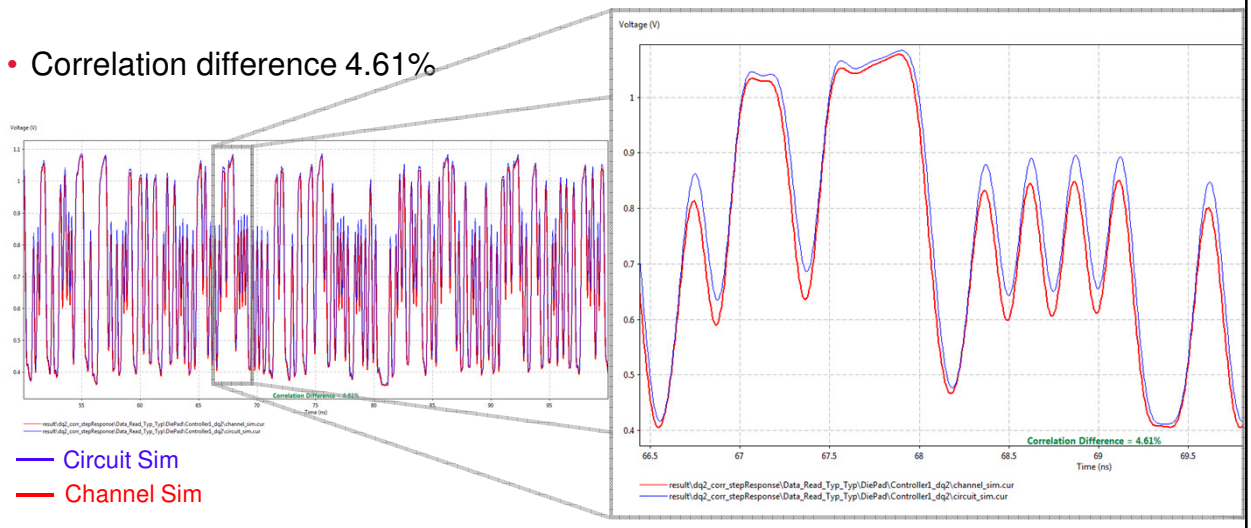
Characterizing with Step Function – One Rising Transition

- Correlation difference 4.61%



Circuit Sim
Channel Sim

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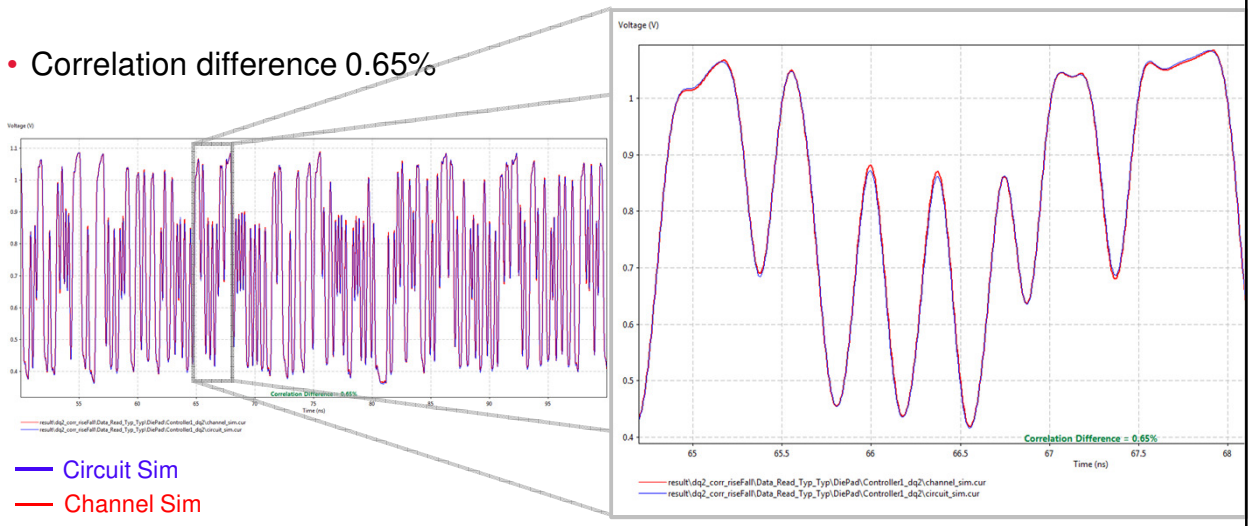
Characterizing with both Rising and Falling Transition

- Correlation difference 0.65%



Circuit Sim
Channel Sim

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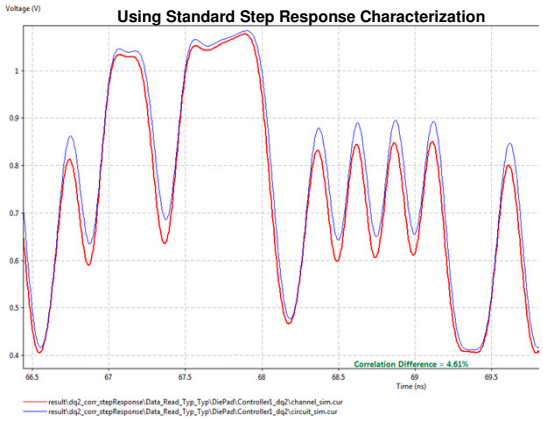
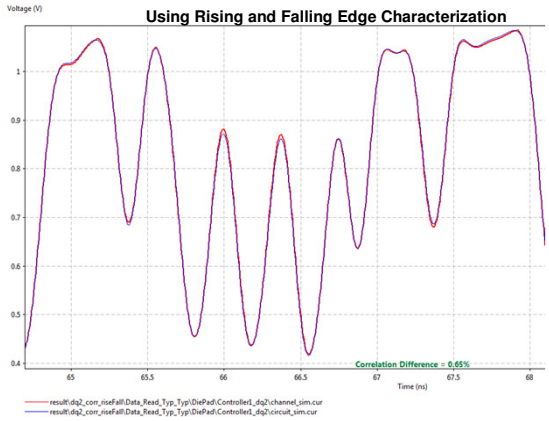
Comparison between Two Different Methods

- Correlation error vs. circuit simulation reduced by about 4%





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Summary

- The **DQ_34_3600** I/O model has some asymmetry in its rising and falling edges
- Standard SerDes step response characterization did not do a great job in capturing this behavior, as seen in the circuit / channel sim correlation
- Characterization methods using rising and falling edges captured this behavior very well for channel simulation

```
|*************************************************************************
|
[Ramp]
R_load = 50
|
|         typ                        min                        max
|
dV/dt_r 3.7990E-01/6.4024E-11   3.4860E-01/8.7846E-11   4.0938E-01/4.9359E-11
dV/dt_f 4.4605E-01/5.4840E-11   4.2048E-01/7.6564E-11   4.6793E-01/4.2557E-11
|*************************************************************************
```


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Strobe as Timing Reference

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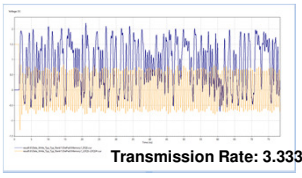
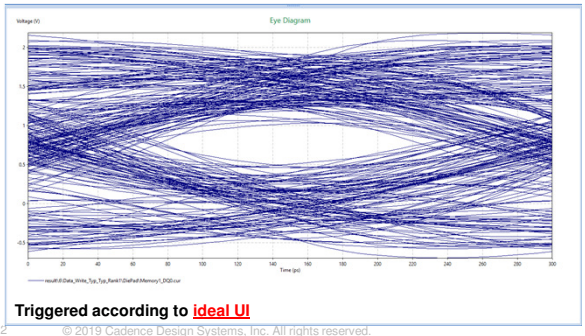
Overview(1)

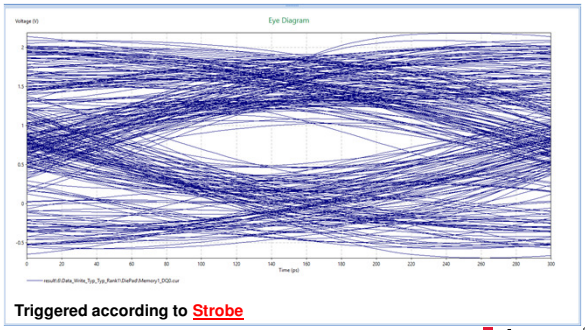
- Different timing reference – Different selection of “trigger” can result in different eye opening



Transmission Rate: 3.333Gbps



Triggered according to ideal UI



Triggered according to Strobe

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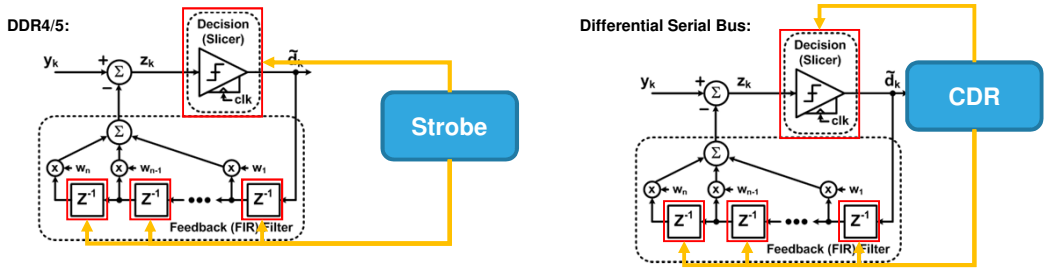
Overview(2)

- DFE's clock in memory bus will be supplied by Strobe rather than CDR, which can be seen in most differential serial bus



- As channel simulation and IBIS-AMI modeling methods are adapted from serial link to DDR interface analysis, serial link CDR algorithms are often used for analysis
- What is the impact?

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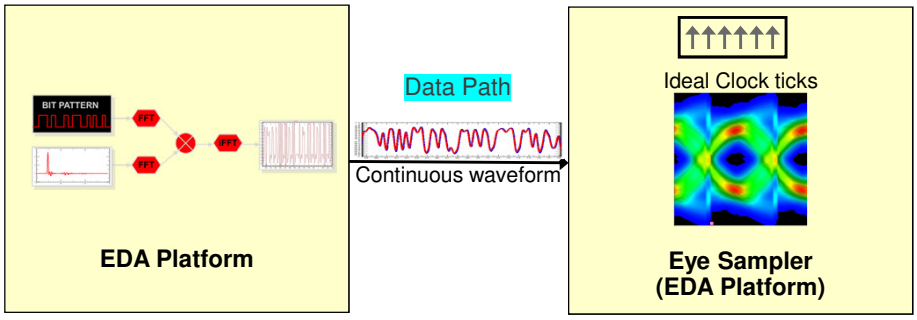
Current CDR-Based Method

- Centers the eye for each individual signal
  - Ideal clock ticks are generated internally by the eye sampler
  - Clock ticks can also be generated by AMI models and sent to the eye sampler



- Some controllers have some individual bit de-skewing

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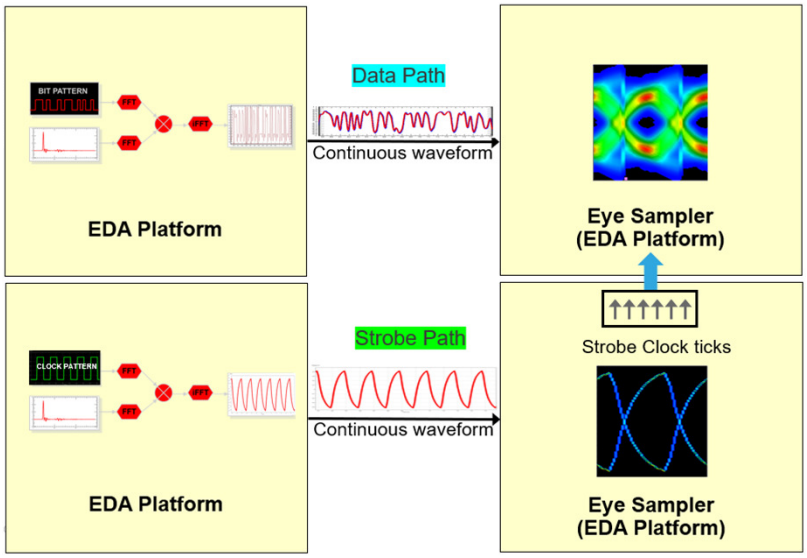
True Strobe Timing (TST)

- Clock ticks are collected from the strobe channel instead of the data channel
  - With real strobe, this is done for entire byte lane
- Strobe channel is only fed with 0101 data



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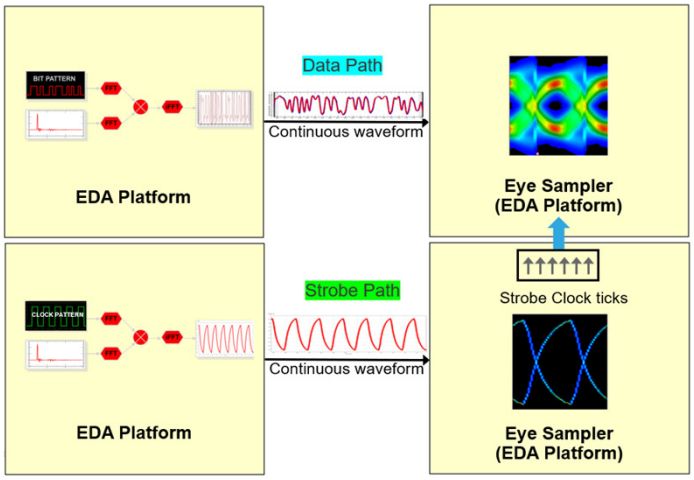
Comparison of Results

- CDR vs. TST
- CDR vs. TST with jitter impairments
- Test configuration
  - 1 data line is used for simulations
  - 6 Gbps
  - Rx CTLE
  - Rx 4 tap DFE
  - In phase between strobe and data



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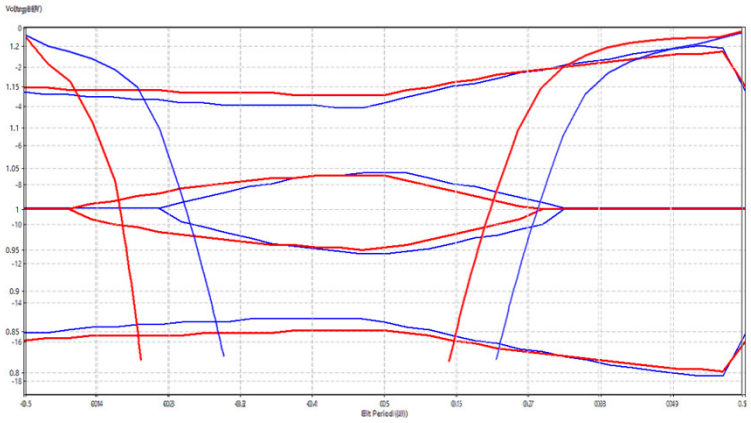
CDR vs. TST

CDR
Strobe



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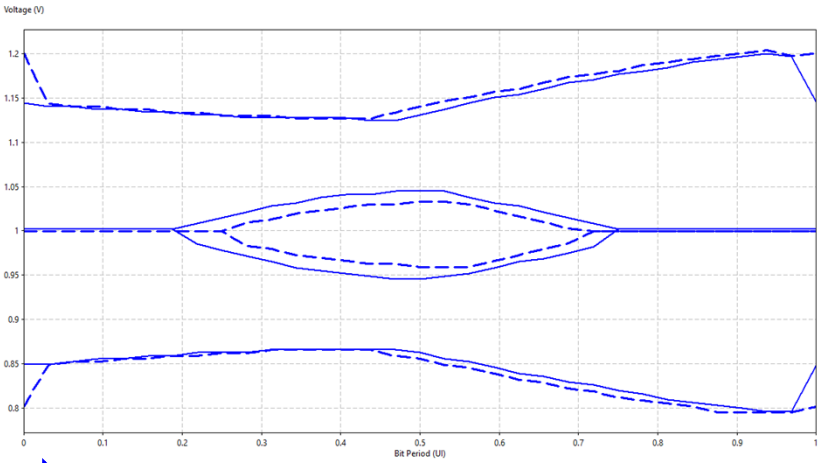
CDR Results with Dj Applied at Tx



5%UI
15%UI

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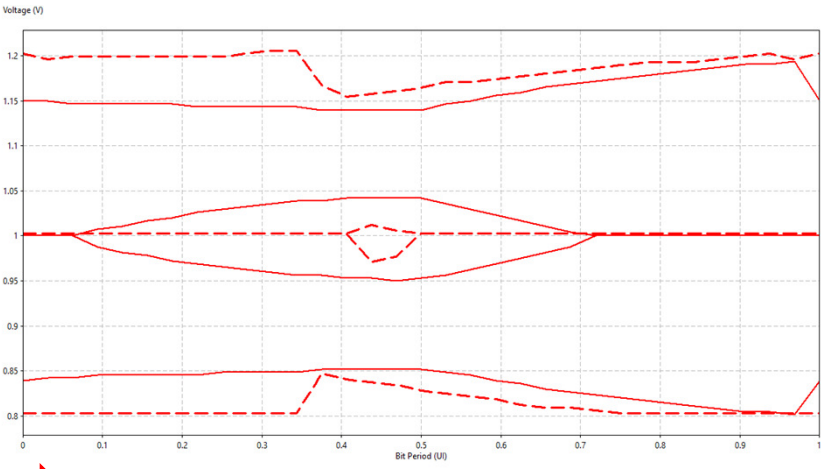
Strobe Results with Dj Applied at Tx



5%UI Dj on both strobe and data

15%UI Dj on both strobe and data

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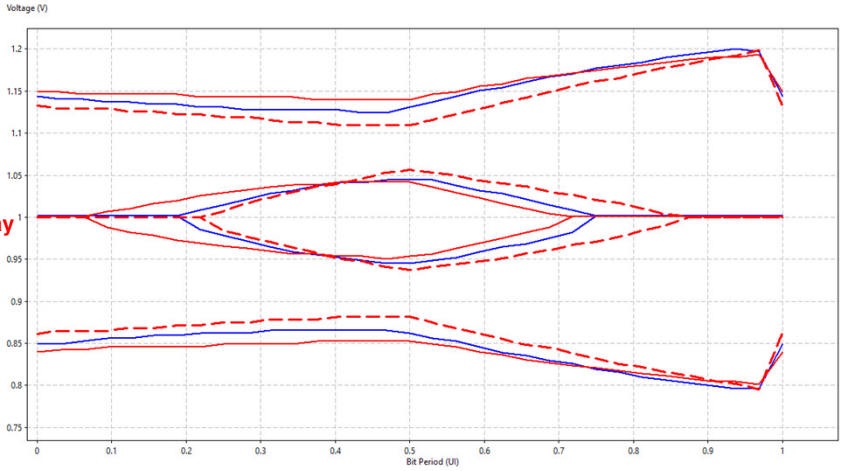
CDR vs. TST

- After delaying by 0.2 UI

CDR
Strobe
Strobe w delay



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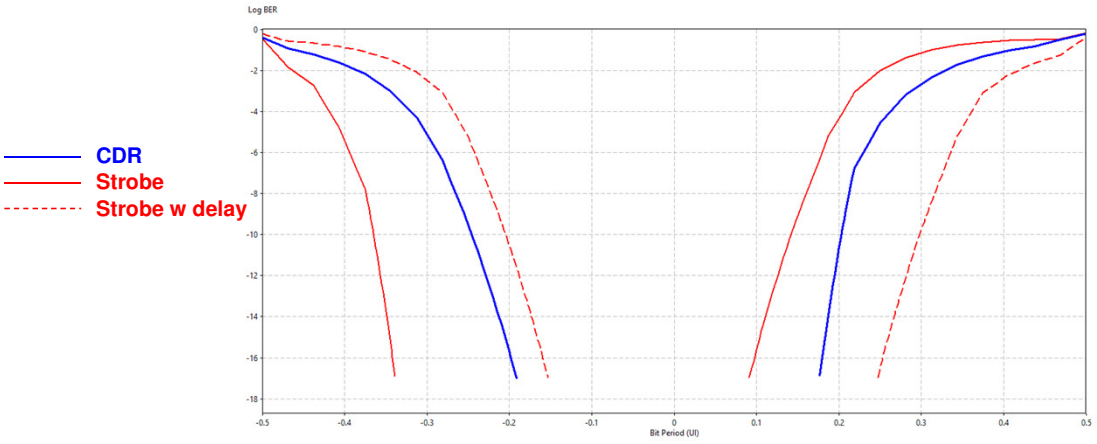
CDR vs. TST

- After delaying by 0.2 UI



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Summary

- Using default CDR instead of actual strobe to get clock risks will miss important impairments/jitter for parallel bus topology
- Analysis results show false optimism using CDR approach as compared to true strobe timing methodology
- Need to model delay accurately

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