Innovations in DDR Memory Simulation

<table>
<thead>
<tr>
<th>Stephen Slater</th>
<th>NOVEMBER 1, 2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Asian IBIS Summit, Shanghai, PRC</td>
<td></td>
</tr>
</tbody>
</table>
A Typical DDR5 Application

1 DIMM Per Channel

2 DIMMs Per Channel

Data (DQ) – Single-ended
Data Strobe (DQS) – Differential
Microstrip & Stripline
What Does it Mean to Succeed?

THE MEASURE OF SUCCESS FOR A PRODUCT WITH DDR5

• No system failures, under stress
  • At Max and Min temperatures
  • Using multiple vendors’ DIMMs
• 1 DIMM slot and 2 DIMM slots filled
• Running diagnostic software that stresses the memory access
• Graceful performance degradation

“I can stop testing when I’m certain my manager is satisfied with the product quality risk”

Source: Burn-in environment test chambers by EDA-Industries S.p.a
# How Did we Get to DDR5?

## A Road Paved by Innovation

<table>
<thead>
<tr>
<th>Signal</th>
<th>MT/s</th>
<th>Generation</th>
<th>Characteristics</th>
<th>Specification</th>
<th>Introduction</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>DDR5+</td>
<td>“Hyper Speed”</td>
<td></td>
<td>2019</td>
</tr>
<tr>
<td></td>
<td>4200 – 8000+</td>
<td></td>
<td>• Eye collapses</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Impulse response</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• BER Rj/Dj, Rn/Dn</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DDR4</td>
<td>“Serial Speed”</td>
<td></td>
<td>2014</td>
</tr>
<tr>
<td></td>
<td>1600 – 4200</td>
<td></td>
<td>• Rx Masks</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Bit error rates</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DDR/2/3</td>
<td>“High Speed Digital”</td>
<td></td>
<td>2002</td>
</tr>
<tr>
<td></td>
<td>200 – 1600</td>
<td></td>
<td>• Transmission lines</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Ts / Th, Skew</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SDRAM</td>
<td>“Low Speed”</td>
<td></td>
<td>1961</td>
</tr>
<tr>
<td></td>
<td>33 – 133</td>
<td></td>
<td>• Fanout</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Capacitance</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Ensuring First Pass Success - One Layer Deeper

ENSURING THE SYSTEM IS PERFORMANT AND RELIABLE

- Logic / Protocol
- Probing
- Power Integrity
- Rx Test
- DDR Methodology
- Test Fixtures
- Modeling and Simulation
- Tx Test

KEYSIGHT TECHNOLOGIES
Change, Challenges and Solutions

1. Crosstalk, Jitter and Bit-Error-Rate (BER) Specs
2. Closed eyes need equalization and training
3. Innovations in Simulation and Modeling of DDR5 & LPDDR5 systems
1. Crosstalk, Jitter and Bit-Error-Rate (BER) Specs
Crosstalk

THE IMPORTANCE OF THE SIGNAL RETURN PATH

No Crosstalk, No Jitter – Just ISI from Channel

< -25dB

Signal Return Path – through shared Ground Pin

Nyquist

PCB Trace Routing of Victim + Worst Aggressors

With Crosstalk

Electromagnetic (EM) Simulation
Jitter

BER CONTOUR AT 1E-16 TELLS US THE REAL MARGIN

No Jitter –
Just ISI from Channel

Random Jitter = 0.02 UI
Applied at Tx (2%)

Jitter injected at Tx, and eye measured at the DRAM Solder-Ball (Rx Input)

47% Reduction in Timing Margin
(27ps less margin to mask)

No Jitter –
More ISI from Channel due to higher speed

DDR4-1600

DDR5-4800
• From the draft spec:
  - Maximum Jitter (Dj, Rj and DCD) specifications for Tx and Rx components
  - For Tx and Rx Voltage and Timing tests, system BER is e-16 and requires 5.3e9 minimum UIs for validation (99.5% confidence level)
  - New receiver stressed-eye tests for components and DIMMs

Stressed Eye is calibrated to a specified height and width. The DIMM, DRAM or Memory Controller Rx must be able to receive to the system BER.
Crosstalk, Jitter & BER Specs

**KEY INSIGHTS**

- Jitter and Crosstalk are Very Significant
- Simulation must predict Eye closure due to Random Jitter down to the system BER (1e-16) in a practical time
- EM simulation must capture Crosstalk accurately

**DDR5-4800**
Jitter, crosstalk & Channel ISI

- 64% Reduction in Voltage Margin
- 63% Reduction in Timing Margin
2. Equalization and Training
**Rx Equalization**

**FIRST TIME TO HAVE DFE ON DRAM!**

![Diagram of Rx Equalization](image)

### Mode Register Settings (per DQ)

<table>
<thead>
<tr>
<th>Setting</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Variable Gain</td>
<td>-6dB to 6dB</td>
</tr>
<tr>
<td>VrefDQ</td>
<td>-3 to +3 Offset steps</td>
</tr>
<tr>
<td>DFE Tap 1</td>
<td>-200mV to 50mV</td>
</tr>
<tr>
<td>DFE Tap 2</td>
<td>-75mV to 75mV</td>
</tr>
<tr>
<td>DFE Tap 3</td>
<td>-60mV to 60mV</td>
</tr>
<tr>
<td>DFE Tap 4</td>
<td>-45mV to 45mV</td>
</tr>
</tbody>
</table>

All values subject to change.
DDR5 Rx Specifications are Inside the Die
DDR5 Tx Test: New Methodology Needed

VIRTUAL PROBING INSIDE THE DIE

DRAM Ball → Package Model → Rx EQ Model

Scope display (virtual probe)
DDR5 Rx Test: New DRAM Feature - Loop-Back Mode

5.3 Billion Bits to be Measured!

"Stressed Eye" Generator / Error Checker

Analyzer

RJ-source

SJ source

Victim pattern generator

Aggressor signal generator

Dedicated IO Pins

< Loop-back

Die

Core

DDR5 DRAM

VGA

DFE

FF

Ck Tree

Rx

Br.O.

Pkg

Br.O.

Pkg

Br.O.

Pkg

"Stressed Eye" Generator / Error Checker

Analyzer

RJ-source

SJ source

Victim pattern generator

Aggressor signal generator

5.3 Billion Bits to be Measured!
Skew Adjustment with Write-Leveling

- Due to the fly-by topology of the clock for DDR4 & DDR5, the Clock (Clk) is inevitably skewed to the DQS at each of the independent DRAM.

- The controller has ability to adjust skew between DQ’s, DQS and the Clock signal.

- DQS is adjusted to match the Clk first, then internal alignment of each DQ is performed (via mode register) to remove DQ-to-DQS skew (due to the package and die)

Before Write-Leveling

After Write-Leveling

This can be done in Simulation too!
Equalization and Training

**KEY INSIGHTS**

- Possible to have a Closed eye at input to Rx
- Optimal Eye opening depends on:
  - Vref setting (per DQ)
  - Gain Setting (per DQ)
  - DFE Tap settings (4 taps per DQ)
  - Timing of DQS to DQ
  - Write-leveling (skew adjustment)
3. Innovations in Simulation and Modeling of DDR5 & LPDDR5 systems
Introducing IBIS AMI for DDR Signals

• EQ Necessary for TX: 3 Tap Pre-Emphasis (Feed Forward Equalization)
• EQ Necessary for RX: CTLE/VGA/DFE
• IBIS-AMI offers
  ➢ Portability – One IBIS-AMI mode can run on many EDA tools
  ➢ IP Protection – Digital signal processing behavior is concealed in model DLL/shared object
  ➢ Interoperability - IC Vendor A↔IC Vendor B (AMI defines a common interface between the vendor model and the EDA channel simulator)
  ➢ Non-linearity – As complex as the model vendor wishes the model to be
  ➢ Performance – Ultra low BER simulations in seconds not days over the traditional SPICE simulation
• AMI has been widely adopted by IC, system and EDA companies for SerDes signals but this is the first application to DDR single-ended signals.
How Does Standard IBIS-AMI Work?

**CHANNEL SIMULATION**

IBIS Model *.ibis + AMI Extension *.ami

Standard IBIS Model

TX AMI FFE

TX .dll or .so

TX Analog + Pkg

S-parameter
(Backplane, Board, Cable, Connector, Via, Package, …)

RX AMI DFE+ CTLE/VGA

RX .dll or .so

Post-EQ Waveform

Impulse response of a Linear Time Invariant Network

1. In Training
2. Converged
3. Failed

Back-Channel Interface For Training
What Do We Need for DDR5 AMI To Work?

Supporting Parallel, Single-Ended Signals With External Clocks

Input to DRAM

After Gain & 4 Tap DFE

DFE Clocked by DQS:
- Correlated Jitter on DQ & DQS cancels out
- Uncorrelated Jitter on DQS is transferred to DQ

Single-Ended Signal can have a DC Offset

Asymmetric Eye: Rise Time ≠ Fall Time

Asymmetric Eye: Crossing Points are shifted in the Equalized Eye

1.1V

0.55V
The Solution

**SIMULATION TECHNOLOGY INNOVATIONS**

1. **Multiple Tx and Rx in one Simulation**
   - TX AMI FFE
   - TX Analog + Pkg
   - RX Analog + Pkg
   - RX AMI DFE+ CTLE/VGA

2. **Calculate Impulse Responses for both a Rising Edge and a Falling Edge**
   - Post-EQ Waveform
   - Clock ticks

3. **Simulator applies the correct impulse responses to the part of the waveform that is rising, or falling**

4. **Simulator passes DC Offset value to the AMI model**
   - Back-Channel Interface For Training

5. **Simulator can pass both DQ & DQS waveform to AMI model**

---

**Notes:**
- 100110
- Clock ticks

---

**Diagrams:**
- Channel diagram showing Tx, Rx, TX AMI FFE, TX Analog, RX Analog, RX AMI DFE+ CTLE/VGA, and Post-EQ Waveform.

---

**Key Points:**
- Multiple Tx and Rx in one Simulation
- Calculate Impulse Responses for Rising and Falling Edges
- Correct impulse responses applied based on rising or falling parts of waveform
- DC Offset value passed to AMI model
- Passes both DQ & DQS waveform to AMI model