

# How to obtain buffer impedance from IBIS

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01

MOTIVATION

02

IMPEDANCE CONCEPT

03

IBIS CONTENT

04

OBTAIN IMPEDANCE FROM IBIS

05

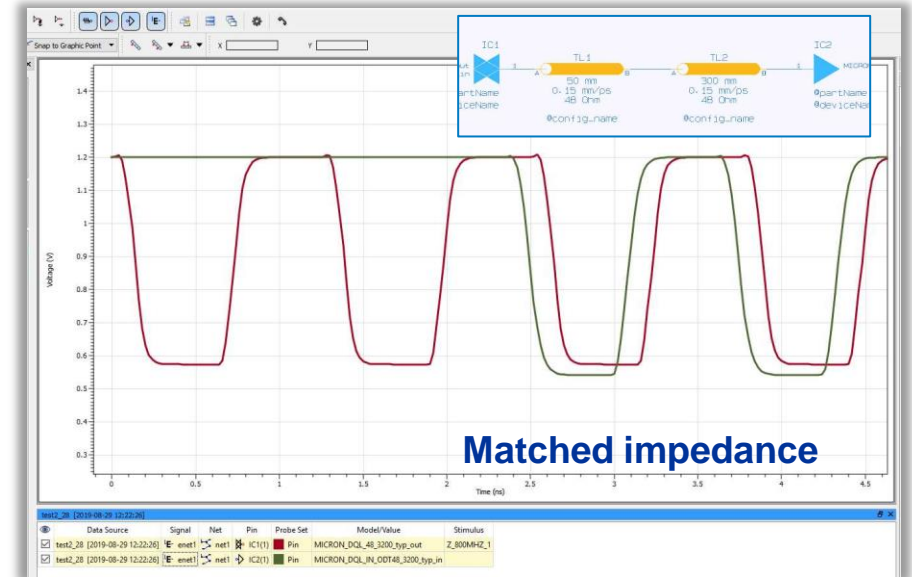
CONCLUSION

## OUTLINE

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# Motivation

- Impedance matching is the biggest task for Signal Integrity engineer and high-speed PCB/PKG designers.
    - Unmatched impedance may cause unpredictable reflection that reduces the signal quality for high-speed circuit design.
  - Interconnects, such as, trace, via, connector, package, etc., are under our radar already.
    - Field Solver helps
  - Interconnect impedance also needs to match buffer Output/Input impedance in order to keep good signal quality
- How to obtain I/O buffer impedance?**



01

MOTIVATION

02

IMPEDANCE CONCEPT

03

IBIS CONTENT

04

OBTAIN IMPEDANCE FROM IBIS

05

CONCLUSION

## OUTLINE

---

# Impedance Concept

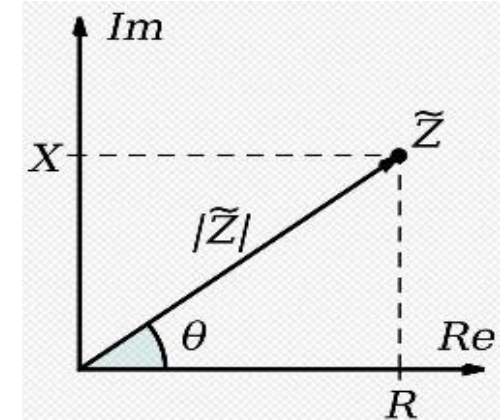
- The impedance of a two-terminal circuit element is represented as a complex quantity  $Z$ . The polar form conveniently captures both magnitude and phase characteristics as

$$Z = |Z|e^{j \arg(Z)}$$

- where the magnitude  $|Z|$  represents the ratio of the voltage difference amplitude to the current amplitude, while the argument  $\arg(Z)$  (commonly given the symbol  $\theta$  gives the phase difference between voltage and current).  $j$  is the imaginary unit and is used instead of  $i$  in this context to avoid confusion with the symbol for electric current.

- In Cartesian form, impedance is defined as  $Z = R + jX$

- where the real part of impedance is the resistance  $R$  and the imaginary part is the reactance  $X$ .

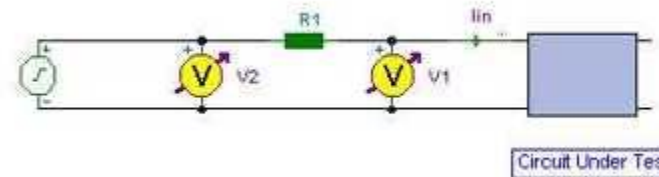


***For a high-speed I/O buffer, the buffer inductance and capacitance are specially designed. It is close to minimum for the reactance  $X$ . So, in this case, the resistance  $R$  is the main factor for impedance matching.***

# Measuring Impedance

## – Input Impedance

- From the AC impedance triangle, the input or output impedance of a two terminal network can be determined by measuring the small signal AC currents and voltages.
  - The voltage is measured across the input terminals and the current measured by inserting the meter in series with the signal generator.



- An easy way to measure small input currents, is to use a fixed resistor, as in the diagram above. Measure the AC voltage at points V1 and V2, then the input current,  $I_{in}$  becomes:

$$I_{in} = \frac{V_2 - V_1}{R_1}$$

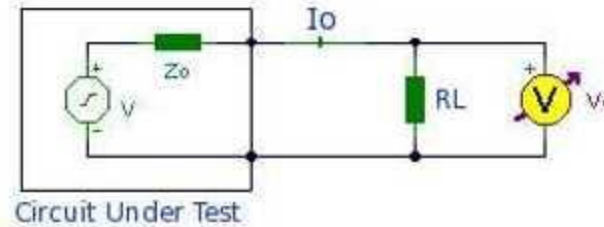
- The input impedance  $Z_{in}$  of the circuit under test is then found by:

$$Z_{in} = \frac{V_1}{I_{in}}$$

# Measuring Impedance

## – Output Impedance

- Output impedance may also be determined using a similar technique. A fixed load resistor is used, and the output voltage is measured first with full load, then without the load.



- $Z_o$  is the internal output impedance of the network to be measured.
- To find the output impedance the output voltage is measured first with no load resistor, then with a fixed load (purely resistive).
- First, the load resistor  $R_L$  is removed and output voltage ( $V$ ) measured and recorded. Then  $R_L$  is placed back in circuit and the output voltage under load ( $V_L$ ). The output impedance,  $Z_o$  is now found by Ohm's Law for AC circuits. As the load is purely resistive  $Z=V/I$ , where "V" is voltage drop across the output impedance:  $(V - V_L)$ , and "I" the output current,  $V_L/R_L$ . Thus:

$$Z_o = \frac{(V - V_L)}{V_L/R_L} = \frac{R_L(V - V_L)}{V_L}$$

01

MOTIVATION

02

IMPEDANCE CONCEPT

03

IBIS CONTENT

04

OBTAIN IMPEDANCE FROM IBIS

05

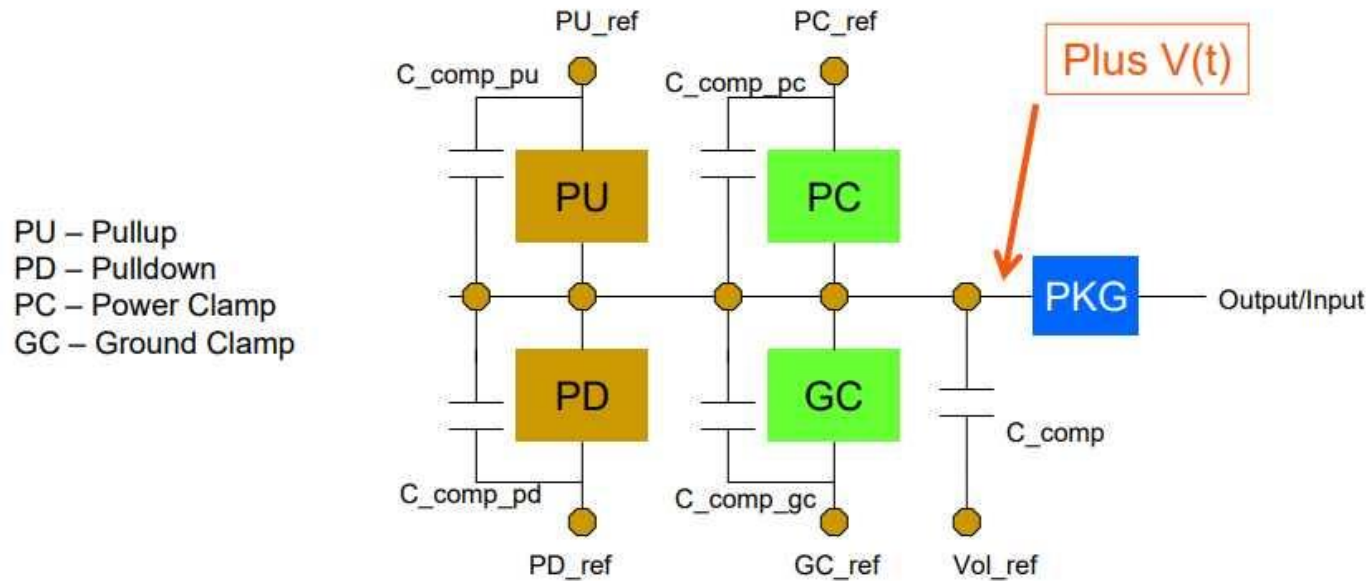
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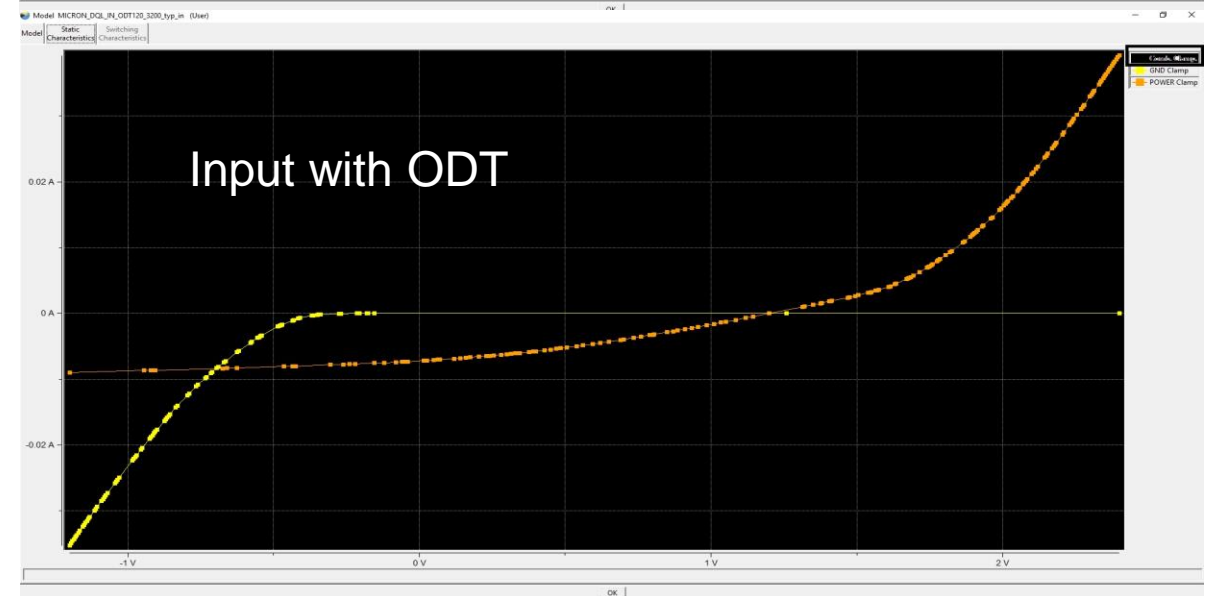
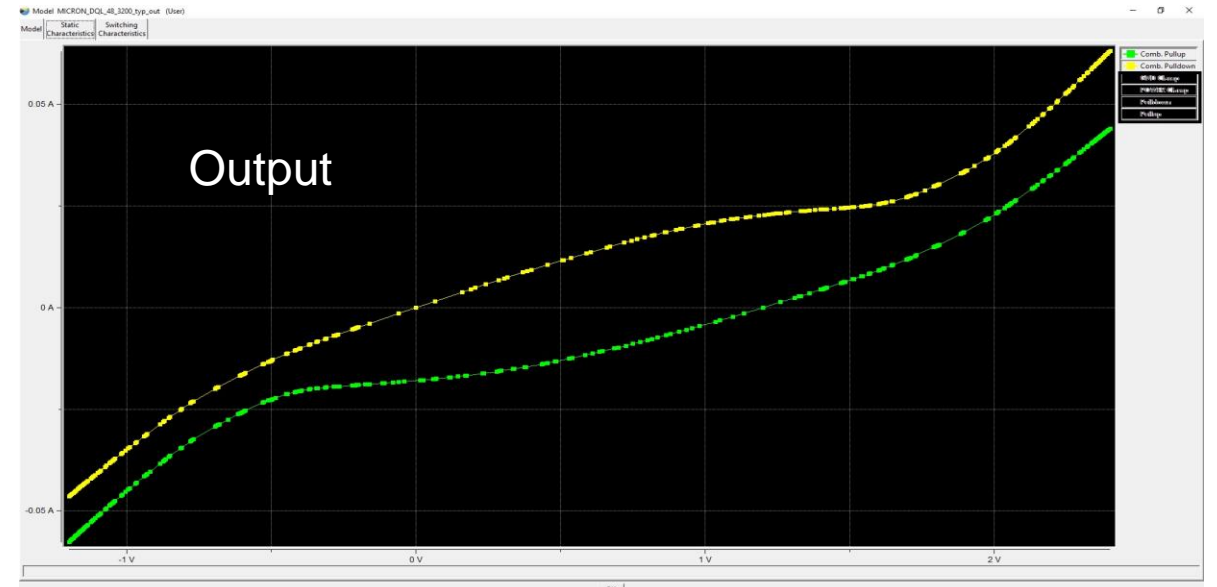
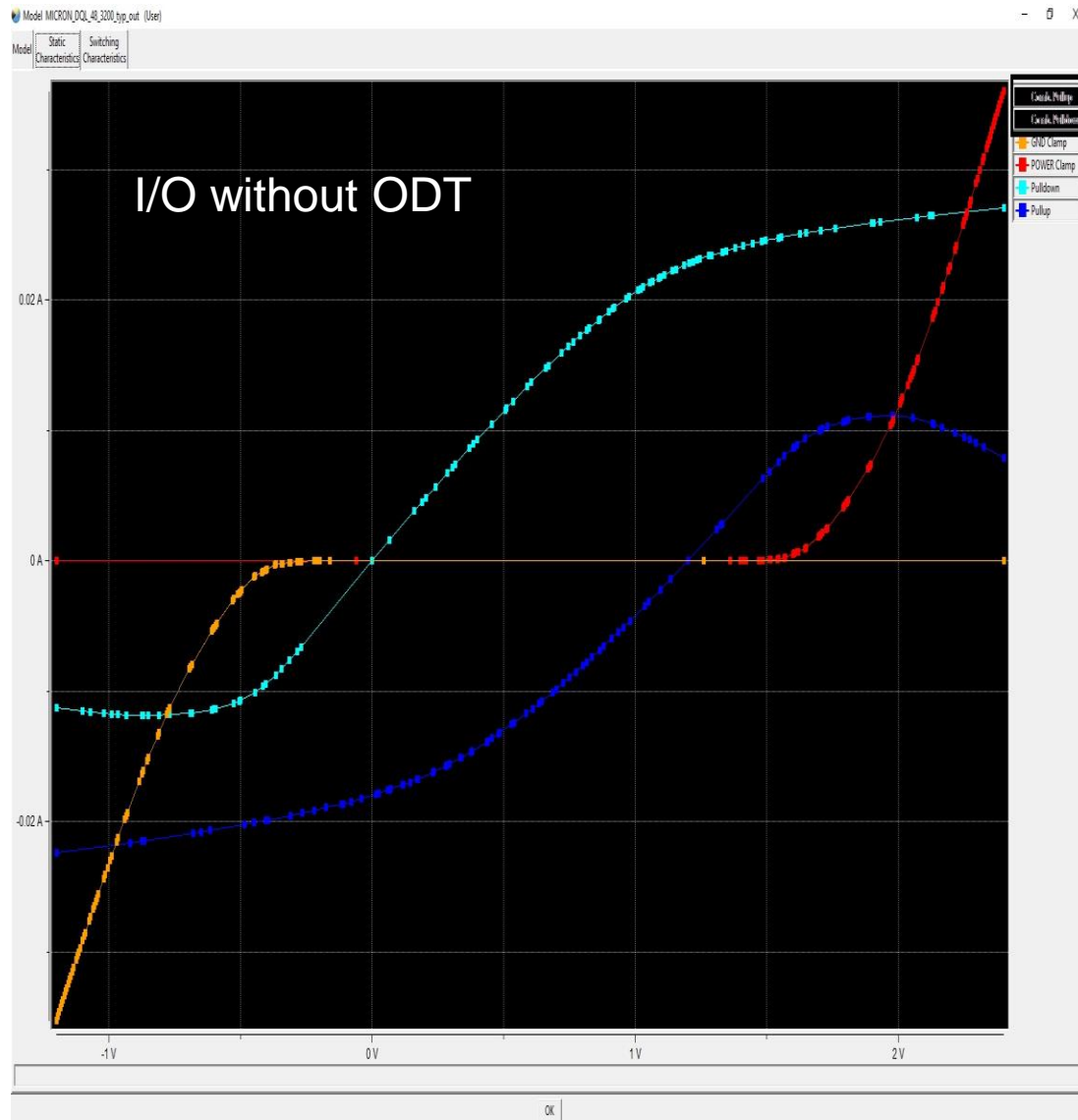
## IBIS Buffer Structure



All curve data are independent with own voltage references

- I/O type
  - 4 static curve data sets
    - Pullup
    - Pulldown
    - Power Clamp
    - Ground Clamp
- Output type
  - 2 static curve data sets
    - Pullup
    - Pulldown
- Input type
  - 2 static curve data sets
    - Power Clamp
    - Ground Clamp

# IBIS model contents



## IBIS MODELING COOKBOOK For IBIS Version 4.0

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The IBIS Open Forum

Approved September 15, 2005

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IBIS Modeling Cookbook

Page 1

### 3.1 Extracting I-V Data from Simulations

The first step to extracting the required I-V tables is understanding the buffer's operation. Analyze the buffer schematic and determine how to put the buffer's output into a logic low, logic high and (if applicable) high impedance (3-state) state. As mentioned above, the schematic should include any ESD or protection diodes. Also, understand the buffer's power supply voltage reference ("Vcc") requirements and connections. The schematic should also indicate if the power clamp and/or ground clamp diode structures are tied to voltage rails (voltage references) different from those used by the pullup and/or pulldown transistors.

#### 3.1.1 Simulation Setup

A typical I-V table simulation setup for an output or I/O buffer is shown in Figure 3.1 below. For this example, the buffer being analyzed is a standard 3-state buffer with a single push-pull output stage. The buffer uses electrostatic discharge protection devices in addition to its parasitic driver diodes. The buffer's clamp supplies are assumed identical to its driver supply (Vcc hereinafter).

Page 12

IBIS Modeling Cookbook

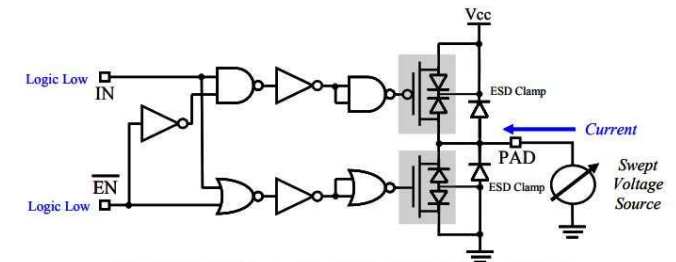


Figure 3.1 – Standard 3-state Buffer (Pulldown I-V Table Extraction Shown)

All measurements are made at the output node (pad) as shown above. Remove all package lead (R<sub>pin</sub>, L<sub>pin</sub>, and C<sub>pin</sub>) parasitics. However, any series resistances present between the pad and the pullup/pulldown transistors should be included (these are not shown in Figure 3.1).

The output buffer is connected to an independent voltage source. Set the buffer's input(s) so that the desired output state (low, high, off) is obtained, then using a DC or "transfer function" analysis sweep the voltage source over the sweep range -Vcc to 2\*Vcc while recording the current into the buffer. An alternative method is to perform a "transient analysis". The voltage source in this case should be linear ramp function driving the output node, slow enough that the current measurement at each time point is effectively DC, without reactive aspects of the design affecting the result. The current flow into the pad is measured (by IBIS convention, current flow into the die pad is positive), as is the voltage at the node with respect to a reference, then the resulting I-T and V-T data is combined into a single I-V table. Note that a transient function analysis may require post-simulation data manipulation.

01

MOTIVATION

02

IMPEDANCE CONCEPT

03

IBIS CONTENT

04

OBTAIN IMPEDANCE FROM IBIS

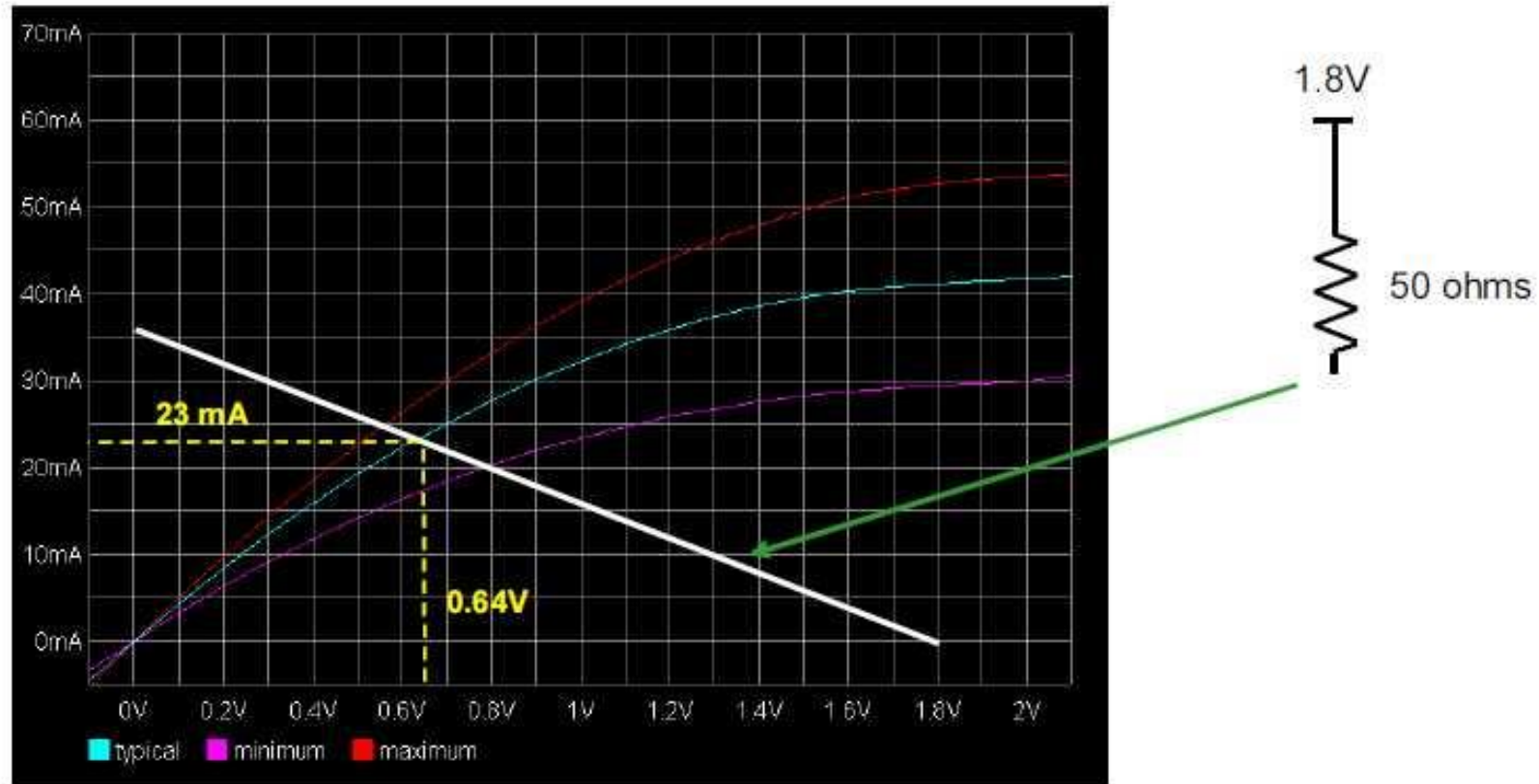
05

CONCLUSION

## OUTLINE

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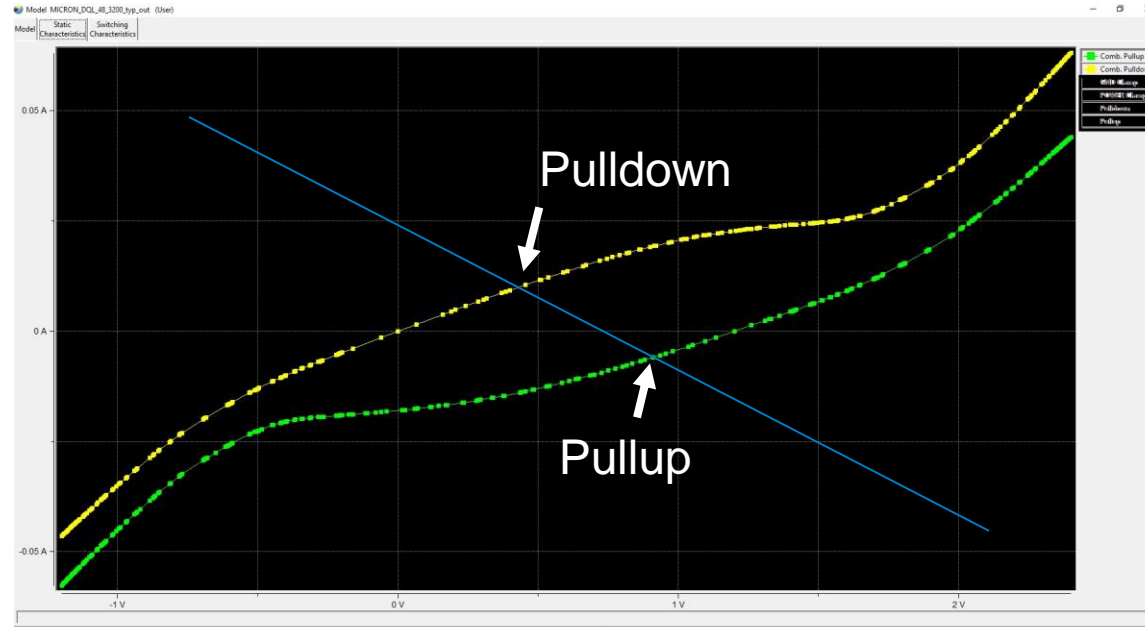
# Obtain impedance from IBIS curves



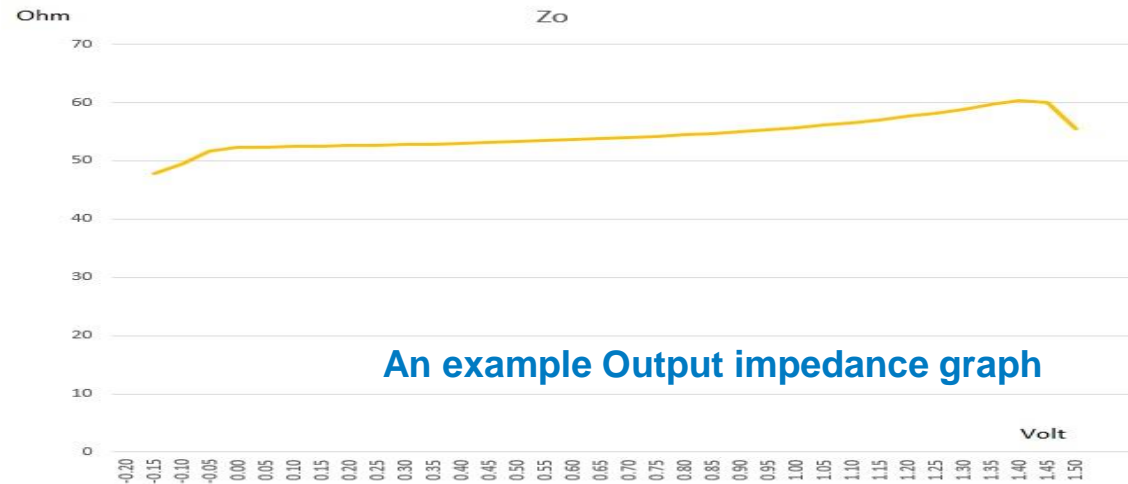
Picture from Todd W. 2005 DAC IBIS Summit

# Obtain Output type buffer impedance from IBIS

- Need to use Combined Pullup/Pulldown curves
  - Pullup + Clamps
  - Pulldown + Clamps
- Load line / Crossing Point
- To avoid numerical errors



$$Z_0 = \frac{dV}{dI} @ R_L$$

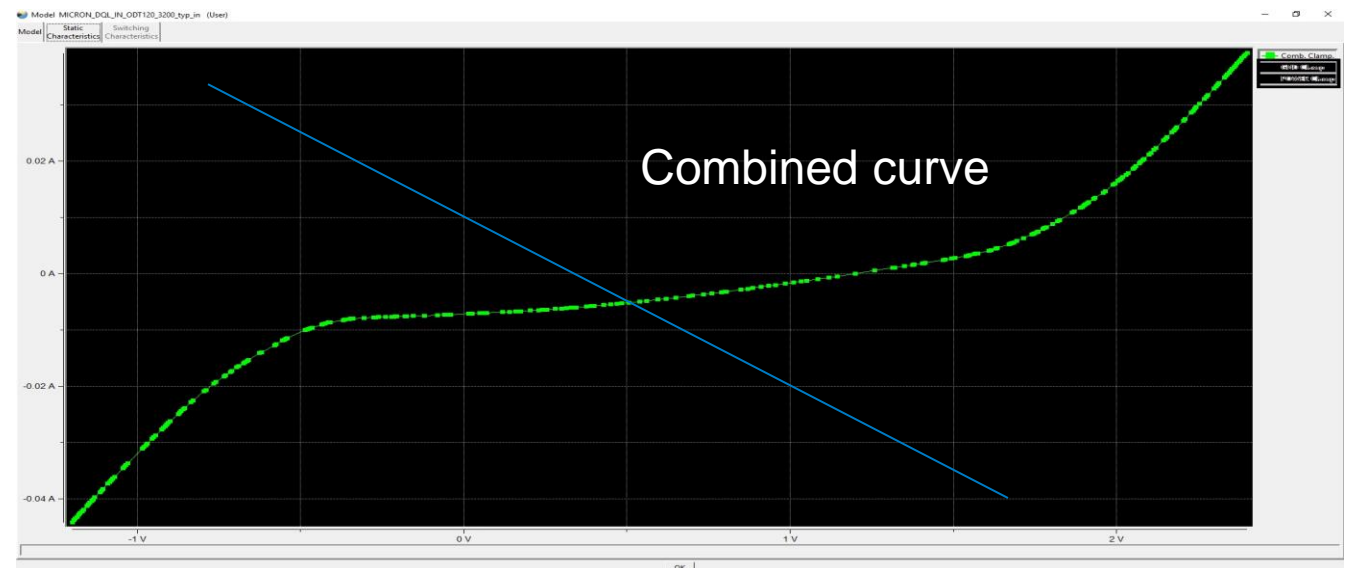
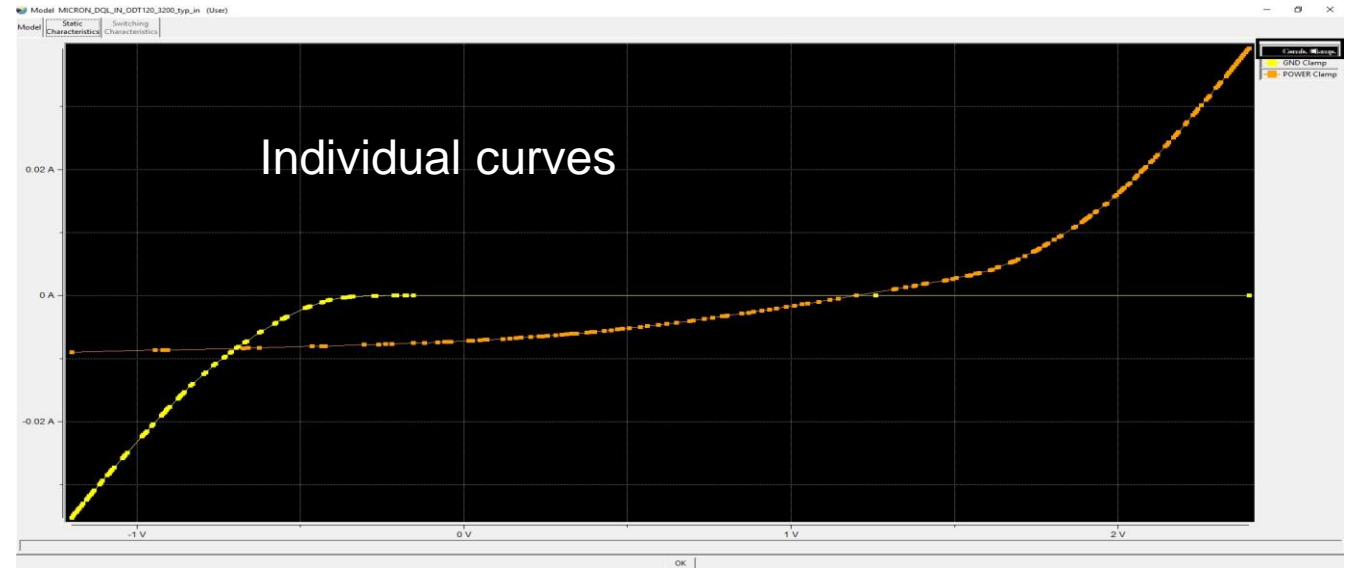
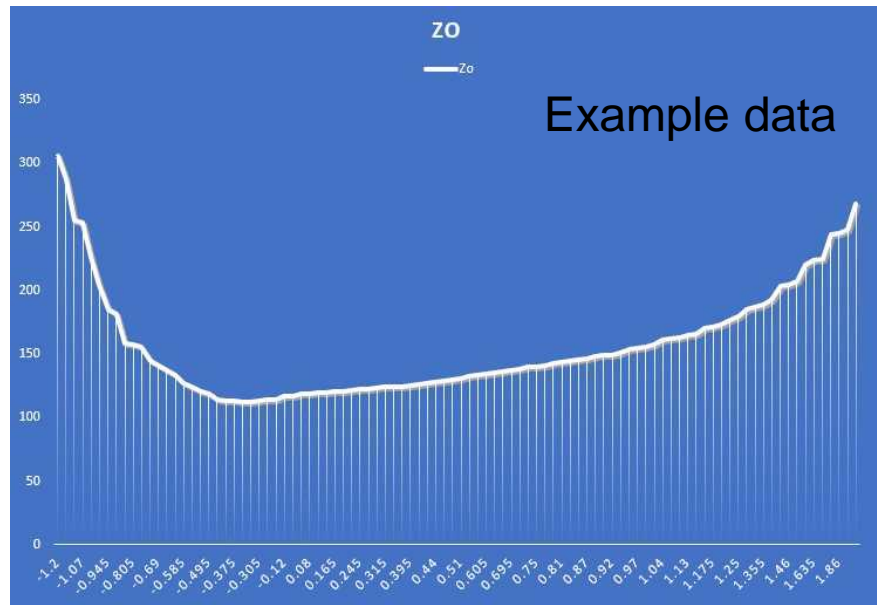


An example Output impedance graph

# Obtain Input type buffer impedance from IBIS

- Use the Combined Clamp data
- To avoid numerical errors

$$Z_0 = \frac{dV}{dI} @ R_L$$



01

MOTIVATION

02

IMPEDANCE CONCEPT

03

IBIS CONTENT

04

OBTAIN IMPEDANCE FROM IBIS

05

CONCLUSION

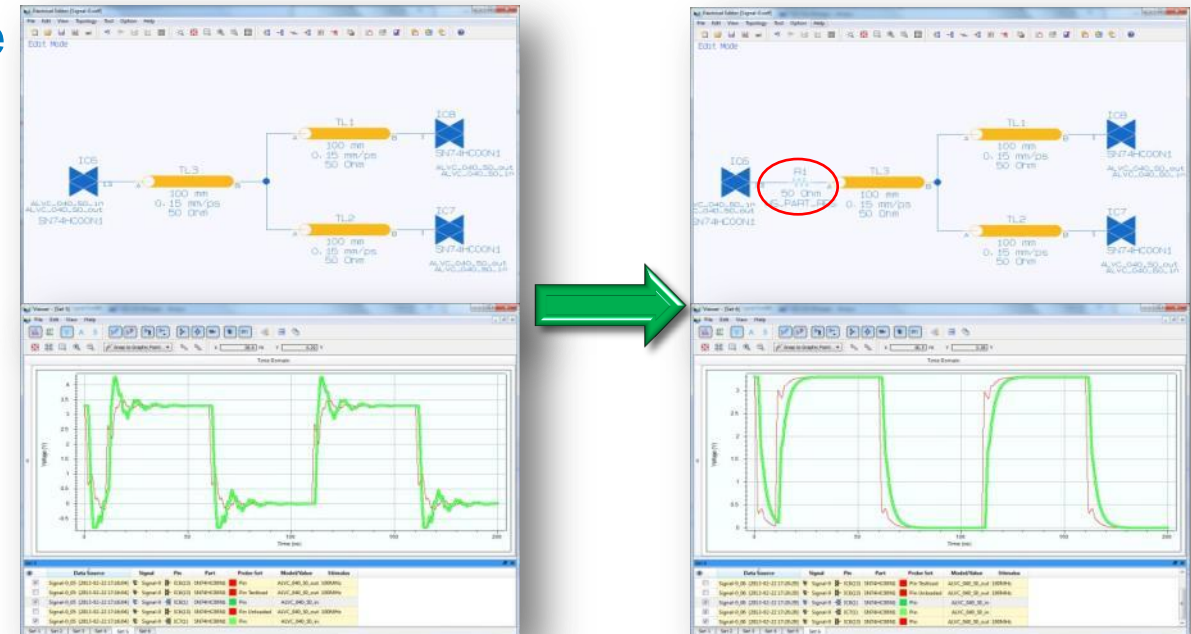
# OUTLINE

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# Conclusion

- Impedance matching is important for high-speed design
  - Not only for interconnect impedance, but also I/O buffer impedance should be counted in the big picture
- The I/O buffer impedance can be obtained from IBIS curve data
  - Obtain buffer driving impedance from IBIS combined Pullup/Pulldown curve data
  - Obtain buffer Input impedance from IBIS combined Power /Ground Clamps curve data
- I/O impedance maybe vary for different loads



The background is a deep blue with various technical illustrations. On the left, there's a faint image of a printed circuit board (PCB) with various components and traces. On the right, there's a glowing network diagram with nodes and connecting lines, some highlighted in a lighter blue. The overall aesthetic is futuristic and technological.

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