IBIS Chair's Report

Randy Wolff

Micron Technology

Chair, IBIS Open Forum

2019 Asian IBIS Summits

Shanghai, China

November 1, 2019

http://www.ibis.org/

26 IBIS Members

Number of Members by Year
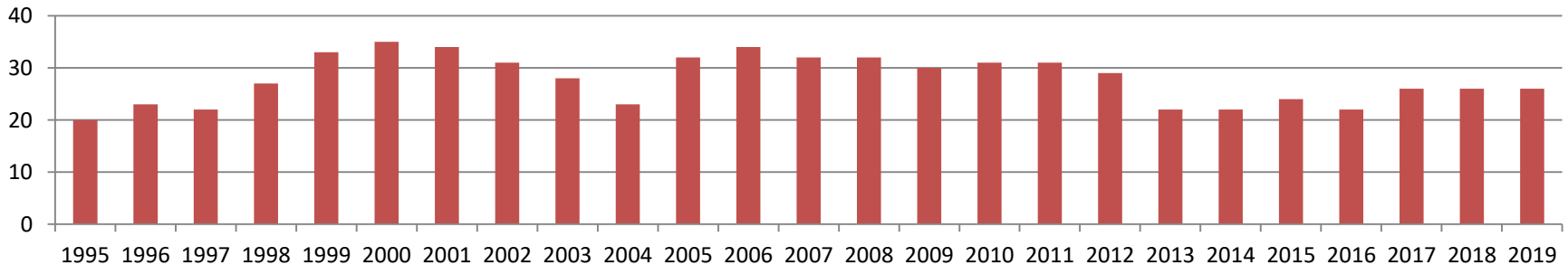
IBIS Officers 2019-2020

Chair: *Randy Wolff, Micron Technology*

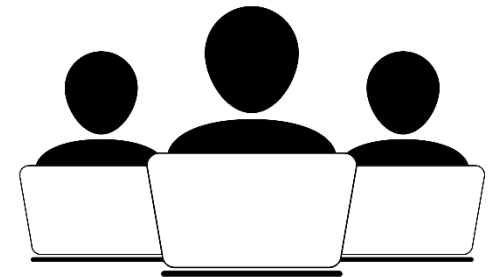Vice-Chair: *Lance Wang, Zuken USA*

Secretary: *Curtis Clark, ANSYS*
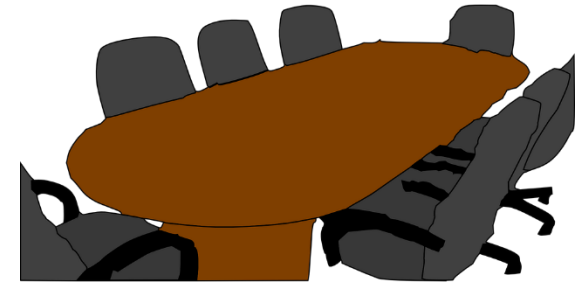
Treasurer: *Bob Ross, Teraspeed Labs*

Librarian: *Anders Ekholm, Ericsson*

Postmaster: *Mike LaBonte, SiSoft (MathWorks)*

Webmaster: *Steve Parker, GlobalFoundries*

IBIS Meetings

- Weekly teleconferences
  - Quality Task Group (Tuesdays)
  - Advanced Technology Modeling Task Group (Tuesdays)
  - Interconnect Task Group (Wednesdays)
  - Editorial Task Group (some Fridays)
- IBIS Open Forum teleconference every 3 weeks
  - 502 meetings so far
- IBIS Summit meetings: DesignCon, IEEE SPI, Shanghai, Taipei, Tokyo

SAE ITC

- SAE Industry Technologies Consortia is the parent organization of the IBIS Open Forum

- IBIS is assisted by SAE employees José Godoy, Phyllis Gross, Laurie Strom

- SAE ITC provides financial, legal, and other services

- http://www.sae-itc.org/

Task Groups

- Interconnect Task Group
  - Chair: Michael Mirmak, Intel
  - http://ibis.org/interconn_wip/
  - Develop on-die/package/module/connector interconnect modeling BIRDs
- Advanced Technology Modeling Task Group
  - Chair: Arpad Muranyi, Mentor, A Siemens Business
  - http://ibis.org/atm_wip/
  - Develop most other technical BIRDs
- Quality Task Group
  - Chair: Mike LaBonte, SiSoft (MathWorks)
  - http://ibis.org/quality_wip/
  - Oversee IBISCHK parser testing and development
- Editorial Task Group
  - Chair: Michael Mirmak, Intel
  - http://ibis.org/editorial_wip/
  - Produce IBIS Specification documents

BIRD = Buffer Issue Resolution Document

IBIS Milestones

I/O Buffer Information Specification

- 1993-1994 **IBIS 1.0-2.1**:
  - Behavioral buffer model (fast simulation)
  - Component pin map (easy EDA import)
- 1997-1999 **IBIS 3.0-3.2**:
  - Package models
  - Electrical Board Description (EBD)
  - Dynamic buffers
- 2002-2006 **IBIS 4.0-4.2**:
  - Receiver models
  - AMS languages
- 2007-2012 **IBIS 5.0-5.1**:
  - IBIS-AMI SerDes models
  - Power aware
- 2013-2015 **IBIS 6.0-6.1**:
  - PAM4 multi-level signaling
  - Power delivery package models
- 2019 **IBIS 7.0**:
  - Back-channel support
  - Interconnect modeling using IBIS-ISS and Touchstone

Other Work

- 1995: **ANSI/EIA-656**
  - IBIS 2.1
- 1999: **ANSI/EIA-656-A**
  - IBIS 3.2
- 2001: **IEC 62014-1**
  - IBIS 3.2
- 2003: **ICM 1.0**
  - Interconnect Model Specification
- 2006: **ANSI/EIA-656-B**
  - IBIS 4.2
- 2009: **Touchstone 2.0**
- 2011: **IBIS-ISS 1.0**
  - Interconnect SPICE Subcircuit specification

IBIS Version Development
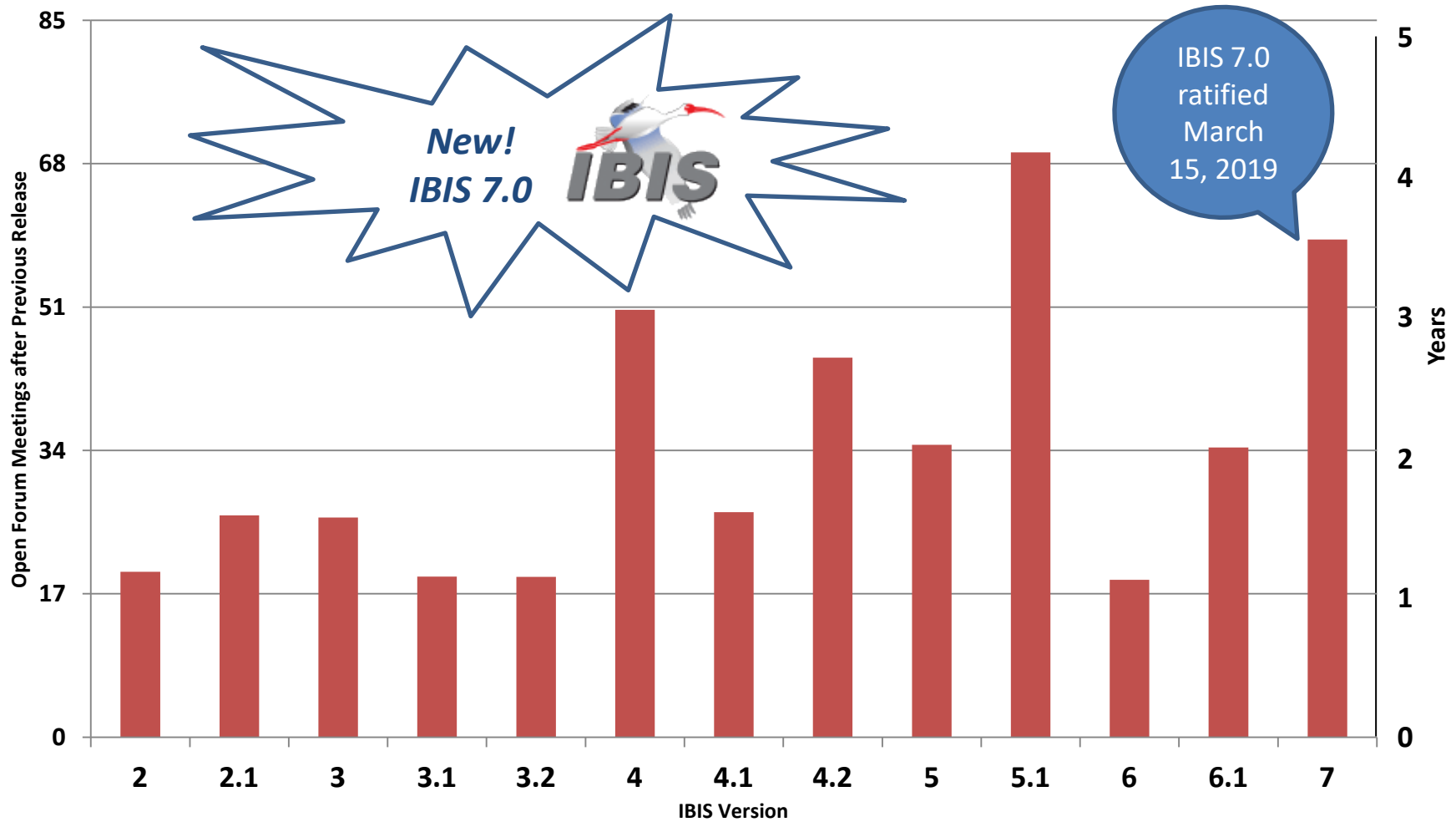
IBISCHK7 Version 7.0.0

- Executables available at www.ibis.org/ibischk7/
  - Interconnect Model syntax
  - Subdirectory references
  - Bus_label definitions
  - Etc.

- Contact treasurer@ibis.org for Source Code License purchase ($3,000)

Beyond IBIS 7.0

- Currently 5 BIRDs in discussion
  - 2 about redriver flow (BIRD166.4, BIRD190)
  - 1 editorial (BIRD181.1)
  - 1 to support single-ended IBIS-AMI (BIRD197.4)
  - 1 for on-die PDN modeling (BIRD198)
- EBD update supporting IBIS-ISS and Touchstone
  - Improved module and multi-chip package modeling
- BIRD200 approved: C_comp model supporting IBIS-ISS and Touchstone
- BIRD195.1 approved: [Rgnd] and [Rpower] for IBIS-AMI Input models
- What other new ideas do you have for IBIS?

What Else Could IBIS Be Used For?

- IBIS is nominally about I/O buffers, used to:
  - Solve signal quality problems like loss, inter-symbol interference (ISI) and crosstalk
  - Generate waveforms used in timing analysis
- But engineers also:
  - Insure proper timing between pins
  - Insure sufficient power distribution
  - Include optical links in analyses
  - Analyze channel operating margin (COM), forward error correction (FEC), etc.
  - Comply with any other new requirements posed by JEDEC, etc.

- What other data might IBIS formats convey?

New Directions for IBIS?

- IBIS VRM models

- IBIS chip power models

- IBIS timing models

- IBIS waveform analysis language

- Data probability distributions
  (or at least more than 3 corners)

- IBIS-ISS [Test Load], external [Test Data]

- Optical Model_type(s) for
  Vertical Cavity Surface Emitting Laser (VCSEL), etc.
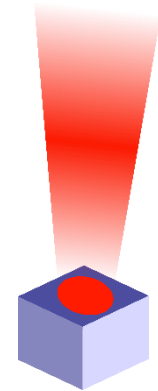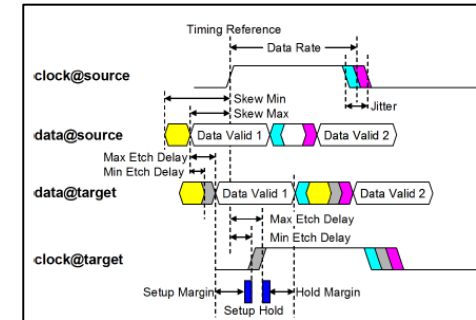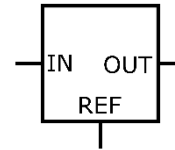
Submitting Your Idea – BIRD Process

- BIRD – Buffer Issue Resolution Document
  - Official method for submitting a proposed change to the IBIS specification
- BIRD Template found on IBIS website
  - Standardized method to describe your idea
- Submit BIRD to chair@ibis.org
- BIRDs discussed in Open Forum meetings
  - Eventual vote by members for approval
- Idea not ready for an official BIRD?
  - Join an IBIS Task Group meeting for technical discussion

BIRD Link on IBIS Website

Link to BIRDs webpage

BIRD Template Link on the BIRD Webpage

Buffer Issue Resolution Documents (BIRD)

To submit a BIRD to the IBIS Open Forum, please use the *BIRD Template, Rev. 1.3*.

ID#	Issue Title	Requester	Date Submitted	Date Accepted	Supporting Version
200	C_comp Model Using IBIS-ISS or Touchstone	Randy Wolff, Micron Technology, Inc. Walter Katz, Signal Integrity Software, Inc.	July 9, 2019	September 27, 2019	
199	Fix Rx_Receiver_Sensitivity Inconsistencies	Arpad Muranyi, Mentor a Siemens Business	March 19, 2019	June 7, 2019	
198	Keyword additions for On Die PDN (Power Distribution Network) Modeling	Kazuki Murata; Ricoh Co., Ltd.; Miyoko Goto; Ricoh Co., Ltd.; Kazuyuki Sakata; Renesas Electronics Corporation; Kazunori Yamada; Renesas Electronics Corporation; Kouji Ichikawa; Denso Corporation; Atsushi Tomishima; Toshiba Electronic Devices & Storage Corporation; Takashi Hasegawa; Sony LSI Design Inc.; Koichi Seko, Panasonic Industrial Devices Systems and Technology Co., Ltd.; Toshiki Kanamoto; Hirosaki University Megumi Ono; Socionext Inc.	March 11, 2019		
197.4	New AMI Reserved Parameters DC_Offset and NRZ_Threshold	Walter Katz, SiSoft, Ambrish Varma, Cadence Design Systems, Randy Wolff, Micron Technology, Justin Butterfield, Micron Technology, Fangyi Rao, Keysight Technologies	November 27, 2018, December 4, 2018, January 15, 2019, June 25, 2019, July 23, 2019		
196.1	Prohibit Periods at the End of File Names	Arpad Muranyi, Mentor Graphics, A Siemens Business	September 25, 2018, October 12, 2018	October 12, 2018	7.0
195.1	Enabling [Rgnd] and [Rpower] Keywords for Input Models	Michael Mirmak, Intel Corp.	June 19, 2018, June 29, 2018	August 31, 2018	

[Thank You]

IBIS Open Forum:
Web: http://www.ibis.org
Email: ibis-info@freelists.org

We welcome participation by all IBIS model makers, EDA tool vendors, IBIS model users, and interested parties.