

# C-PHY SI SIMULATION WITH IBIS MODEL

---

Bailing Zhang 张百玲  
ANSYS

Asian IBIS Summit  
Shanghai, PRC  
November 1, 2019

# Outline

---

- C-PHY interface instruction
- How to use IBIS model to do the C-PHY SI simulation
- Check the simulation result
- Summary

# C-PHY interface instruction

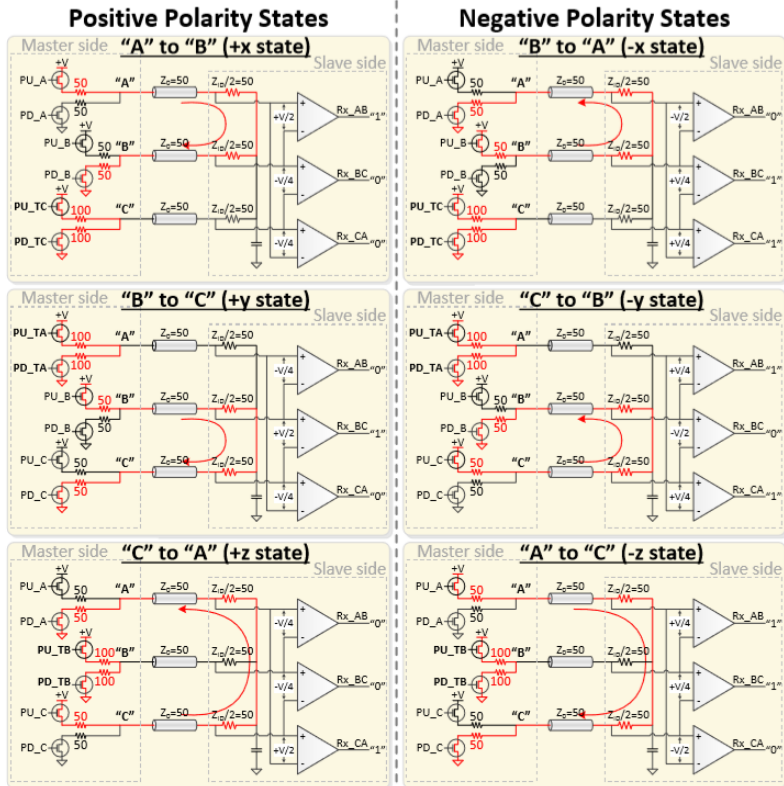


Figure 1 Six Physical Layer Wire States of C-PHY Encoding, Nominal Values Shown

The MIPI C-PHY uses a 3-phase symbol. Each symbol provides 2.28 bits, and transmits data on a 3-wire path with 3-state signals. Each 3-state symbol includes an embedded clock. C-PHY signals are single ended, and each has 3 levels. They are represented by lineA, lineB, and lineC. At any given timing point, no two signals will be at the same voltage level. The receiver uses differential sensing to produce four voltage levels: strong 1, weak 1, strong 0, and weak 0. However, the output of the receiver is logical 1 or logical 0.

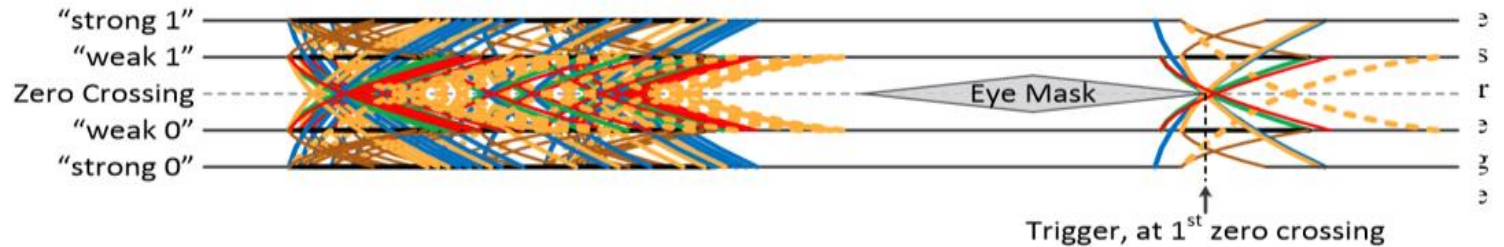
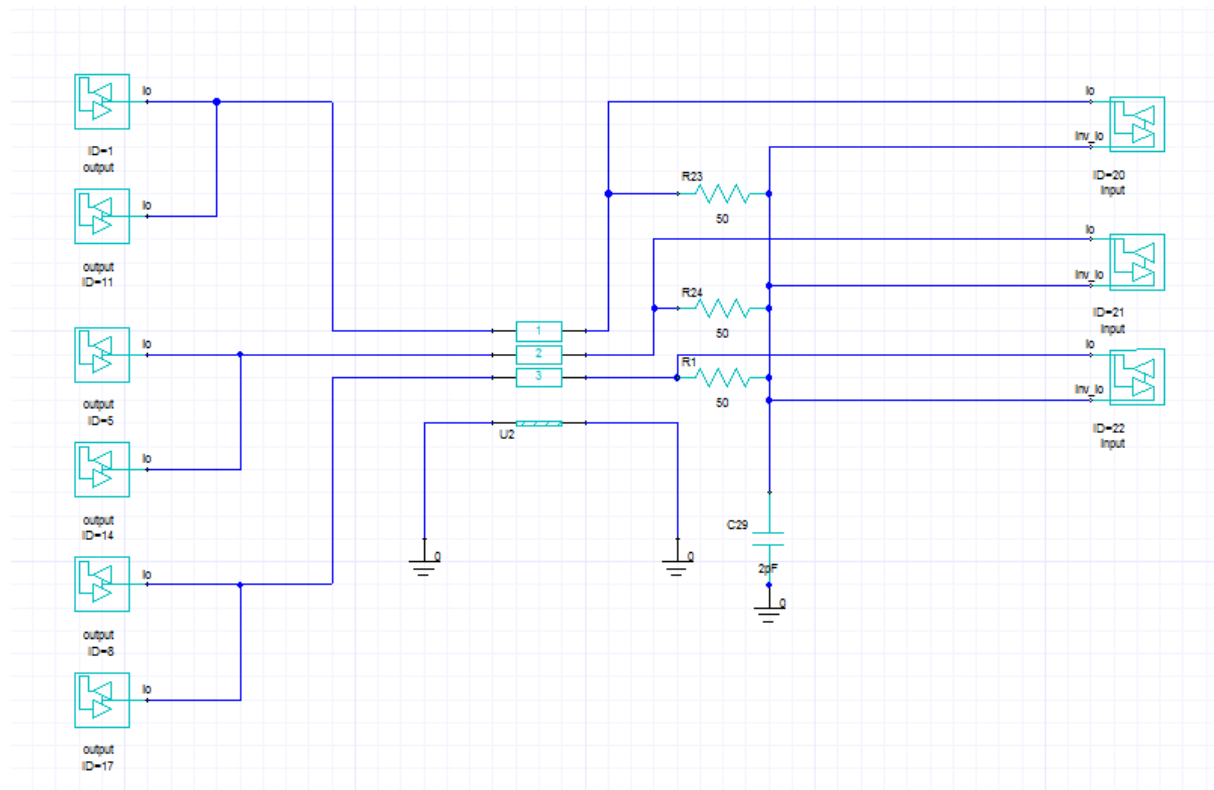


Figure 58 C-PHY Eye Pattern Example, Triggered Eye

# How to use IBIS model do the C-PHY SI simulation



MIPI C-PHY using IBIS I/O drivers and differential receivers

# Check the simulation result

$$V_{DIF\_RX\_AB}(t) = V_A(t) - V_B(t); V_{DIF\_RX\_BC}(t) = V_B(t) - V_C(t); V_{DIF\_RX\_CA}(t) = V_C(t) - V_A(t);$$

$$V_{DIF\_RX\_MAX} = V_{IHHS\_MAX} - V_{ILHS\_MIN}$$

Version 1.0  
05-Aug-2014

2.5Gbps  
1U=400ps

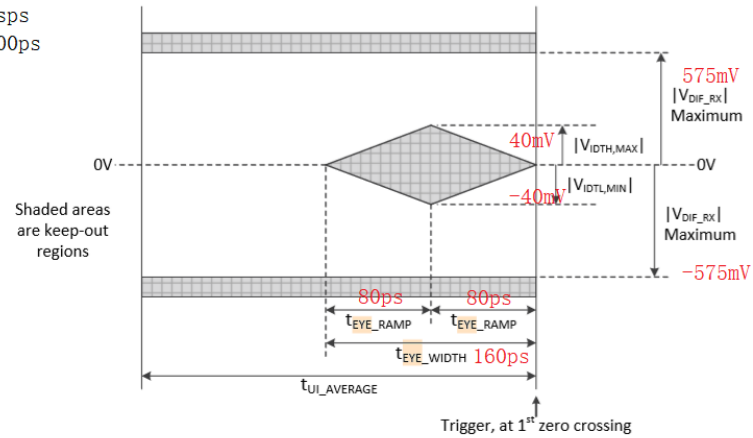
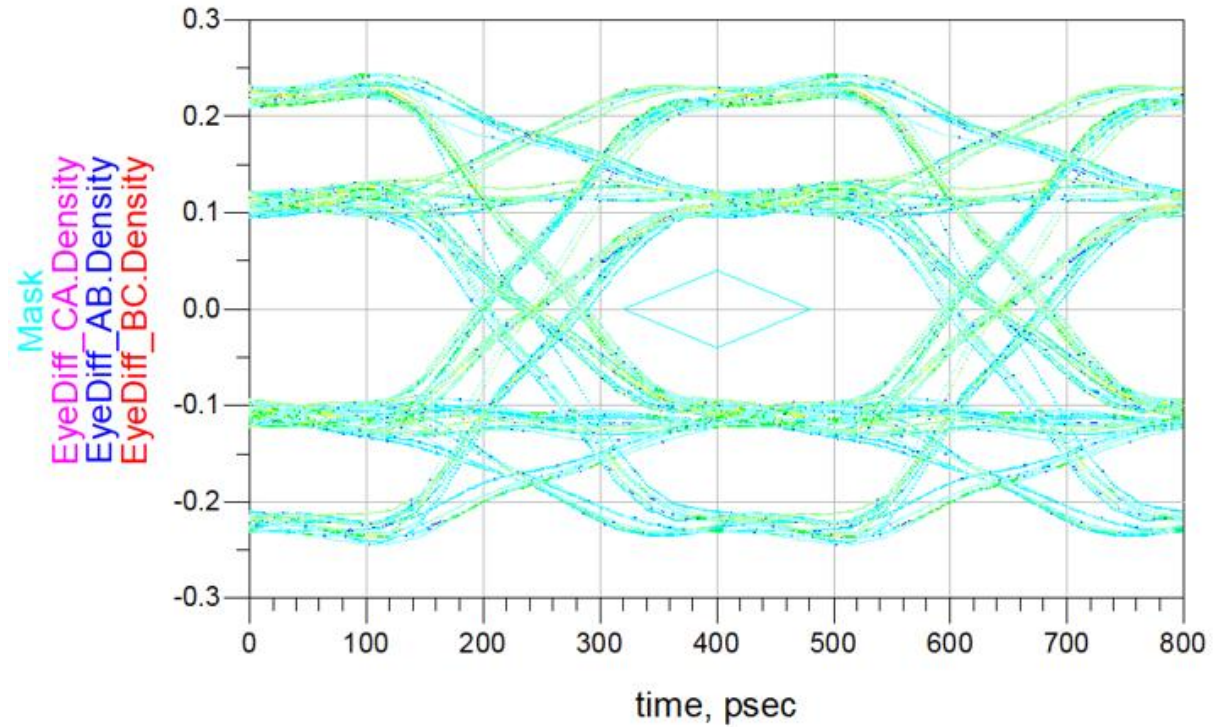


Figure 59 C-PHY Receiver Eye Diagram

Table 34 Receiver Timing Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
t <sub>EYE_RAMP</sub>	Eye ramp time at the receiver	0.2			UI	
t <sub>EYE_WIDTH</sub>	Eye width at the receiver	0.4			UI	
t <sub>UI_AVERAGE</sub>	UI average		U <sub>INST</sub>			



# Summary

---

Use IBIS model to do the C-PHY SI simulation is very convenient, accurate and fast.

From the simulation we can best evaluate the quality of C-PHY signal and make the product successful.

---

**Thank you**