WELCOME FROM RANDY WOLFF, IBIS OPEN FORUM

Ladies and Gentlemen,

As chair of the IBIS Open Forum it is my pleasure to welcome you to the 2019 Asian IBIS Summit in Taipei and to thank you for your presentations and participation. We are grateful to our sponsors ANSYS, Cadence Design Systems, and Synopsys for making this event possible.

Since 1993 IBIS has provided the digital electronics industry with specifications to make signal, timing, and power integrity analyses much easier and faster. With the introduction of IBIS-AMI in 2008, the IBIS community generated new energy for high speed electronic design. IBIS is now known by engineers worldwide and is a required technology for many applications. IBIS Version 7.0 was released in 2019, adding enhancements for IBIS-AMI and supporting advanced interconnect modeling.

Support for IBIS in Asia has been strong, and the IBIS Open Forum looks forward to continued innovation and contributions from technology companies in Asia. Thank you!

Randy Wolff
Micron Technology
Chair, IBIS Open Forum

WELCOME FROM RANDY WOLFF, IBIS OPEN FORUM

女士們先生們，

作為 IBIS 開放論壇的主席，我很高興地歡迎您參加 2018 年在台北舉辦的亞洲 IBIS 峰會，感謝您的介紹和參與。我們非常感謝我們的讚助商 ANSYS, Cadence Design Systems, 和 Synopsys，以使這一事件成為可能。

自 1993 年以來，IBIS 為數字電子行業提供了使信號，時序和電源完整性分析更容易和更快速的規範。隨著 IBIS-AMI 在 2008 年的推出，IBIS 社區為高速電子設計創造了新的能量。 IBIS 現在已被世界各地的工程師所了解，是許多應用所需的技術。2019 年，新的 IBIS 7.0 版本包含了更多的 IBIS-AMI 模型和互联接口模型的定义及提升。

IBIS 在亞洲的支持一直很強，IBIS 開放論壇期待著亞洲技術公司的不斷創新和貢獻。

谢谢!

Randy Wolff (兰迪·沃尔夫)
Micron Technology 公司
主席，IBIS 开放论坛

AGENDA AND ORDER OF THE PRESENTATIONS

(The actual agenda might be modified)

I B I S S U M M I T M E E T I N G A G E N D A

9:00 **SIGN IN**
- Vendor Tables Open at 8:30

9:30 **WELCOME**
- Randy Wolff (Chair, IBIS Open Forum)
  (Micron Technology, USA)

9:45 **IBIS Chair's Report** **5**
Randy Wolff (Micron Technology, USA)

10:05 **Introducing IBIS Version 7.0** **13**
Michael Mirmak*, Randy Wolff**
(*Intel Corporation, **Micron Technology; USA)
[Presented by Randy Wolff (Micron Technology, USA)]

10:30 **BREAK** (Refreshments and Vendor Tables)

10:50 **How to Obtain Buffer Impedance from IBIS** **20**
Lance Wang (Zuken, USA)

11:20 **IBIS-AMI & COM Co-design for 25G Serdes** **29**
Nan Hou*, Amy Zhang*, Guohua Wang*, David Zhang**,
Anders Ekholm** (Ericsson, *China, **Sweden)
[Presented by Anders Ekholm (Ericsson, Sweden)]

12:00 **FREE BUFFET LUNCH** (Hosted by Sponsors)
- Vendor Tables

13:30 **Innovations in DDR Memory Simulation** **44**
Stephen Slater (Keysight Technologies, USA)
[Presented by Nash Tu (Keysight Technologies, Taiwan)]

14:10 **Channel Simulation Over DDR4/5 and Above** **56**
Kumar Keshavan*, Ambrish Varma*, Ken Willis*, Skipper Liang**
(Cadence Design Systems, (*USA, **Taiwan)
[Presented by Skipper Liang (Cadence Design Systems, Taiwan)]

14:40 **IBIS File Format Links** **68**
Bob Ross (Teraspeed Labs, USA)
[Presented by Randy Wolff (Micron Technology, USA)]

15:10 **CONCLUDING ITEMS**

15:15 **END OF IBIS SUMMIT**

15:15 **BREAK** (Refreshments and Vendor Tables)

15:35 **VENDOR PRESENTATIONS, MODERATOR**
- Lance Wang (Vice-chair, IBIS Open Forum)
  (Zuken, USA)

16:50 **END OF VENDOR PRESENTATONS**

IBIS Chair's Report

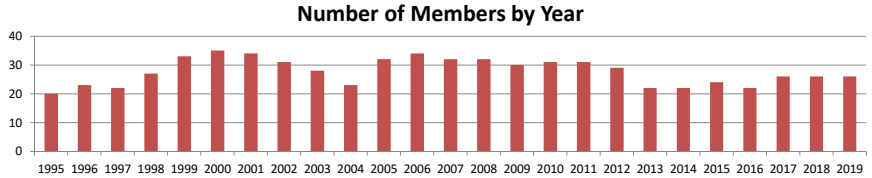
Randy Wolff
Micron Technology
Chair, IBIS Open Forum

2019 Asian IBIS Summits
Taipei, Taiwan
November 4, 2019

http://www.ibis.org/

Organization

26 IBIS Members



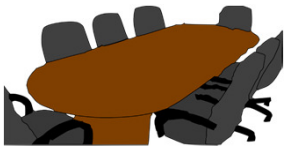
Organization

IBIS Officers 2019-2020

Chair:	*Randy Wolff, Micron Technology*
Vice-Chair:	*Lance Wang, Zuken USA*
Secretary:	*Curtis Clark, ANSYS*
Treasurer:	*Bob Ross, Teraspeed Labs*
Librarian:	*Anders Ekholm, Ericsson*
Postmaster:	*Mike LaBonte, SiSoft (MathWorks)*
Webmaster:	*Steve Parker, GlobalFoundries*

Organization

IBIS Meetings



- Weekly teleconferences
  - Quality Task Group (Tuesdays)
  - Advanced Technology Modeling Task Group (Tuesdays)
  - Interconnect Task Group (Wednesdays)
  - Editorial Task Group (some Fridays)
- IBIS Open Forum teleconference every 3 weeks
  - 502 meetings so far
- IBIS Summit meetings: DesignCon, IEEE SPI, Shanghai, Taipei, Tokyo

Organization

SAE ITC

- SAE Industry Technologies Consortia is the parent organization of the IBIS Open Forum
- IBIS is assisted by SAE employees José Godoy, Phyllis Gross, Laurie Strom
- SAE ITC provides financial, legal, and other services
- http://www.sae-itc.org/

Organization

Task Groups

- Interconnect Task Group
  - Chair: Michael Mirmak, Intel
  - http://ibis.org/interconn_wip/
  - Develop on-die/package/module/connector interconnect modeling BIRDs
- Advanced Technology Modeling Task Group
  - Chair: Arpad Muranyi, Mentor, A Siemens Business
  - http://ibis.org/atm_wip/
  - Develop most other technical BIRDs
- Quality Task Group
  - Chair: Mike LaBonte, SiSoft (MathWorks)
  - http://ibis.org/quality_wip/
  - Oversee IBISCHK parser testing and development
- Editorial Task Group
  - Chair: Michael Mirmak, Intel
  - http://ibis.org/editorial_wip/
  - Produce IBIS Specification documents

BIRD = Buffer Issue Resolution Document

Specification Development

IBIS Milestones

I/O Buffer Information Specification

- 1993-1994 **IBIS 1.0-2.1**:
  - Behavioral buffer model (fast simulation)
  - Component pin map (easy EDA import)
- 1997-1999 **IBIS 3.0-3.2**:
  - Package models
  - Electrical Board Description (EBD)
  - Dynamic buffers
- 2002-2006 **IBIS 4.0-4.2**:
  - Receiver models
  - AMS languages
- 2007-2012 **IBIS 5.0-5.1**:
  - IBIS-AMI SerDes models
  - Power aware
- 2013-2015 **IBIS 6.0-6.1**:
  - PAM4 multi-level signaling
  - Power delivery package models
- 2019 **IBIS 7.0**:
  - Back-channel support
  - Interconnect modeling using IBIS-ISS and Touchstone

Other Work

- 1995: **ANSI/EIA-656**
  - IBIS 2.1
- 1999: **ANSI/EIA-656-A**
  - IBIS 3.2
- 2001: **IEC 62014-1**
  - IBIS 3.2
- 2003: **ICM 1.0**
  - Interconnect Model Specification
- 2006: **ANSI/EIA-656-B**
  - IBIS 4.2
- 2009: **Touchstone 2.0**
- 2011: **IBIS-ISS 1.0**
  - Interconnect SPICE Subcircuit specification

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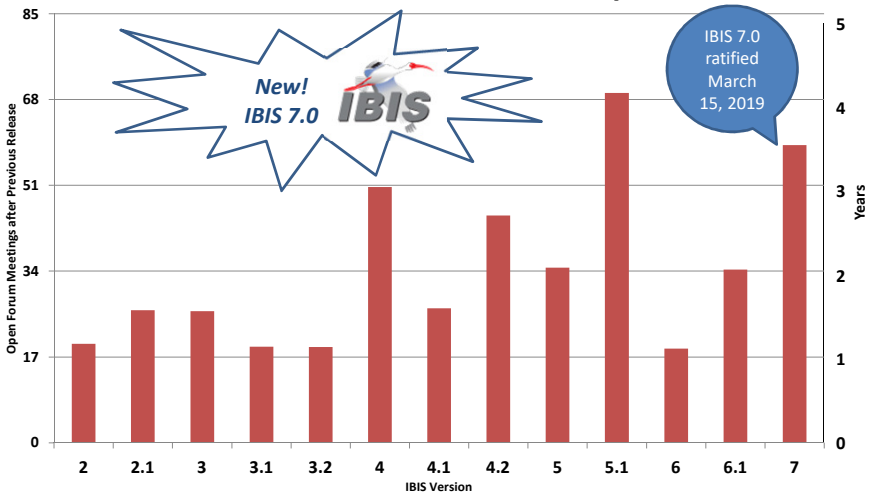
Specification Development

IBIS Version Development



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Specification Development

IBISCHK7 Version 7.0.0

- Executables available at www.ibis.org/ibischk7/
  - Interconnect Model syntax
  - Subdirectory references
  - Bus_label definitions
  - Etc.
- Contact treasurer@ibis.org for Source Code License purchase ($3,000)

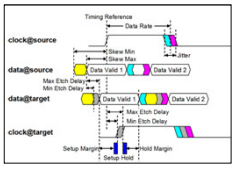
Beyond IBIS 7.0

- Currently 5 BIRDs in discussion
  - 2 about redriver flow (BIRD166.4, BIRD190)
  - 1 editorial (BIRD181.1)
  - 1 to support single-ended IBIS-AMI (BIRD197.4)
  - 1 for on-die PDN modeling (BIRD198)
- EBD update supporting IBIS-ISS and Touchstone
  - Improved module and multi-chip package modeling
- BIRD200 approved: C_comp model supporting IBIS-ISS and Touchstone
- BIRD195.1 approved: [Rgnd] and [Rpower] for IBIS-AMI Input models
- What other new ideas do you have for IBIS?

What Else Could IBIS Be Used For?

- IBIS is nominally about I/O buffers, used to:
  - Solve signal quality problems like loss, inter-symbol interference (ISI) and crosstalk
  - Generate waveforms used in timing analysis
- But engineers also:
  - Insure proper timing between pins
  - Insure sufficient power distribution
  - Include optical links in analyses
  - Analyze channel operating margin (COM), forward error correction (FEC), etc.
  - Comply with any other new requirements posed by JEDEC, etc.
- What other data might IBIS formats convey?

New Directions for IBIS?

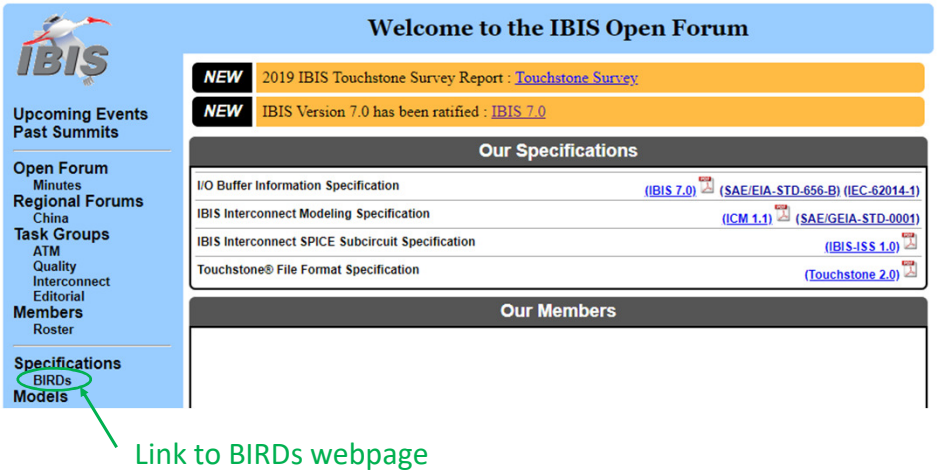


- IBIS VRM models
- IBIS chip power models
- IBIS timing models
- IBIS waveform analysis language
- Data probability distributions (or at least more than 3 corners)
- IBIS-ISS [Test Load], external [Test Data]
- Optical Model_type(s) for Vertical Cavity Surface Emitting Laser (VCSEL), etc.

Submitting Your Idea – BIRD Process

- BIRD – Buffer Issue Resolution Document
  - Official method for submitting a proposed change to the IBIS specification
- BIRD Template found on IBIS website
  - Standardized method to describe your idea
- Submit BIRD to chair@ibis.org
- BIRDs discussed in Open Forum meetings
  - Eventual vote by members for approval
- Idea not ready for an official BIRD?
  - Join an IBIS Task Group meeting for technical discussion

BIRD Link on IBIS Website



BIRD Template Link on the BIRD Webpage

Buffer Issue Resolution Documents (BIRD)

To submit a BIRD to the IBIS Open Forum, please use the BIRD Template, Rev. 1.3

ID#	Issue Title	Requester	Date Submitted	Date Accepted	Supporting Version
200	C_comp Model Using IBIS-ISS or Touchstone	Randy Wolff, Micron Technology, Inc. Walter Katz, Signal Integrity Software, Inc.	July 9, 2019	September 27, 2019	
199	Fix Rx_Receiver_Sensitivity Inconsistencies	Arpad Muranyi, Mentor a Siemens Business	March 19, 2019	June 7, 2019	
198	Keyword additions for On Die PDN (Power Distribution Network) Modeling	Kazuki Murata; Ricoh Co., Ltd.; Miyoko Goto; Ricoh Co., Ltd.; Kazuyuki Sakata; Renesas Electronics Corporation; Kazunori Yamada; Renesas Electronics Corporation; Kouji Ichikawa; Denso Corporation; Atsushi Tomishima; Toshiba Electronic Devices & Storage Corporation; Takashi Hasegawa; Sony LSI Design Inc.; Koichi Seko, Panasonic Industrial Devices Systems and Technology Co., Ltd.; Toshiki Kanamoto; Hirosaki University Megumi Ono; Socionext Inc.	March 11, 2019		
197.4	New AMI Reserved Parameters DC_Offset and NRZ_Threshold	Walter Katz, SiSoft, Ambrish Varma, Cadence Design Systems, Randy Wolff, Micron Technology, Justin Butterfield, Micron Technology, Fangyi Rao, Keysight Technologies	November 27, 2018, December 4, 2018, January 15, 2019, June 25, 2019, July 23, 2019		
196.1	Prohibit Periods at the End of File Names	Arpad Muranyi, Mentor Graphics, A Siemens Business	September 25, 2018, October 12, 2018	October 12, 2018	7.0
195.1	Enabling [Rgnd] and [Rpower] Keywords for Input Models	Michael Mirmak, Intel Corp.	June 19, 2018, June 29, 2018	August 31, 2018	

[Thank You]

IBIS Open Forum:
Web: http://www.ibis.org
Email: ibis-info@freelists.org

We welcome participation by all IBIS model makers, EDA tool vendors, IBIS model users, and interested parties.

Introducing IBIS Version 7.0

Michael Mirmak
michael.mirmak@intel.com
Randy Wolff
rrwolff@micron.com

http://www.ibis.org/ver7.0/
2019 Asian IBIS Summit
Taipei, Taiwan
November 4, 2019

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Agenda

What IBIS 7.0 Contains

Key Features
- New Interconnect support
- AMI Improvements
- Traditional and Multi-lingual IBIS Improvements

Development Timeline

What's Next?

References

2

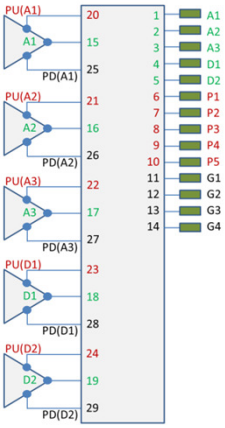
What IBIS 7.0 Contains

- IBIS Version 7.0 is now available
  - 12 chapters, 331 pages
  - Available at http://www.ibis.org/ver7.0/
- 17 BIRDs addressed
  - 5 interconnect/packaging or related changes
  - 6 IBIS-AMI changes
  - 6 traditional IBIS and multi-lingual syntax changes

BIRDs Included in IBIS 7.0

Number	Issue Title	Date First Submitted	Date Approved	Days Open
196.1	Prohibit Periods at the End of File Names	25-Sep-18	12-Oct-18	17
194	Revised AMI Ts4file Analog Buffer Models	2-May-18	29-Jun-18	58
193	Figure 29 corrections	10-Jan-18	23-Mar-18	72
192.1	Clarification of List Default Rules	22-Aug-17	15-Sep-17	24
191.2	Clarifying Locations for Si_location and Timing_location	28-Jun-17	15-Sep-17	79
189.7	Interconnect Modeling Using IBIS-ISS and Touchstone	27-Jan-17	29-Jun-18	518
188.1	Expanded Rx Noise Support for AMI	13-Dec-16	17-Feb-17	66
187.3	Format and Usage Out Clarifications	13-Dec-16	21-Apr-17	129
186.4	File Naming Rules	29-Nov-16	14-Jul-17	227
185.2	Section 3 Reserved Word Guideline Update	13-Sep-16	6-Jan-17	115
184.2	Model_name and Signal_name Restriction for POWER and GND Pins	1-Sep-16	6-Jan-17	127
183	[Model Data] Matrix Subparameter Terminology Correction	30-Aug-16	14-Oct-16	45
182	POWER and GND [Pin] signal_name as [Pin Mapping] bus_label	30-Aug-16	14-Oct-16	45
180	Require Unique Pin Names in [Pin]	17-Feb-16	14-Oct-16	240
179	New IBIS-AMI Reserved Parameter Special_Param_Names	13-Oct-15	18-Dec-15	66
165.1	Parameter Passing Improvements for [External Circuit]s	9-Jan-14	15-Dec-17	1436
158.7	AMI Ts4file Analog Buffer Models	20-Feb-13	27-Oct-17	1710
147.6	Back-channel Support	18-Oct-11	10-Mar-17	1970

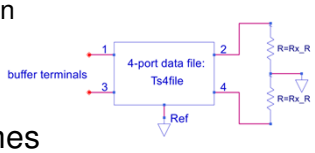
IBIS Interconnect Support



- Improved package modeling is finally here!
  - Touchstone and IBIS-ISS directly supported
  - Explicit locations for buffer, pin, plus die pad
  - On-die power delivery networks
- More detail shared at previous Summits
  - http://ibis.org/summits/feb18/mirmak.pdf
- Additional modifications
  - Voltage and timing measurement locations updated
  - Model, signal name clarifications for POWER and GND
  - Updates to [Pin Mapping] and bus label concepts

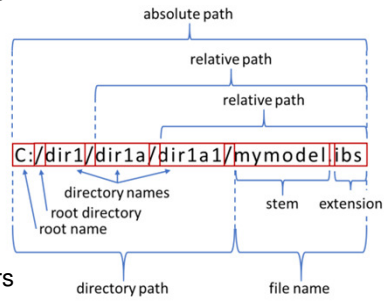
IBIS-AMI Improvements

- Backchannel support!
  - Tx/Rx buffer models negotiate equalization
- Touchstone for analog buffer models
  - 4-port through paths for Tx and Rx
- New parameter Special_Param_Names
  - Enables EDA functions or user interactions under Model_Specific parameters beyond current IBIS definitions
- Clarifications to Format and Usage Out (parser bug fix)
- Clarification of Format List rules, including default value
- Expanded receiver noise support
  - Alternate name for Rx_Noise: Rx_GaussianNoise
  - New Rx_UniformNoise parameter



Traditional & Multi-Lingual IBIS Changes

- Parameters may be passed to instances of [External Circuit]
- File and directory clarifications
  - Naming rules for files and directories
  - Cross-OS support is ensured
- [Pin] list names now must be unique
  - Avoids unintentional shorts or other errors
- Reserved word (e.g., GND) rules relaxed
- Package matrices are no longer “subparameters”



Other Changes

- Organization
  - Three numbered levels
  - Lists of Tables and Figures
  - Hyperlinked Figures and Tables
- Readability improvements
  - Fixes made to grammar and spelling

These improvements create a more readable and more usable document

IBIS 7.0 Timeline

Date	Milestone
4/21/2017	Vote to establish 7.0 as the next IBIS version passes
	BIRD review and acceptance (30 meetings)
7/20/2018	7.0 BIRD set accepted
	Editorial task group drafts IBIS 7.0
12/19/2018	Editorial announces IBIS 7.0 Draft 1 ready Review period begins 12/21/2018 at Open Forum
	Work begins to address comments
1/18/2019	Editorial announces IBIS 7.0 Draft 2 ready
1/25/2019	Editorial announces IBIS 7.0 Draft 3 ready
2/22/2019	Vote to ratify 7.0 scheduled for next meeting
3/15/2019	IBIS 7.0 ratified
10/8/2019	IBISCHK7 Version 7.0.0 parser source code released

BIRDs Excluded from IBIS 7.0 (at time of approval)

BIRD	Title
166.2	Resolving problems with Redriver Init Flow
181.1	I-V Table Clarifications
190	Clarification for Redriver Flow
195.1	Enabling [Rgnd] and [Rpower] Keywords for Input Models
197.2	New AMI Reserved Parameter DC_Offset

- Two of these expand or clarify traditional IBIS
  - Voltage referencing continues to be point of debate
- Two clarify AMI repeater treatment (redrivers)
  - Tabled in IBIS-ATM
- DC_Offset looks ahead to DDR5, LPDDR5, GDDR6
  - Current focus of IBIS-ATM

Targeted for the next IBIS version – possibly 7.1 or beyond

What's Next?

- A Known Editorial Issues document is available
  - Mostly clarifications needed in a future release
- An ibischk7 version 7.0.0 parser for IBIS 7.0 has recently been released (source code to purchases and executables for users)
  - Fixes one BUG discovered by parser developer

Your feedback is vital

References

- IBIS Web site: www.ibis.org
  - Links to Task Groups, including Editorial, available there
- Version 7.0 Specification
  - www.ibis.org/ver7.0/
  - Includes evolution and extended keyword hierarchy information
- Summit Presentations
  - www.ibis.org/summits/

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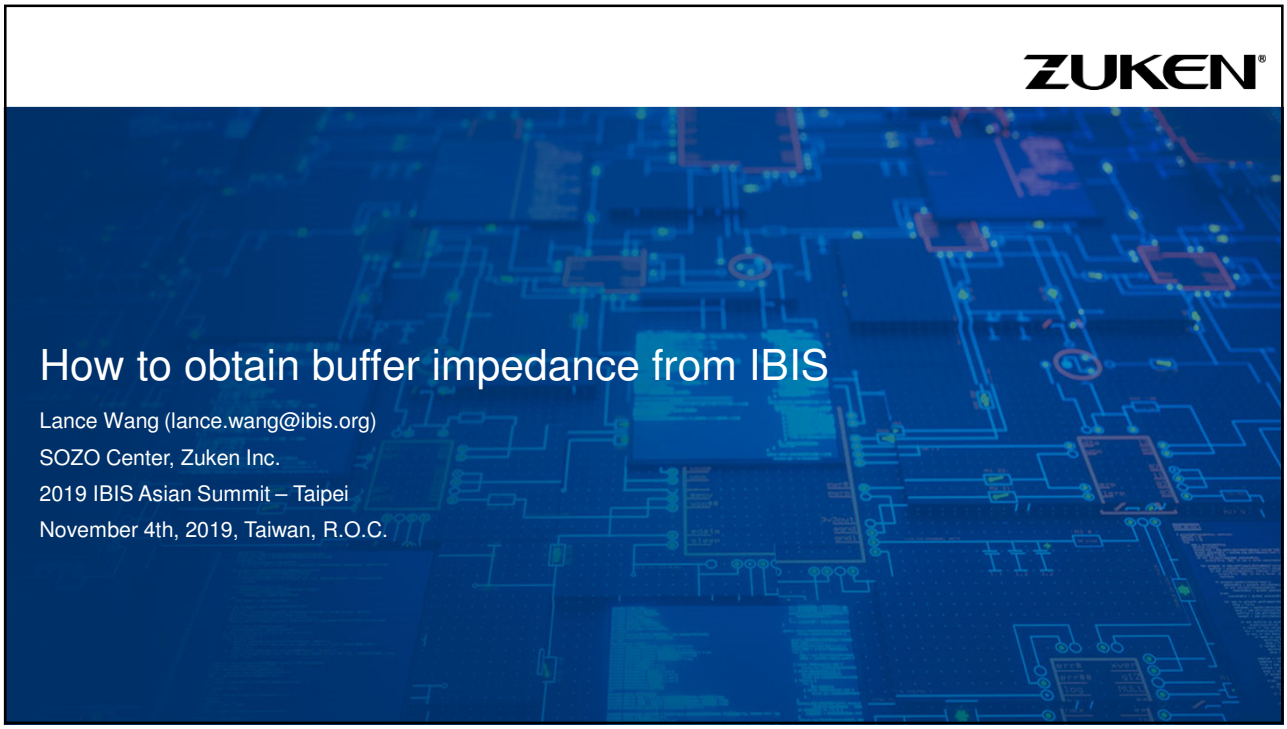
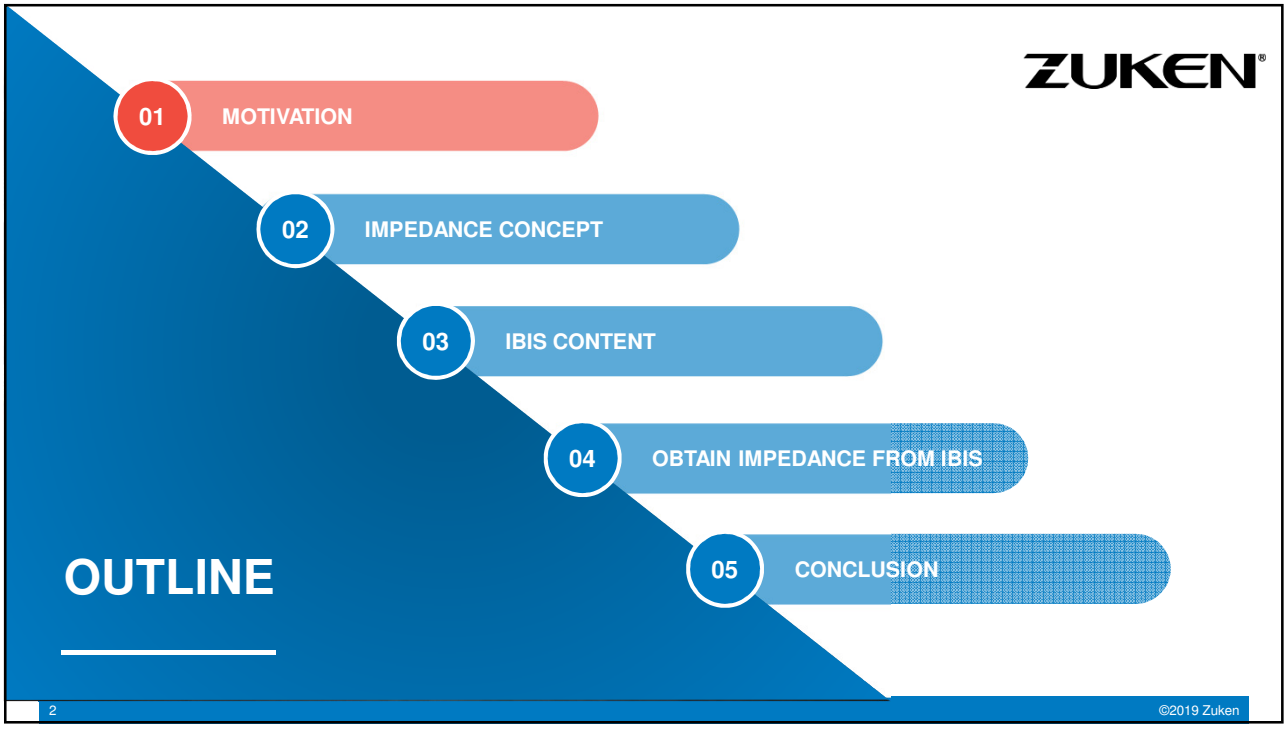
* Other names and brands may be claimed as the property of others


ZUKEN
How to obtain buffer impedance from IBIS
Lance Wang (lance.wang@ibis.org)
SOZO Center, Zuken Inc.
2019 IBIS Asian Summit – Taipei
November 4th, 2019, Taiwan, R.O.C.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01 MOTIVATION
02 IMPEDANCE CONCEPT
03 IBIS CONTENT
04 OBTAIN IMPEDANCE FROM IBIS
05 CONCLUSION
OUTLINE
2
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Motivation

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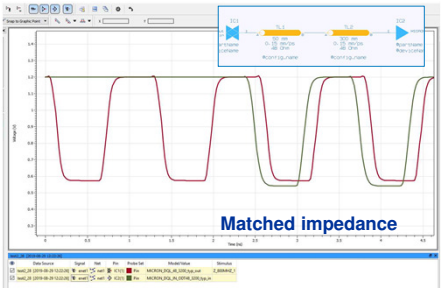
- Impedance matching is the biggest task for Signal Integrity engineer and high-speed PCB/PKG designers.
  - Unmatched impedance may cause unpredictable reflection that reduces the signal quality for high-speed circuit design.
- Interconnects, such as, trace, via, connector, package, etc., are under our radar already.
  - Field Solver helps
- Interconnect impedance also needs to match buffer Output/Input impedance in order to keep good signal quality **How to obtain I/O buffer impedance?**



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Impedance Concept

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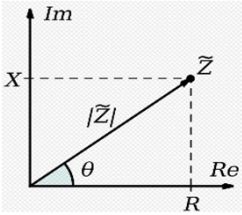
- The impedance of a two-terminal circuit element is represented as a complex quantity Z. The polar form conveniently captures both magnitude and phase characteristics as $Z = |Z|e^{j\,arg(Z)}$
- where the magnitude $|Z|$ represents the ratio of the voltage difference amplitude to the current amplitude, while the argument $arg(Z)$ (commonly given the symbol θ gives the phase difference between voltage and current). j is the imaginary unit and is used instead of i in this context to avoid confusion with the symbol for electric current.
- In Cartesian form, impedance is defined as $Z = R + jX$
- where the real part of impedance is the resistance R and the imaginary part is the reactance X.

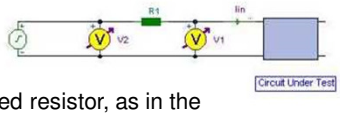


For a high-speed I/O buffer, the buffer inductance and capacitance are specially designed. It is close to minimum for the reactance X. So, in this case, the resistance R is the main factor for impedance matching.

Measuring Impedance – Input Impedance

ZUKEN

- From the AC impedance triangle, the input or output impedance of a two terminal network can be determined by measuring the small signal AC currents and voltages.
  - The voltage is measured across the input terminals and the current measured by inserting the meter in series with the signal generator.



  - An easy way to measure small input currents, is to use a fixed resistor, as in the diagram above. Measure the AC voltage at points V1 and V2, then the input current, I_{in} becomes:

$$I_{in} = \frac{V_2 - V_1}{R_1}$$

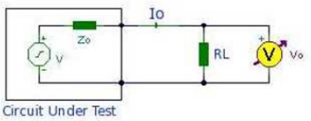
  - The input impedance Z_{in} of the circuit under test is then found by:

$$Z_{in} = \frac{V_1}{I_{in}}$$

Measuring Impedance – Output Impedance

ZUKEN

- Output impedance may also be determined using a similar technique. A fixed load resistor is used, and the output voltage is measured first with full load, then without the load.



- Z_0 is the internal output impedance of the network to be measured.
- To find the output impedance the output voltage is measured first with no load resistor, then with a fixed load (purely resistive).
- First, the load resistor R_L is removed and output voltage (V) measured and recorded. Then R_L is placed back in circuit and the output voltage under load (V_L). The output impedance, Z_0 is now found by Ohm's Law for AC circuits. As the load is purely resistive $Z=V/I$, where *"V"* is voltage drop across the output impedance: (V - V_L), and *"I"* the output current, V_L/R_L. Thus:

$$Z_0 = \frac{(V - V_L)}{V_L/R_L} = \frac{R_L(V - V_L)}{V_L}$$

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OUTLINE

01 MOTIVATION

02 IMPEDANCE CONCEPT

03 IBIS CONTENT

04 OBTAIN IMPEDANCE FROM IBIS

05 CONCLUSION

IBIS model contents

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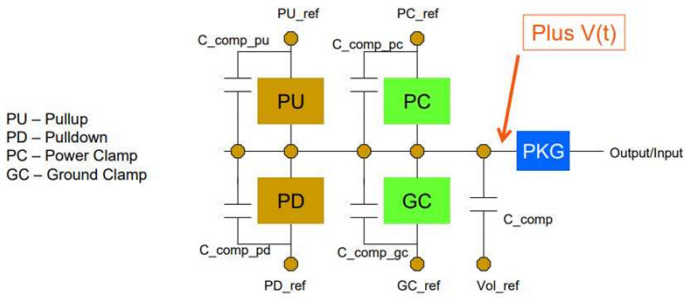
IBIS Buffer Structure



All curve data are independent with own voltage references

- I/O type
  - 4 static curve data sets
    - Pullup
    - Pulldown
    - Power Clamp
    - Ground Clamp
- Output type
  - 2 static curve data sets
    - Pullup
    - Pulldown
- Input type
  - 2 static curve data sets
    - Power Clamp
    - Ground Clamp

IBIS model contents

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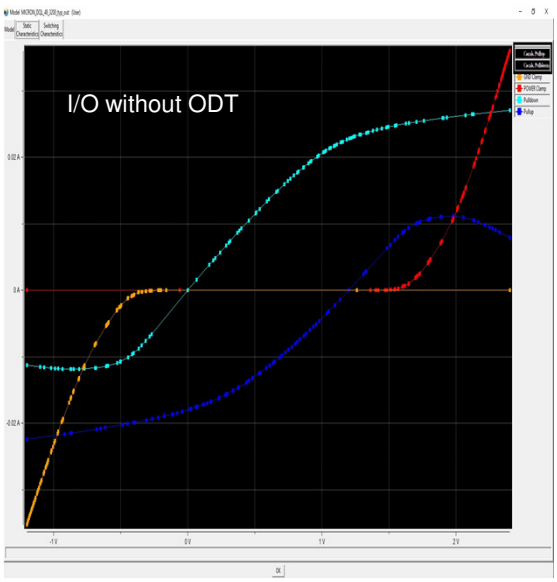

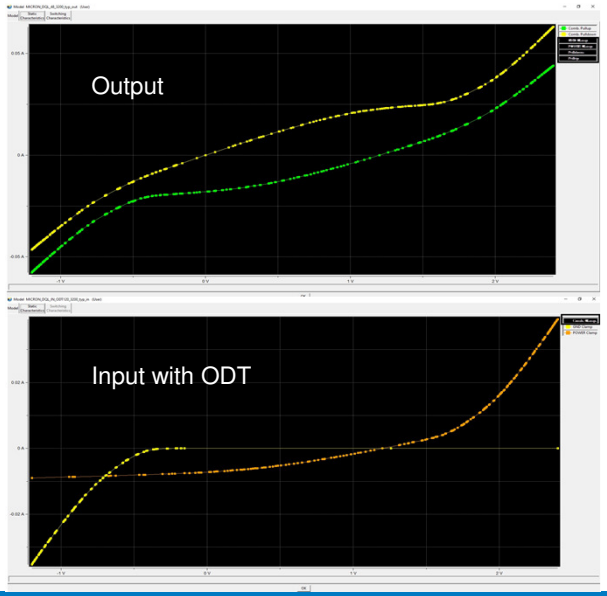

IBIS model contents

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IBIS MODELING COOKBOOK
For IBIS Version 4.0

Prepared By:
The IBIS Open Forum

Approved September 15, 2005

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From an original by Stephen Peters published 1997

3.1 Extracting I-V Data from Simulations

The first step to extracting the required I-V tables is understanding the buffer's operation. Analyze the buffer schematic and determine how to put the buffer's output into a logic low, logic high and (if applicable) high impedance (3-state) state. As mentioned above, the schematic should include any ESD or protection diodes. Also, understand the buffer's power supply voltage reference ("Vcc") requirements and connections. The schematic should also indicate if the power clamp and/or ground clamp diode structures are tied to voltage rails (voltage references) different from those used by the pullup and/or pulldown transistors.

3.1.1 Simulation Setup

A typical I-V table simulation setup for an output or I/O buffer is shown in Figure 3.1 below. For this example, the buffer being analyzed is a standard 3-state buffer with a single push-pull output stage. The buffer uses electrostatic discharge protection devices in addition to its parasitic driver diodes. The buffer's clamp supplies are assumed identical to its driver supply (Vcc hereinafter).

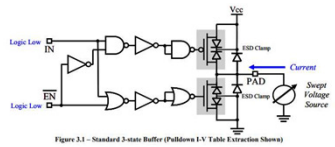

Figure 3.1 – Standard 3-state Buffer (Pulldown I-V Table Extraction Shown)

All measurements are made at the output node (pad) as shown above. Remove all package lead (R_pin, L_pin, and C_pin) parasitics. However, any series resistances present between the pad and the pullup/pulldown transistors should be included (these are not shown in Figure 3.1).

The output buffer is connected to an independent voltage source. Set the buffer's input(s) so that the desired output state (low, high, off) is obtained, then using a DC or "transfer function" analysis sweep the voltage source over the sweep range -Vcc to 2*Vcc while recording the current into the buffer. An alternative method is to perform a "transient analysis". The voltage source in this case should be linear ramp function driving the output node, slow enough that the current measurement at each time point is effectively DC, without reactive aspects of the design affecting the result. The current flow into the pad is measured (by IBIS convention, current flow into the die pad is positive), as is the voltage at the node with respect to a reference, then the resulting I-T and V-T data is combined into a single I-V table. Note that a transient function analysis may require post-simulation data manipulation.

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OUTLINE

Obtain impedance from IBIS curves

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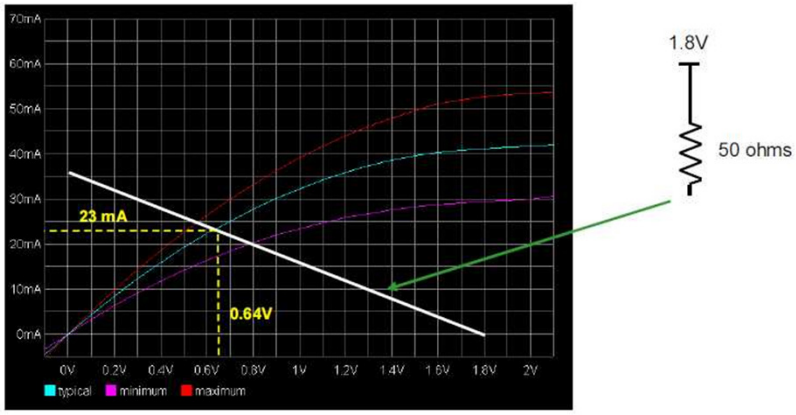

Picture from Todd W. 2005 DAC IBIS Summit

Obtain Output type buffer impedance from IBIS

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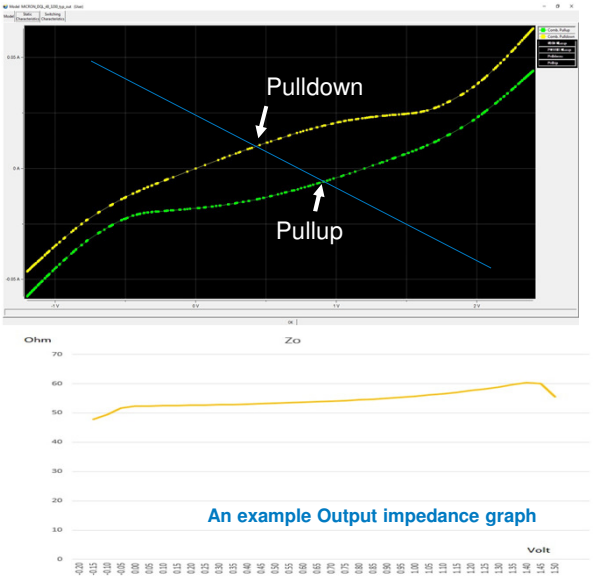
- Need to use Combined Pullup/Pulldown curves
  - Pullup + Clamps
  - Pulldown + Clamps
- Load line / Crossing Point
- To avoid numerical errors

$$Z_0 = \frac{dV}{dI} \text{ @ } R_L$$



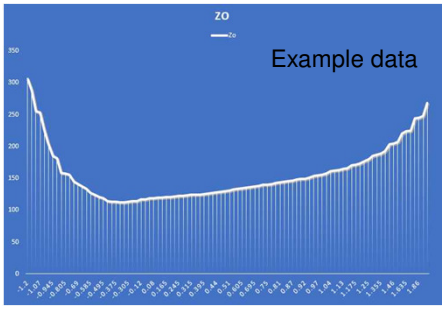
An example Output impedance graph

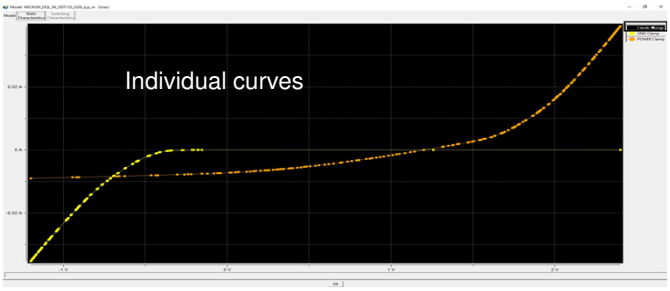
Obtain Input type buffer impedance from IBIS

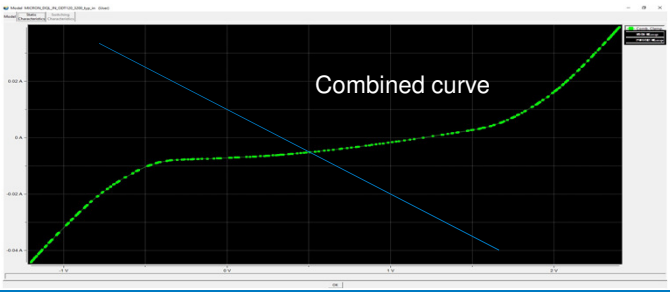
ZUKEN

- Use the Combined Clamp data
- To avoid numerical errors

$$Z_0 = \frac{dV}{dI} @ R_L$$







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01 MOTIVATION

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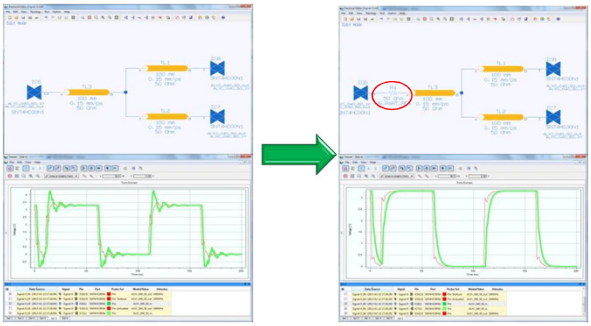
OUTLINE

Conclusion

ZUKEN

- Impedance matching is important for high-speed design
  - Not only for interconnect impedance, but also I/O buffer impedance should be counted in the big picture
- The I/O buffer impedance can be obtained from IBIS curve data
  - Obtain buffer driving impedance from IBIS combined Pullup/Pulldown curve data
  - Obtain buffer Input impedance from IBIS combined Power /Ground Clamps curve data
- I/O impedance maybe vary for different loads



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IBIS-AMI & COM Co-design for 25G Serdes

Asian IBIS Summit
Taipei, ROC
November 4, 2019

Nan Hou, Amy Zhang, Guohua Wang, David Zhang, Anders Ekholm

AGENDA

- Traditional IBIS-AMI
- COM Overview
- IBIS-AMI Co-design with COM for 25G
- Two example channels
- Co-simulation Conclusion
- Next Steps

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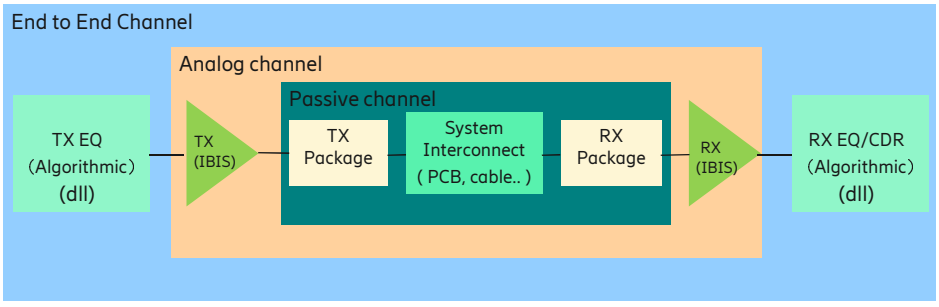
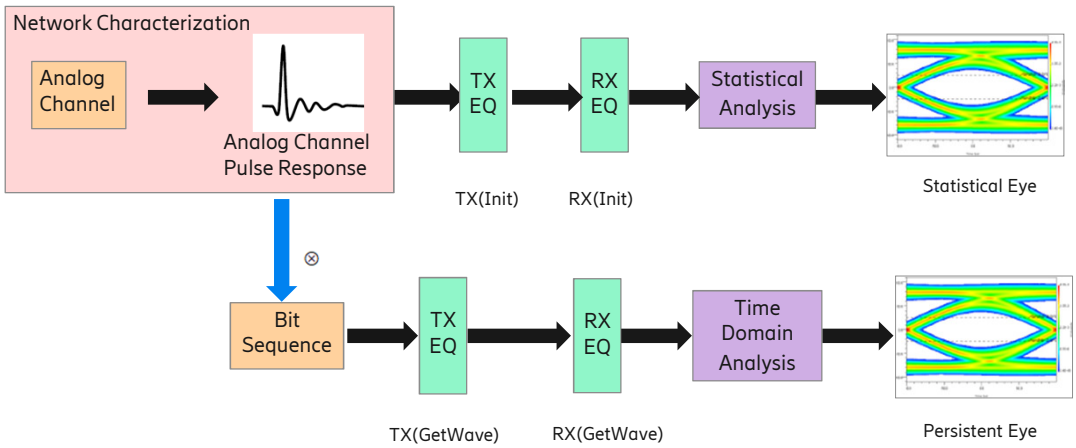
IBIS-AMI OVERVIEW

- IBIS is Input/output Buffer Information Specification
- AMI stands for Algorithmic Modeling Interface
- Analog model: drive strength/amplitude, rise/fall time, impedance
- Algorithmic model: Equalizer (CTLE, FFE, DFE) , clock data recovery



IBIS-AMI FLOW



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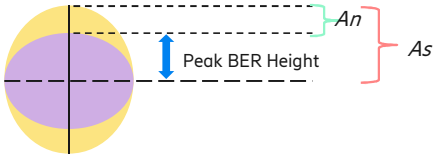
COM OVERVIEW

The Channel Operating Margin (COM) is a figure of merit for a channel derived from a measurement of its scattering parameters
COM is related to the ratio of a calculated signal amplitude to a calculated noise amplitude as defined by Equation

$$COM = 20 \times log10(As/An)$$



Where *As* is the signal amplitude, *An* is the noise amplitude
COM has been adapted by various standards:

- IEEE 802.3
- OIF CEI
- JEDEC 204C

An (Peak BER Noise) = *As* - Peak BER Height

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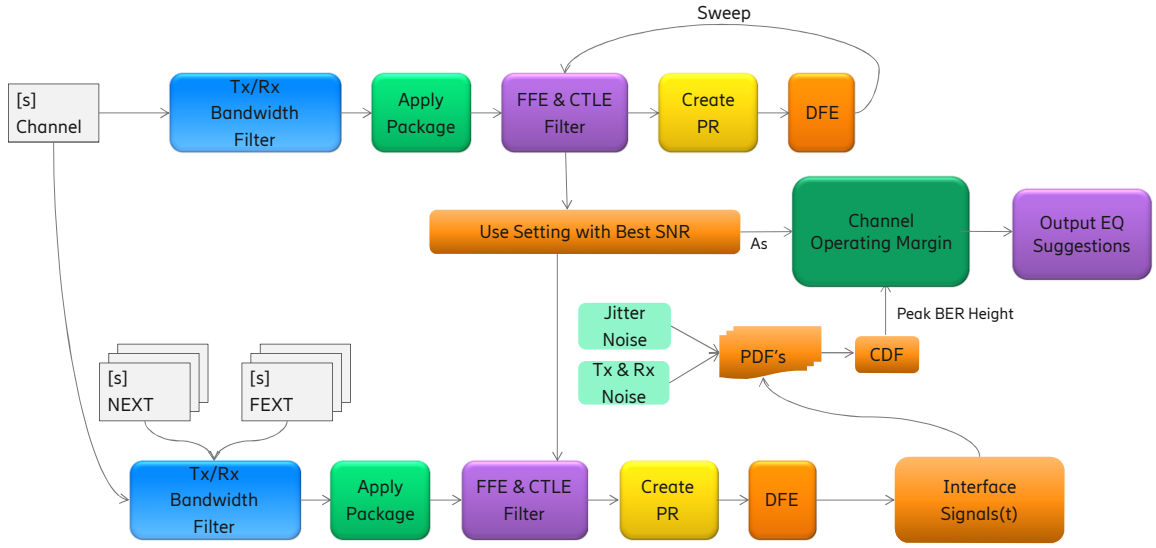
COM FLOW



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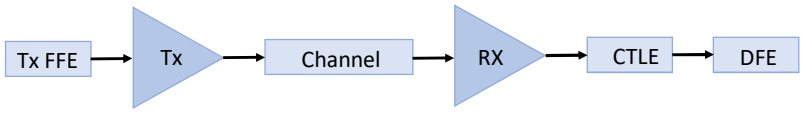
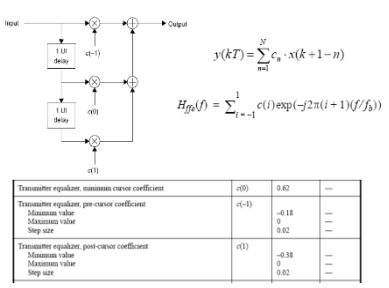
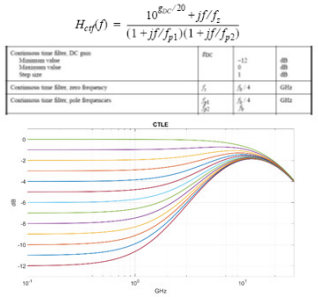
COM CHANNEL TRANSFER FUNCTION



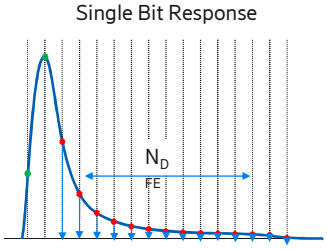
$$H(f) = H_{Tx}(f) \times H_{TxFFE}(f) \times H_{ch}(f) \times H_{Rx}(f) \times H_{RxCTLE}(f)$$



Tx FFE



Rx CTLE



Rx DFE

COM OPTIMAL EQ SETTINGS

- COM is a figure of merit (FOM), which calculates the ratio of peak signal level to the peak noise level at the receiver sampling latch, comprehending device Tx characteristics (i.e., driver filter, FFE filter, package S-parameters), channel characteristics (i.e., S-parameters) and receiver characteristics (i.e., Rx filter, CTLE filter, package S-parameters and DFE)
- Determine optimal equalization settings
  - An exhaustive search for the best SNR used as a FOM for finding the best FFE and CTLE setting
  - FFE and CTLE are optimized jointly
  - The DFE is only used to gate the SBR

$$FOM = 10log_{10}\left(\frac{A_S^2}{\sigma_{TX}^2 + \sigma_{ISI}^2 + \sigma_J^2 + \sigma_{XT}^2 + \sigma_N^2}\right)$$

A_S – peak signal amplitude
σ_{TX} - transmitter noise
σ_{ISI} - residual ISI
σ_J – jitter contribution to amplitude noise
σ_{XT} – peak crosstalk
σ_N – spectral noise at the ouput of CTLE

AGENDA

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IBIS-AMI COMBINE WITH COM

- Can we use COM to evaluate the channel margin in early design phase of a project?
- Are the COM recommended equalization parameters suitable for the Channel?
- How can we combine the advantages of COM with IBIS-AMI?

25G CO-SIMULATION PROCESS

- Extraction of passive S parameter model of the simulation channel
- Use S parameter to do COM simulation
- IBIS simulation using COM recommended EQ parameter
- IBIS simulation to sweep EQ parameter
- Comparing the eye diagram in time domain

AGENDA

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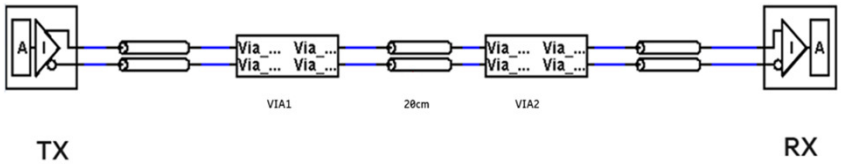
CASE1-SIMULATION TOPOLOGY

Simulation Topology Configuration

- Signal Rate: 25Gbps
- PCB Material: Mid-loss FR4
- PCB Channel Length: 20 cm



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COM SIMULATION CONFIGURATION

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	24.576	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[2.5e-4 2.5e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 30]	mm	[test cases]
z_p (NEXT)	[12 12]	mm	[test cases]
z_p (FEXT)	[12 30]	mm	[test cases]
z_p (RX)	[12 30]	mm	[test cases]
C_p	[1.8e-4 1.8e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[55 55]	Ohm	[TX RX]
f_r	0.75	*fb	
c(0)	0.62		min
c(-1)	[-0.18:0.02:0]		[min:step:max]
c(1)	[-0.38:0.02:0]		[min:step:max]
g_DC	[-12:1:0]	dB	[min:step:max]
f_z	6.144	GHz	
f_p1	6.144	GHz	
f_p2	24.576	GHz	
A_v	0.4	V	
A_fe	0.4	V	
A_ne	0.6	V	
L	2		
M	32		
N_b	0	UI	
b_max(1)	1		
b_max(2..N_b)	1		
sigma_RJ	0.01	UI	
A_DD	0.05	UI	
eta_0	5.20E-08	V^2/GHz	
SNR_TX	27	dB	
R_LM	1		
DER_0	1.00E-12		
Operational control			
COM Pass threshold	3	dB	
Include PCB	0	logical	

Table 93A-2 parameter		
Parameter	**Setting**	**Units**
package_tl_tau	6.141E-03	ns
package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
package_Z_c	78.2	Ohm

Table 92-C12 parameter		
Parameter	**Setting**	
board_tl_tau	6.191E-03	ns
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
board_Z_c	109.8	Ohm
z_bp (TX)	151	mm
z_bp (NEXT)	72	mm
z_bp (FEXT)	72	mm
z_bp (RX)	151	mm

All parameter come from IEEE 802.3bj

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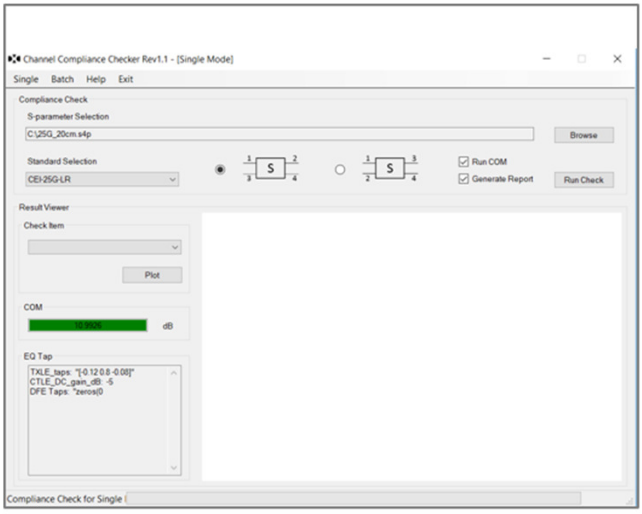
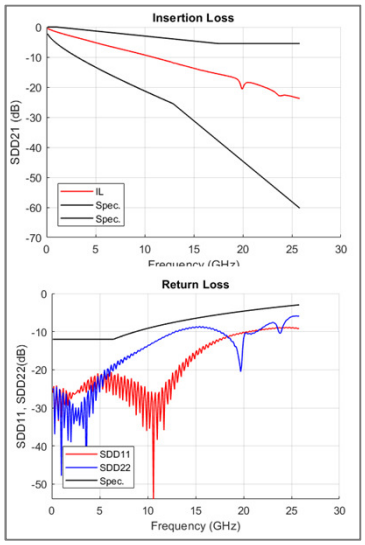
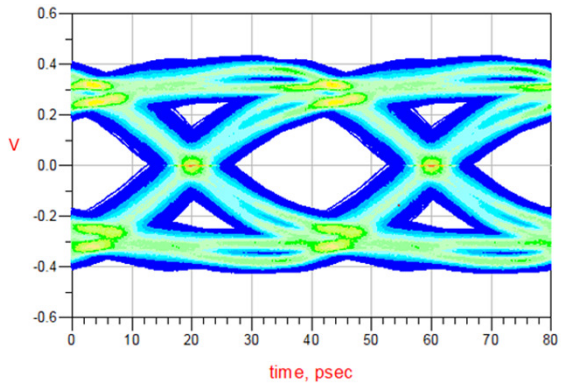
COM SIMULATION RESULT





IBIS-AMI SIMULATION WITH COM RECOMMENDED PARAMETER



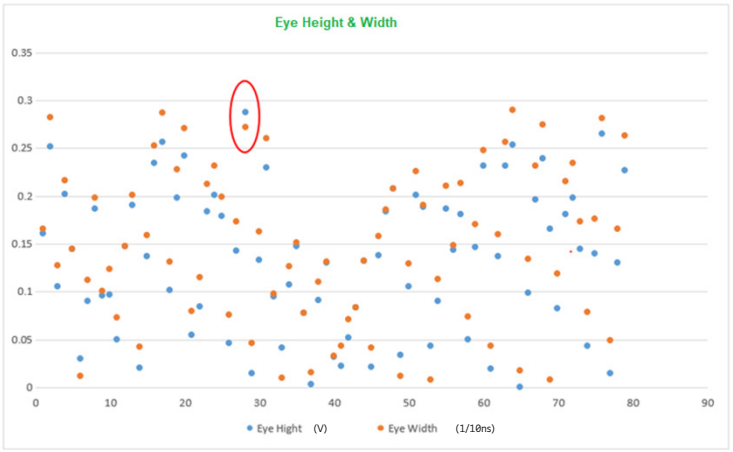
Eye Diagram after RX EQ

index	Width	Height
0.000	2.780E-11	0.289

EQ Parameters: COM Recommend

TX: C(-1)=-0.12
C(0)=0.8
C(1)=-0.08
RX: CTLE=-5
DFE off

IBIS-AMI SWEEP PARAMETERS RESULT



In the red circle is COM recommend EQ parameters

✓ COM recommended EQ parameters produce an acceptable eye opening, but possibly less optimal than the eye opening obtained by time domain simulation

Sweep parameter:
TX: C(-1),C(0),C(1)
RX: CTLE
Total case: 80
Time Domain Simulation

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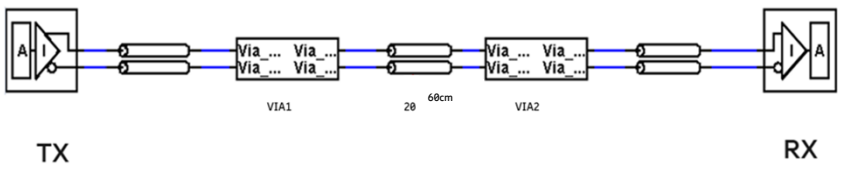
CASE2-SIMULATION TOPOLOGY

Simulation Topology Configuration

- Signal Rate: 25Gbps
- PCB Material: Mid-loss FR4
- PCB Channel Length: 60 cm



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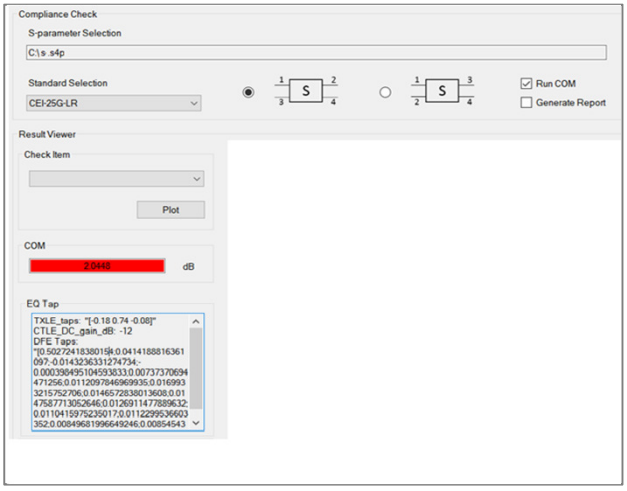
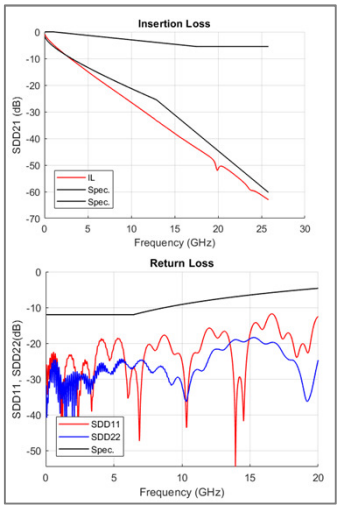
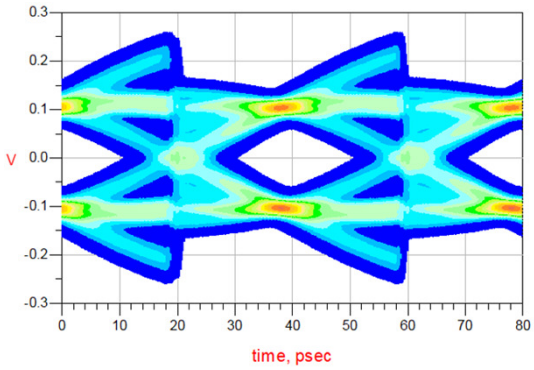
COM SIMULATION RESULT





IBIS-AMI SIMULATION WITH COM RECOMMENDED PARAMETER

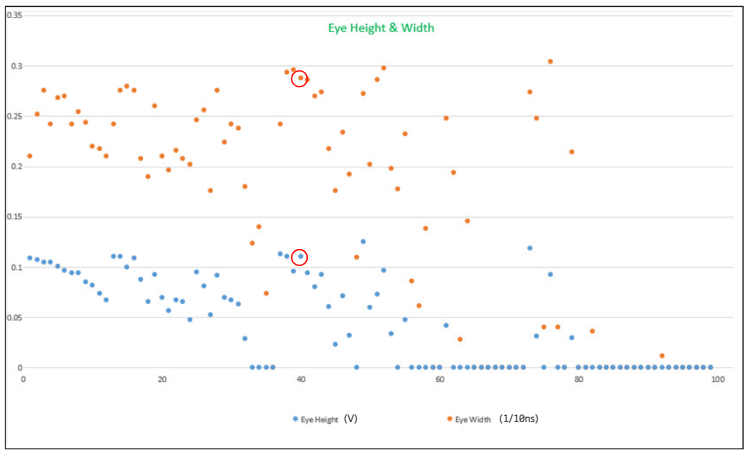


Eye Diagram after RX EQ

index	...robe1.Height)	...Probe1.Width)
0.000	0.109	2.100E-11

EQ Parameters: Use COM Recommended

IBIS-AMI SWEEP PARAMETERS RESULT



In the red circle is COM recommended EQ parameters

- ✓ COM recommended EQ parameters produce a good time domain eye diagram

Sweep parameter:
TX: C(-1),C(0),C(1)
RX: CTLE&DFE
Total case: 100
Time Domain Simulation

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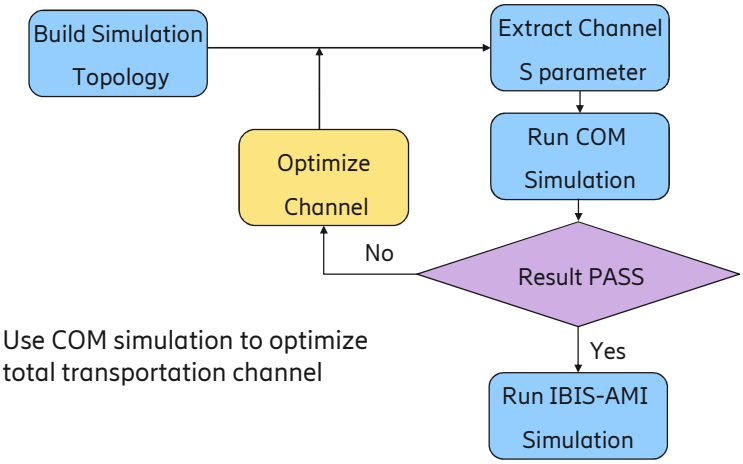
CO-DESIGN SIMULATION FLOW



Use COM simulation to optimize total transportation channel

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CO-SIMULATION CONCLUSION

- COM enables passive channel evaluation of high-speed signals at early design phase
- COM recommended EQ parameters are suitable for same channel in time domain simulation
- COM simulation is faster, making them more suitable for the post-layout phase of large designs to sweep EQ parameters

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NEXT STEPS

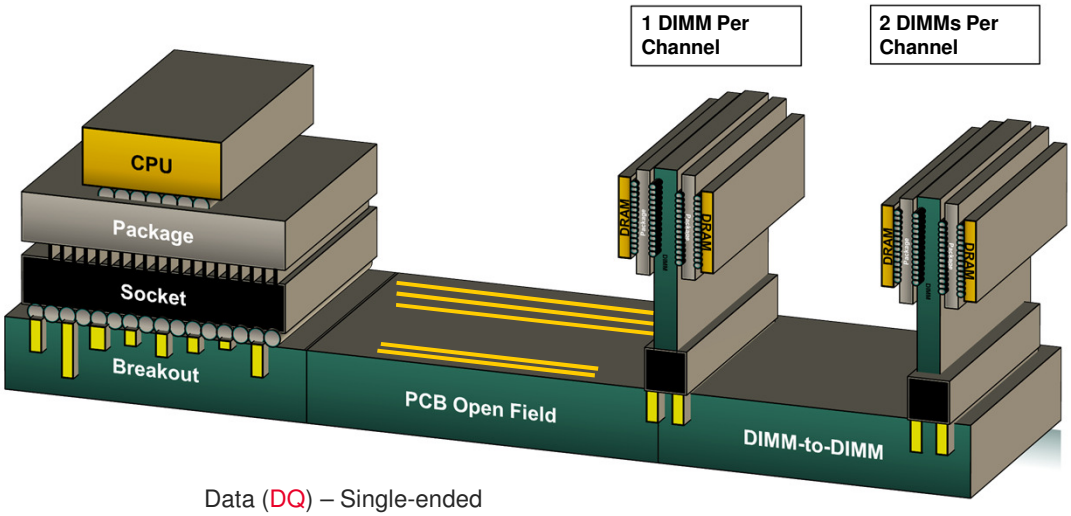
- Model crosstalk in actual link
- Co-simulation for 56G PAM-4
- Accuracy of IBIS-AMI model
- Correlation of Co-simulation with measurement

Innovations in DDR Memory Simulation

Stephen Slater | NOVEMBER 4, 2019
Asian IBIS Summit, Taipei, ROC

KEYSIGHT TECHNOLOGIES

A Typical DDR5 Application



Data (DQ) – Single-ended
Data Strobe (DQS) – Differential
Microstrip & Stripline

KEYSIGHT TECHNOLOGIES

2

What Does it Mean to Succeed?

THE MEASURE OF SUCCESS FOR A PRODUCT WITH DDR5

- No system failures, under stress
  - At Max and Min temperatures
  - Using multiple vendors' DIMMs
  - 1 DIMM slot and 2 DIMM slots filled
  - Running diagnostic software that stresses the memory access
  - Graceful performance degradation

"I can stop testing when I'm certain my manager is satisfied with the product quality risk"

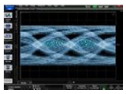
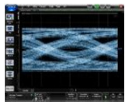
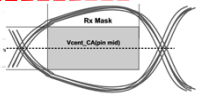
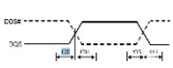
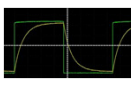
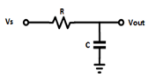
Source: Burn-in environment test chambers by EDA-Industries S.p.a

KEYSIGHT TECHNOLOGIES

3

How Did we Get to DDR5?

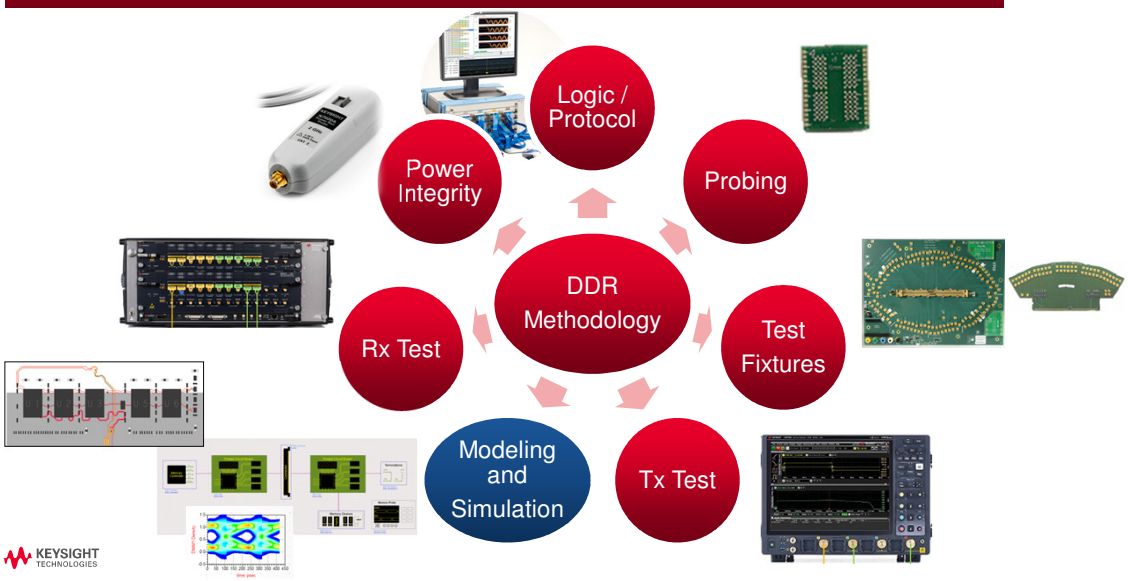
A ROAD PAVED BY INNOVATION

Signal	MT/s	Generation	Characteristics	Specification	Introduction
	4200 – 8000+	DDR5+	"Hyper Speed" • Eye collapses • Impulse response • BER Rj/Dj, Rn/Dn		2019
	1600 – 4200	DDR4	"Serial Speed" • Eye Diagrams • Rx Masks • Bit error rates		2014
	200 – 1600	DDR/2/3	"High Speed Digital" • Transmission lines • Ts / Th, Skew		2002
	33 – 133	SDRAM	"Low Speed" • Fanout • Capacitance		1961

KEYSIGHT TECHNOLOGIES

Ensuring First Pass Success - One Layer Deeper

ENSURING THE SYSTEM IS PERFORMANT AND RELIABLE



KEYSIGHT TECHNOLOGIES

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Change, Challenges and Solutions

1. Crosstalk, Jitter and Bit-Error-Rate (BER) Specs
2. Closed eyes need equalization and training
3. Innovations in Simulation and Modeling of DDR5 & LPDDR5 systems

KEYSIGHT TECHNOLOGIES

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1. Crosstalk, Jitter and Bit-Error-Rate (BER) Specs

KEYSIGHT TECHNOLOGIES

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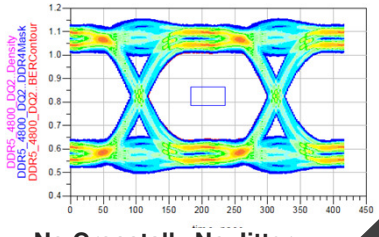
Electromagnetic (EM) Simulation

Crosstalk

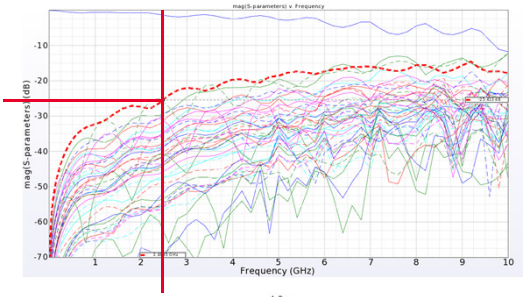
THE IMPORTANCE OF THE SIGNAL RETURN PATH

DDR5-4800



No Crosstalk, No Jitter –
Just ISI from Channel

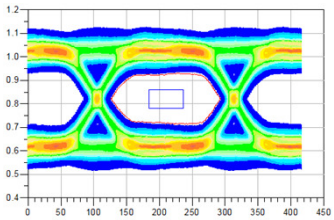
< -25dB



Nyquist

Signal Return Path –
through shared Ground
Pin

PCB Trace Routing of Victim +
Worst Aggressors



With Crosstalk

KEYSIGHT TECHNOLOGIES

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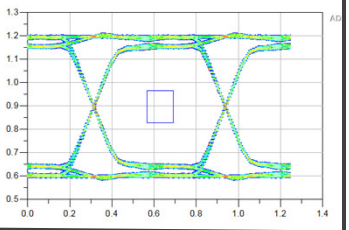
Jitter

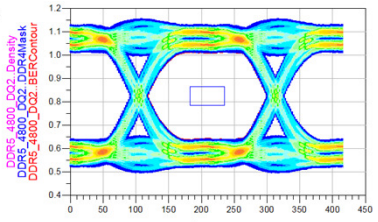
Jitter injected at Tx, and eye measured at the DRAM Solder-Ball (Rx Input)

BER CONTOUR AT 1E-16 TELLS US THE REAL MARGIN

DDR4-1600 | DDR5-4800

No Jitter – Just ISI from Channel



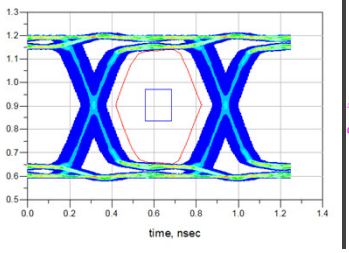


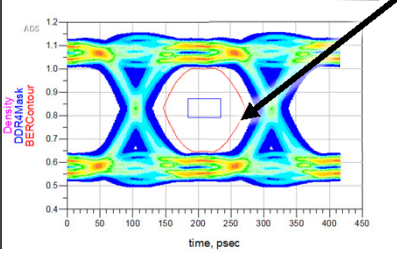
No Jitter – More ISI from Channel due to higher speed

47% Reduction in Timing Margin

(27ps less margin to mask)

Random Jitter = 0.02 UI Applied at Tx (2%)





KEYSIGHT TECHNOLOGIES

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Specs Becoming More Bit-Error-Rate Focused

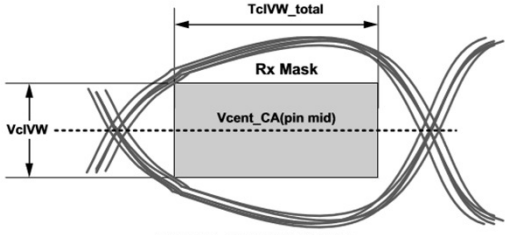

Figure 179 — CA Receiver (Rx) mask

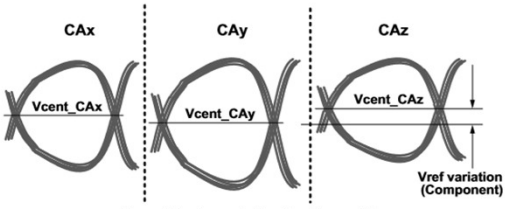

Figure 180 — Across pin V_{REF}CA voltage variation

- From the draft spec:
  - Maximum Jitter (Dj, Rj and DCD) specifications for Tx and Rx components
  - For Tx and Rx Voltage and Timing tests, system BER is e-16 and requires 5.3e9 minimum UIs for validation (99.5% confidence level)
  - New receiver stressed-eye tests for components and DIMMs

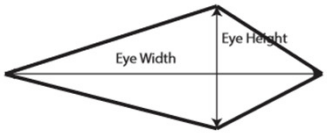

Figure 196 — Example of Rx Stressed Eye Height and Eye Width

Stressed Eye is calibrated to a specified height and width. The DIMM, DRAM or Memory Controller Rx must be able to receive to the system BER

KEYSIGHT TECHNOLOGIES

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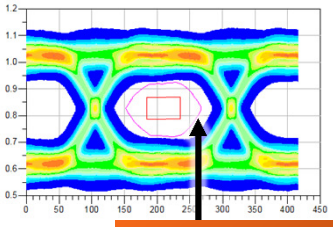
Crosstalk, Jitter & BER Specs

KEY INSIGHTS

- Jitter and Crosstalk are Very Significant
- Simulation must predict Eye closure due to Random Jitter down to the system BER (1e-16) in a practical time
- EM simulation must capture Crosstalk accurately

DDR5-4800

Jitter, crosstalk & Channel ISI



64% Reduction in Voltage Margin

63% Reduction in Timing Margin

KEYSIGHT TECHNOLOGIES

2. Equalization and Training

KEYSIGHT TECHNOLOGIES

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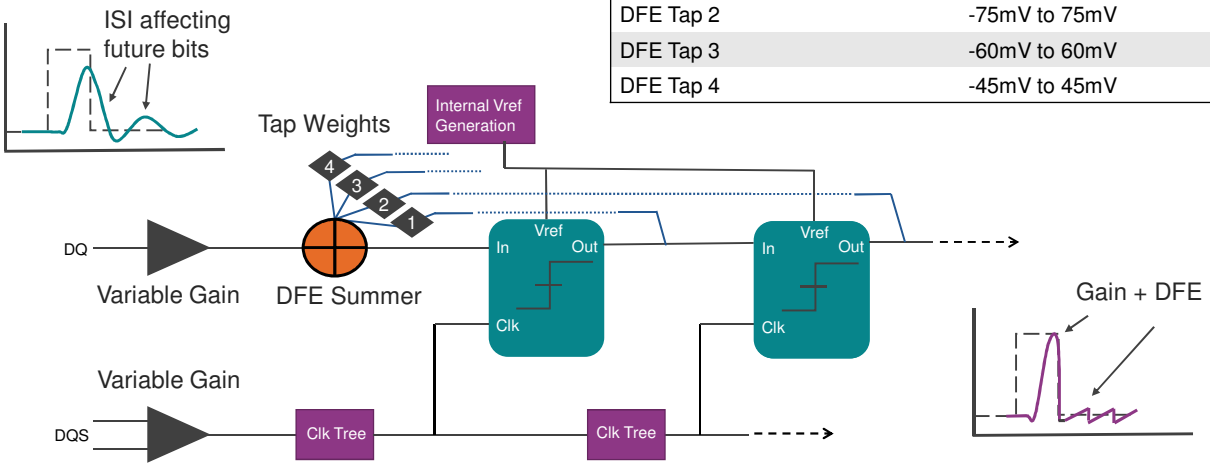
Rx Equalization

FIRST TIME TO HAVE DFE ON DRAM!

Mode Register Settings (per DQ)	*All values subject to change*
Variable Gain	-6dB to 6dB
VrefDQ	-3 to +3 Offset steps
DFE Tap 1	-200mV to 50mV
DFE Tap 2	-75mV to 75mV
DFE Tap 3	-60mV to 60mV
DFE Tap 4	-45mV to 45mV



KEYSIGHT TECHNOLOGIES

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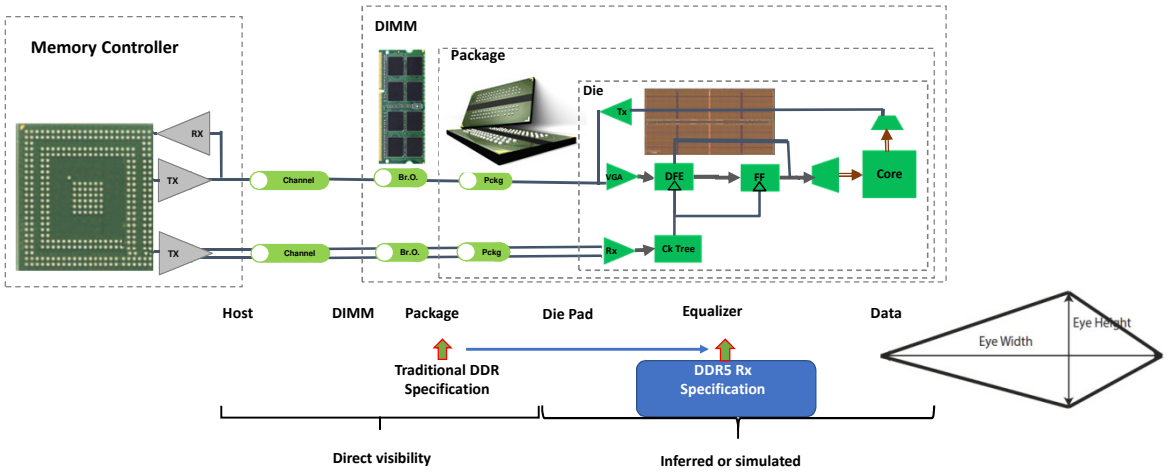
DDR5 Rx Specifications are Inside the Die



KEYSIGHT TECHNOLOGIES

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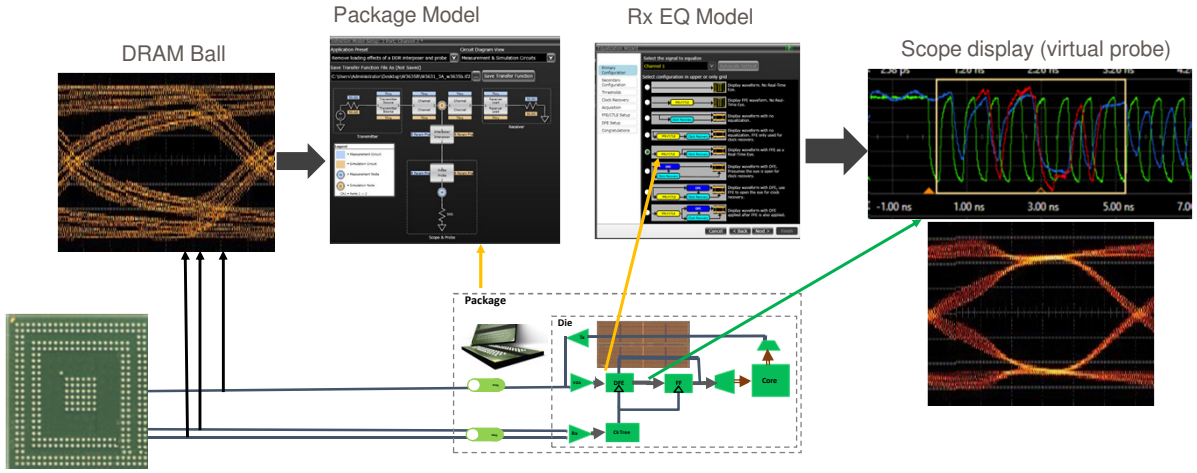
DDR5 Tx Test: New Methodology Needed

VIRTUAL PROBING INSIDE THE DIE



KEYSIGHT TECHNOLOGIES

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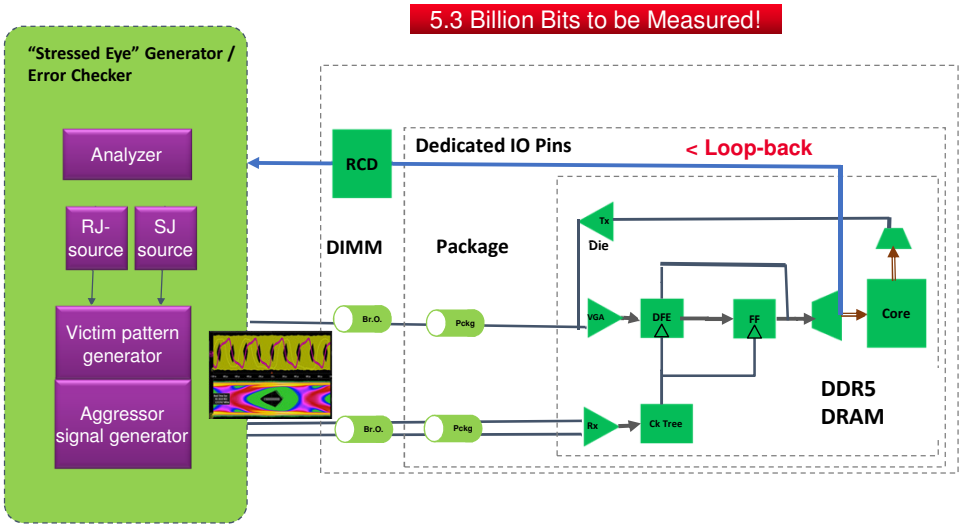
DDR5 Rx Test: New DRAM Feature - Loop-Back Mode

5.3 Billion Bits to be Measured!



KEYSIGHT TECHNOLOGIES

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Skew Adjustment with Write-Leveling

- Due to the fly-by topology of the clock for DDR4 & DDR5, the Clock (Clk) is inevitably skewed to the DQS at each of the independent DRAM

- The controller has ability to adjust skew between DQ's, DQS and the Clock signal.
- DQS is adjusted to match the Clk first, then internal alignment of each DQ is performed (via mode register) to remove DQ-to-DQS skew (due to the package and die)

Equalization and Training

KEY INSIGHTS

- **Possible to have a Closed eye at input to Rx**
- **Optimal Eye opening depends on:**
  - **Vref setting (per DQ)**
  - **Gain Setting (per DQ)**
  - **DFE Tap settings (4 taps per DQ)**
  - **Timing of DQS to DQ**
  - **Write-leveling (skew adjustment)**

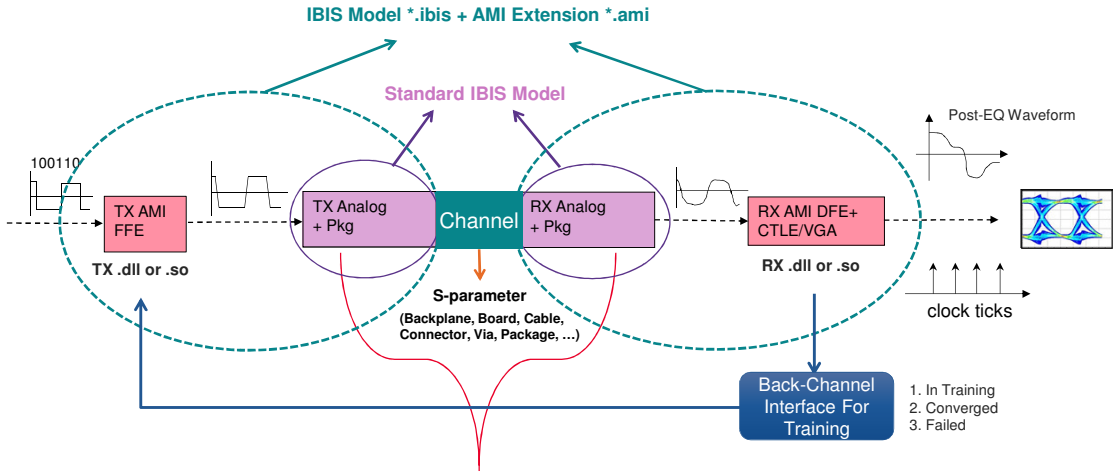
3. Innovations in Simulation and Modeling of DDR5 & LPDDR5 systems

Introducing IBIS AMI for DDR Signals

- EQ Necessary for TX: 3 Tap Pre-Emphasis (Feed Forward Equalization)
- EQ Necessary for RX: CTLE/VGA/DFE
- IBIS-AMI offers
  - Portability – One IBIS-AMI mode can run on many EDA tools
  - IP Protection – Digital signal processing behavior is concealed in model DLL/shared object
  - Interoperability - IC Vendor A←→IC Vendor B (AMI defines a common interface between the vendor model and the EDA channel simulator)
  - Non-linearity – As complex as the model vendor wishes the model to be
  - Performance – Ultra low BER simulations in seconds not days over the traditional SPICE simulation
- AMI has been widely adopted by IC, system and EDA companies for SerDes signals but this is the first application to DDR single-ended signals.

How Does Standard IBIS-AMI Work?

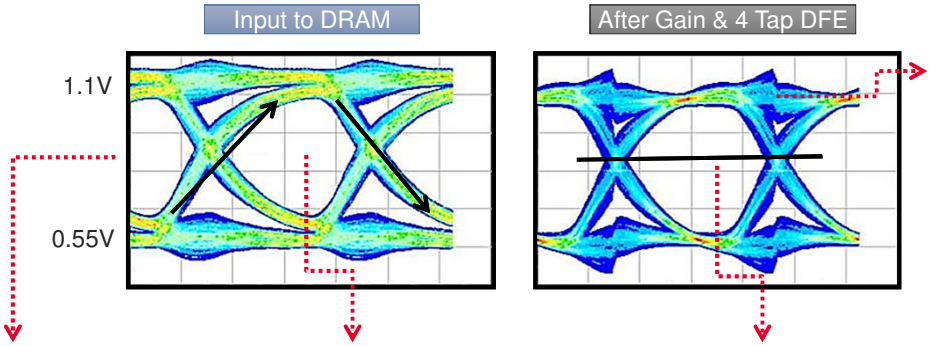
CHANNEL SIMULATION



Impulse response of a Linear Time Invariant Network

What Do We Need for DDR5 AMI To Work?

SUPPORTING PARALLEL, SINGLE-ENDED SIGNALS WITH EXTERNAL CLOCKS



DFE Clocked by DQS:

- Correlated Jitter on DQ & DQS cancels out
- Uncorrelated Jitter on DQS is transferred to DQ

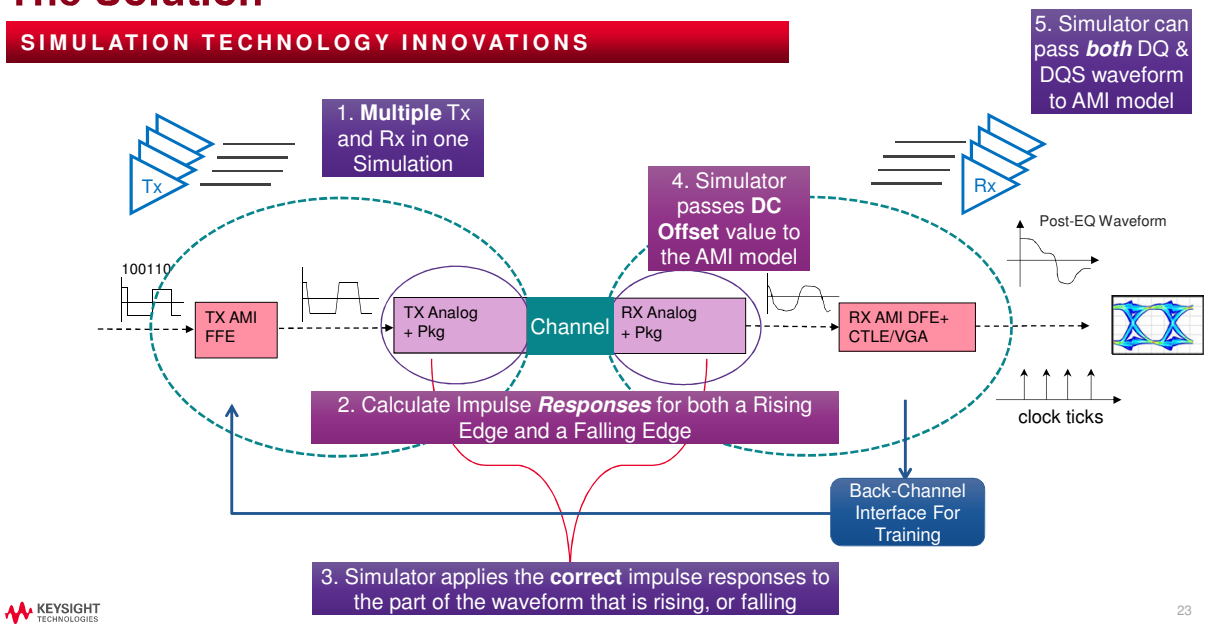
Single-Ended Signal can have a DC Offset

Asymmetric Eye: Rise Time ≠ Fall Time

Asymmetric Eye: Crossing Points are shifted in the Equalized Eye

The Solution

SIMULATION TECHNOLOGY INNOVATIONS



KEYSIGHT TECHNOLOGIES

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KEYSIGHT TECHNOLOGIES

Channel Simulation Over DDR4/5 and Above

Kumar Keshavan, Ambrish Varma, Ken Willis, Skipper Liang
Asian IBIS Summit
Taipei, Taiwan
November 4, 2019

cadence

Two Concerns:

- As the transmission rate of memory bus goes beyond 5Gbps, besides the well-known timing and overshoot/undershoot analysis, it requires BER prediction analysis and channel analysis
- Two additional concerns we need to face while using channel engine to deal with memory bus:
  - Asymmetric rising/falling edges

    Different from differential serial buses, single-ended memory buses will have non-symmetrical rising and falling edges due to the inherent difference between these two kinds of circuits
  - Strobes as timing reference

    While the sampling clock ticks in serial bus are recovered from the signal itself by CDR, the sampling clocks or the timing references in memory bus will be the strobes rather than any recoveries

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Asymmetric Rising and Falling Edges

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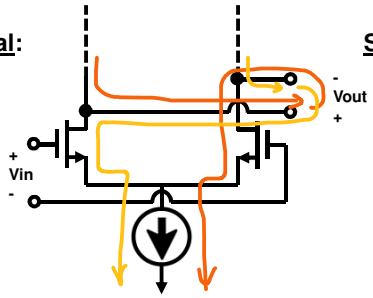
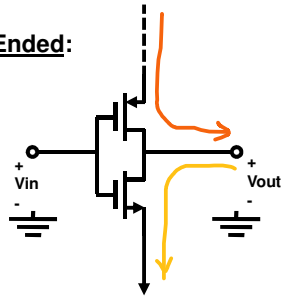
Circuits

Differential:

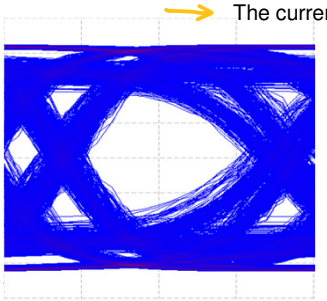


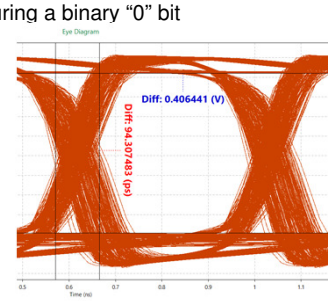
Single-Ended:



The current path during a binary “1” bit

The current path during a binary “0” bit





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Overview

- As channel simulation and IBIS-AMI modeling methods are adapted from serial link to DDR interface analysis, we encounter IBIS I/O models with asymmetric rising and falling edges
- This is different from the highly symmetric drivers we typically encounter with serial link analysis
- Traditional single-step response methods for impulse response generation may not reproduce circuit simulation results accurately enough
- These slides show how an EDA tool can handle this (without changes to the IBIS specification)
- All cases use **Micron**'s **y11a.ibs** file for 8Gbps DDR5

5

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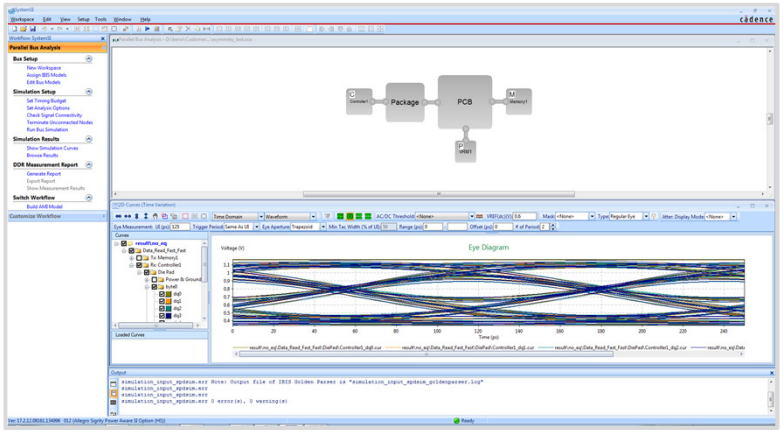
Testbench

- Package block uses an extracted RLCK SPICE model
- PCB block uses W-elements with 0.3 meter lengths



6

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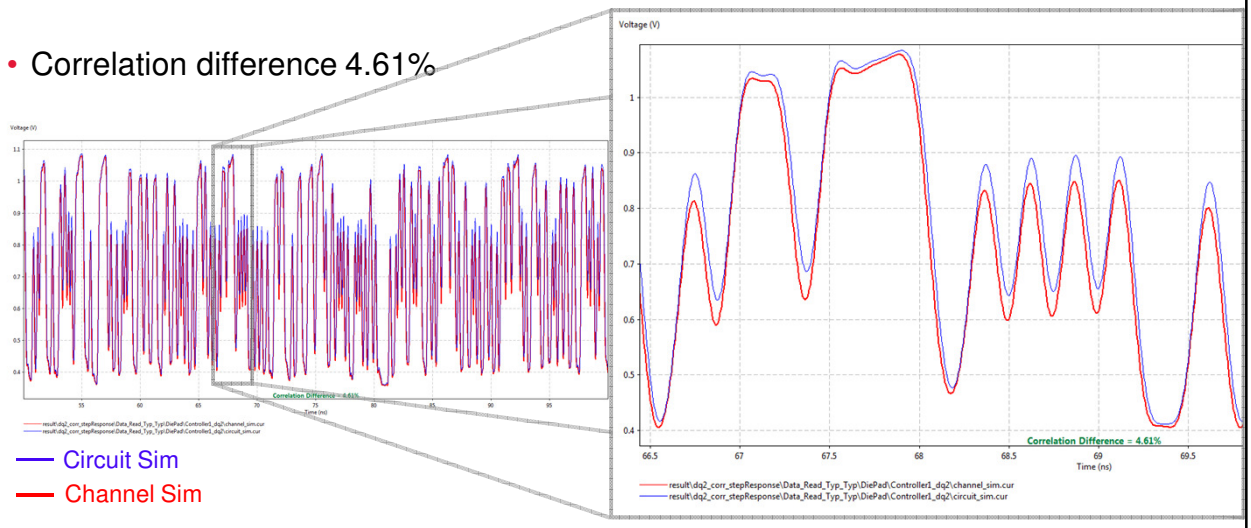
Characterizing with Step Function – One Rising Transition

- Correlation difference 4.61%

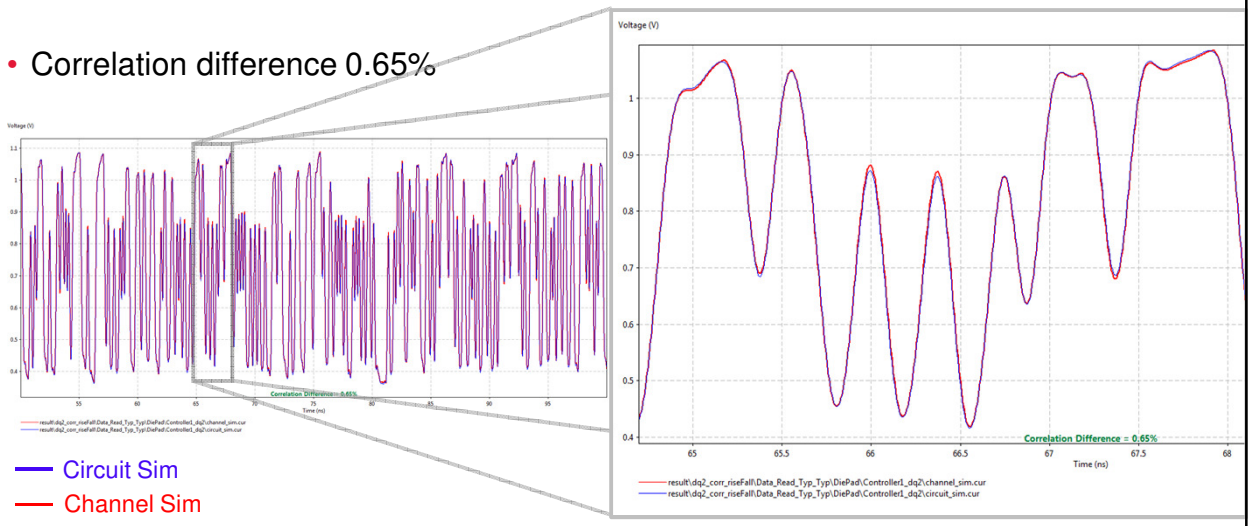


Circuit Sim
Channel Sim

cadence

Characterizing with both Rising and Falling Transition

- Correlation difference 0.65%

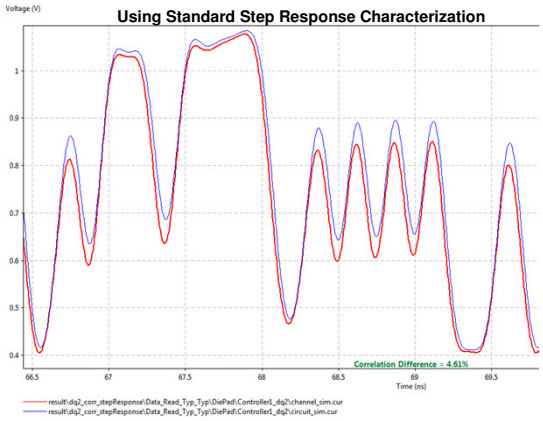


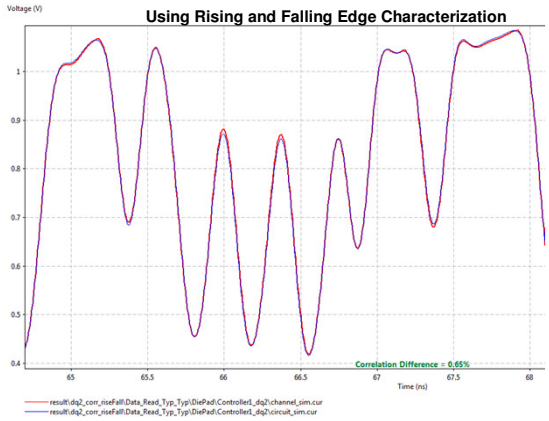
Circuit Sim
Channel Sim

cadence

Comparison between Two Different Methods

- Correlation error vs. circuit simulation reduced by about 4%





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Summary

- The **DQ_34_3600** I/O model has some asymmetry in its rising and falling edges
- Standard SerDes step response characterization did not do a great job in capturing this behavior, as seen in the circuit / channel sim correlation
- Characterization methods using rising and falling edges captured this behavior very well for channel simulation

```
|*************************************************************************
|
[Ramp]
R_load = 50
|
|         typ                        min                        max
|
dV/dt_r 3.7990E-01/6.4024E-11   3.4860E-01/8.7846E-11   4.0938E-01/4.9359E-11
dV/dt_f 4.4605E-01/5.4840E-11   4.2048E-01/7.6564E-11   4.6793E-01/4.2557E-11
|*************************************************************************
```


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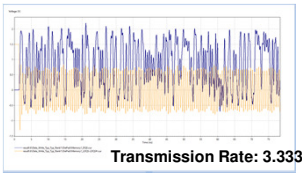
Strobe as Timing Reference

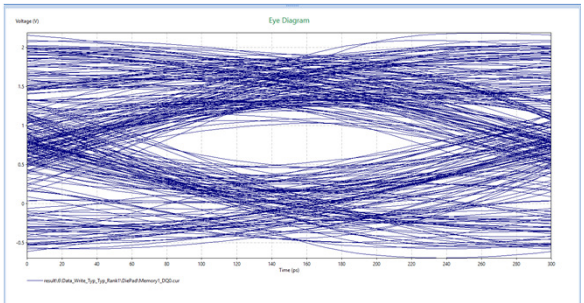
cadence

Overview(1)

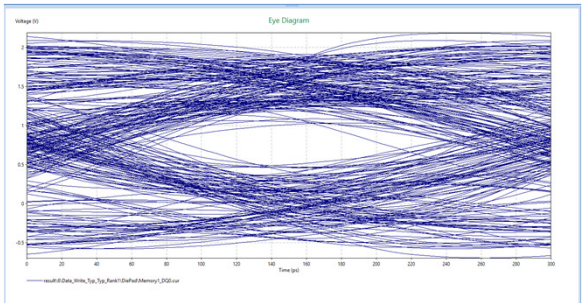
- Different timing reference – Different selection of “trigger” can result in different eye opening



Transmission Rate: 3.333Gbps



Triggered according to ideal UI

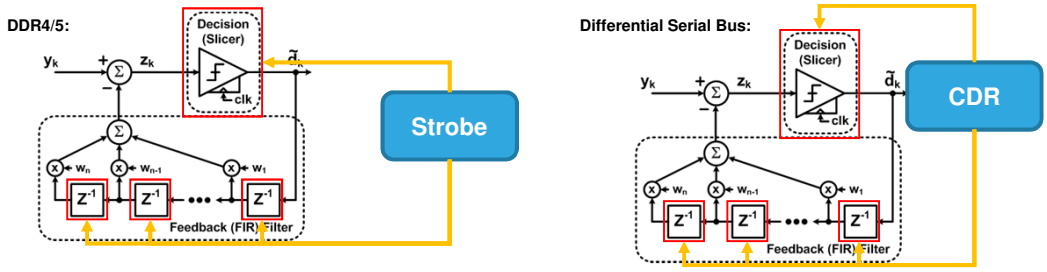


Triggered according to Strobe

cadence

Overview(2)

- DFE's clock in memory bus will be supplied by Strobe rather than CDR, which can be seen in most differential serial bus



- As channel simulation and IBIS-AMI modeling methods are adapted from serial link to DDR interface analysis, serial link CDR algorithms are often used for analysis
- What is the impact?

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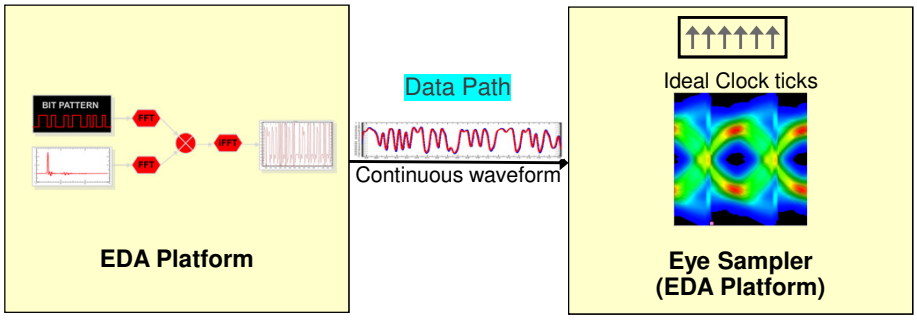
Current CDR-Based Method

- Centers the eye for each individual signal
  - Ideal clock ticks are generated internally by the eye sampler
  - Clock ticks can also be generated by AMI models and sent to the eye sampler



- Some controllers have some individual bit de-skewing

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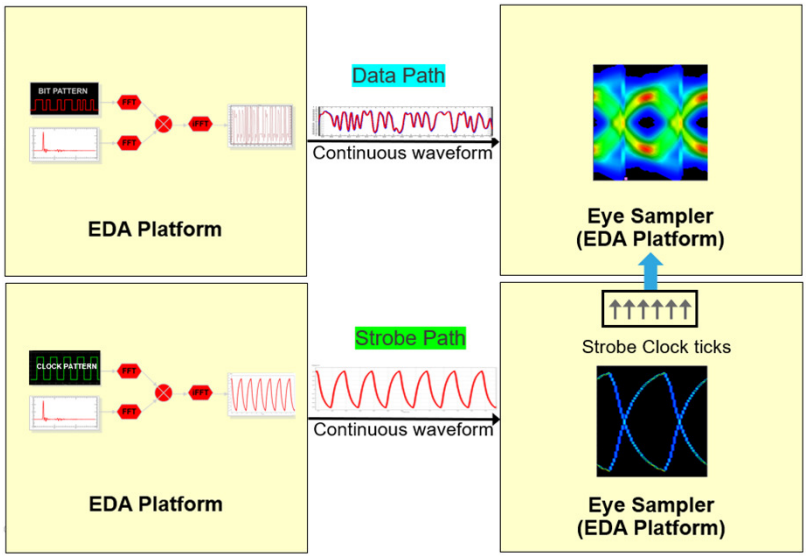
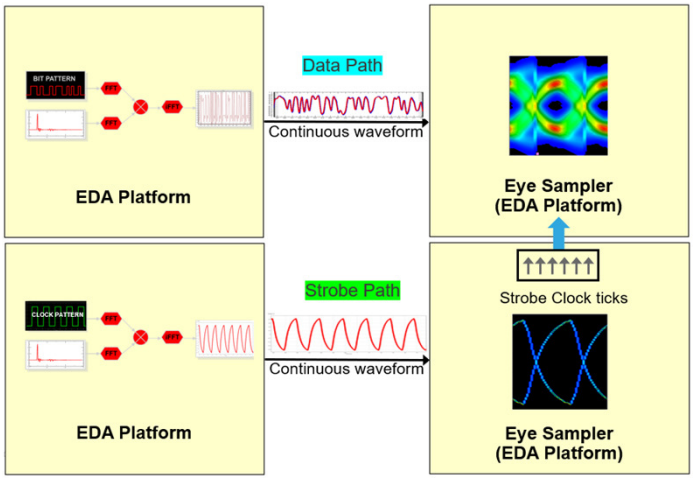
True Strobe Timing (TST)

- Clock ticks are collected from the strobe channel instead of the data channel
  - With real strobe, this is done for entire byte lane
- Strobe channel is only fed with 0101 data



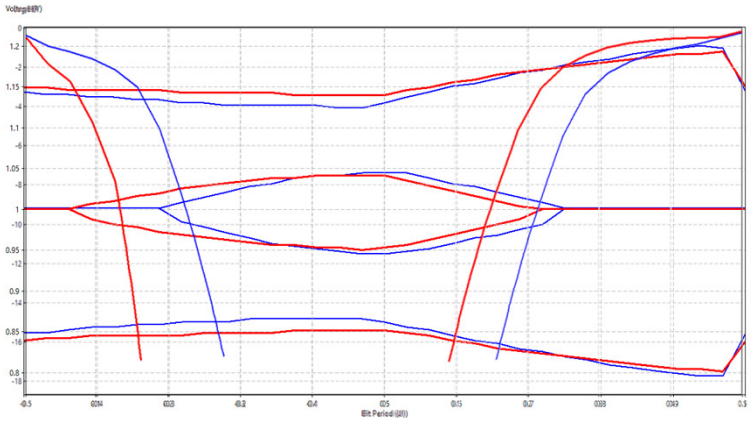
Comparison of Results

- CDR vs. TST
- CDR vs. TST with jitter impairments
- Test configuration
  - 1 data line is used for simulations
  - 6 Gbps
  - Rx CTLE
  - Rx 4 tap DFE
  - In phase between strobe and data



CDR vs. TST

CDR
Strobe



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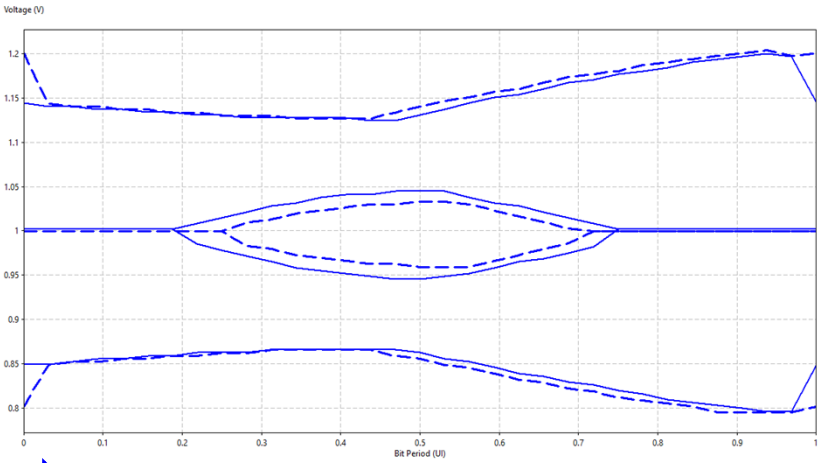
CDR Results with Dj Applied at Tx



5%UI
15%UI

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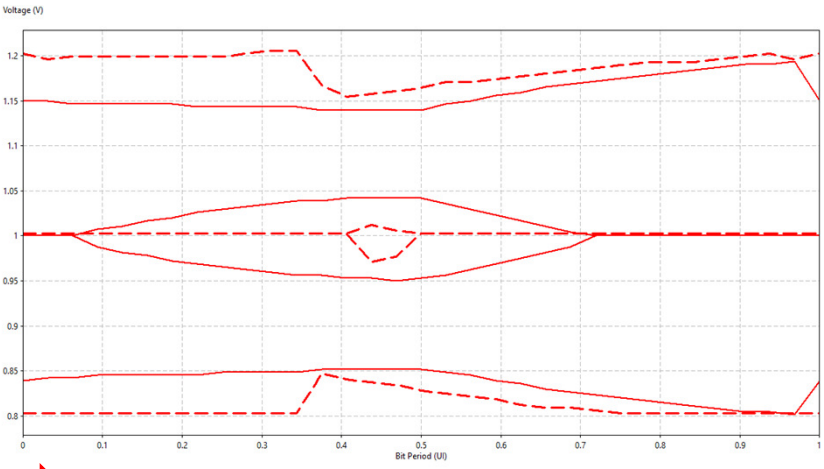
Strobe Results with Dj Applied at Tx



5%UI Dj on both strobe and data

15%UI Dj on both strobe and data

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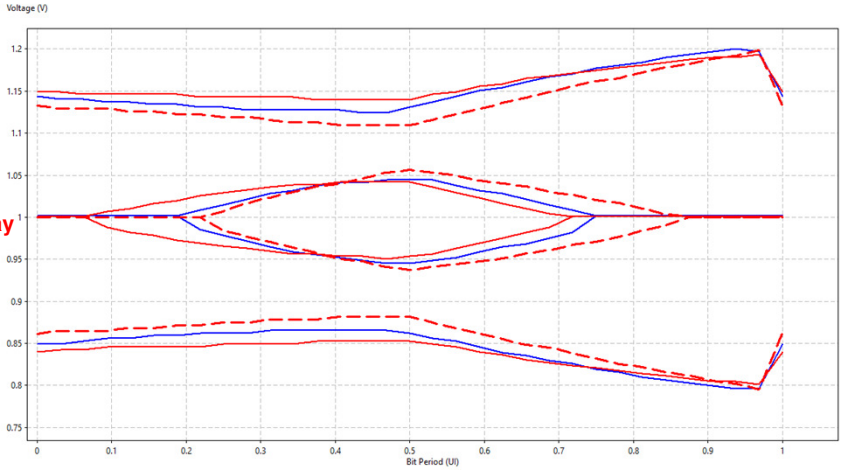
CDR vs. TST

- After delaying by 0.2 UI

CDR
Strobe
Strobe w delay



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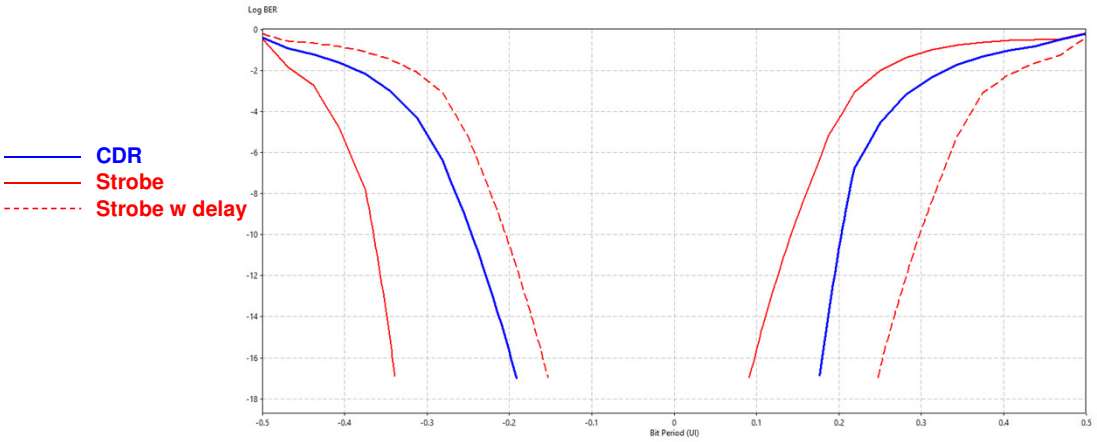
CDR vs. TST

- After delaying by 0.2 UI



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Summary

- Using default CDR instead of actual strobe to get clock risks will miss important impairments/jitter for parallel bus topology
- Analysis results show false optimism using CDR approach as compared to true strobe timing methodology
- Need to model delay accurately

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IBIS File Format Links

Bob Ross, Teraspeed Labs
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Asian IBIS Summit
Taipei, Taiwan
November 4, 2019

(Updated from June 21, 2019 version)
(Presented by Randy Wolff, Micron Technology)

Story of IBIS

- In the beginning … (1993) 1 file format, 8 pages
- Then a committee got involved …
- (2019) … 17 or more formats or links to formats:
  - IBIS Version 7.0 (331 pages)
  - Touchstone 2.0 (34 pages)
  - IBIS-ISS (58 pages)

- Story of file formats given here

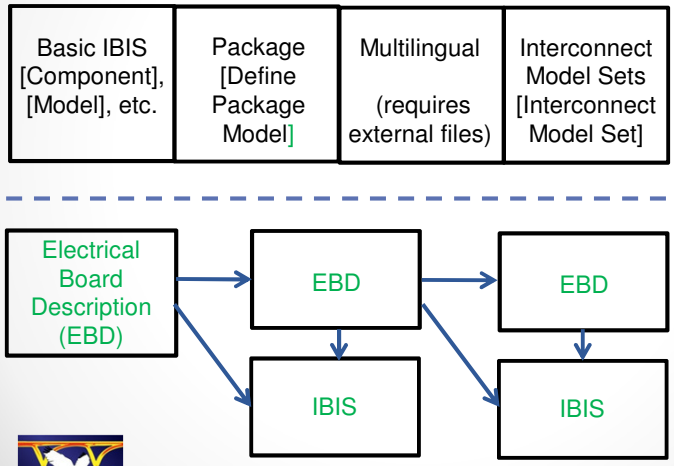
File Format Legend

- Green – Official IBIS formats (ebd, ibs, pkg, ami, ims, Touchstone, Ts4file, executable models, "txt")
  - Checked by ibischk7 (with/without flags) or separately with tschk2
  - Content referenced in EBD and IBIS files are usually parsed (or checked for connectivity only)
  - Note, tschk2 is an independent checker, separate from ibischk7
- Red – Official IBIS format, but no parser (IBIS-ISS)
- Black – Format managed by other specifications or standards
- Touchstone means official Touchstone 1.0 and Touchstone 2.0

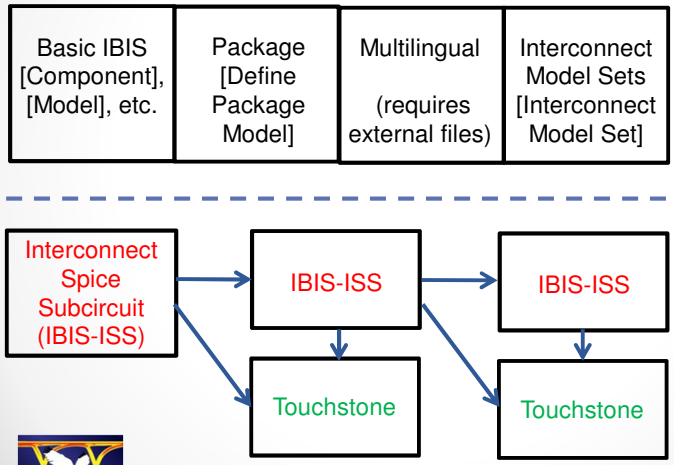
File Name and Extension Reference

- I/O Buffer Information Specification (IBIS) Version 7.0
  - Electrical Board Description (ebd) Section 8
  - IBIS (ibs) Sections 4-6, 12
  - Package Modeling (pkg) Section 7
  - IBIS-AMI (ami), Ts4File (usually s4p),Section 10
  - executable models (usually so, dll) Section 6
  - Interconnect Model Set (ims) Section 11
- Touchstone File Format Specification Version 2.0
  - Touchstone 1.0 (usually sNp)
  - Touchstone 2.0 (usually sNp)
  - Ts4file (usually s4p)
- IBIS Interconnect SPICE Subcircuit (IBIS-ISS) Specification Version 1.0
  - IBIS-ISS (usually iss)

Optional Internal IBIS Content and EBD Links



Optional Internal IBIS Content and IBIS-ISS Links



Basic IBIS External File Links

Basic IBIS [Component], [Model], etc.	Package [Define Package Model]	Multilingual (requires external files)	Interconnect Model Sets [Interconnect Model Set]

ami
Ts4file (subset of Touchstone under ami)
Executable models (dll, so, etc.)

Optional External Package File Link

Basic IBIS [Component], [Model], etc.	Package [Define Package Model]	Multilingual (requires external files)	Interconnect Model Sets [Interconnect Model Set]

pkg

Multilingual External File Links

Basic IBIS [Component], [Model], etc.	Package [Define Package Model]	Multilingual (requires external files)	Interconnect Model Sets [Interconnect Model Set]

ami (for passing parameters)
"txt" (text file for passing parameters)
IBIS-ISS (can call Touchstone and other files)
SPICE (Berkeley Version 3F5)
VHDL-AMS
Verilog-AMS
VHDL-A(MS)
Verilog-A(MS)

Interconnect Model Set External File Links

Basic IBIS [Component], [Model], etc.	Package [Define Package Model]	Multilingual (requires external files)	Interconnect Model Sets [Interconnect Model Set]

ims
IBIS-ISS
Touchstone

File Formats With IBIS

- ebd
- ibs
- ami
- Executable models (dll, so, etc.)
- Ts4file
- pkg
- ami (for parameter passing)
- "txt" text format (for parameter passing)
- IBIS-ISS
- SPICE
- VHDL-AMS, Verilog-AMS, VHDL-A(MS), Verilog-A(MS)
- ims
- Touchstone 1.0, Touchstone 2.0

Example of EBD to IBIS to IMS Linkage (Without Details)

```
abc.ebd
U1.23 …
U1.24 …
[Reference Designator Map]
U1   def.ibs   DEF
```

```
def.ibs
[Component] DEF
[Pin]
23 IO1 IO_Buf
24 IO2 I0_Buf
[Interconnect Model Group]
GHI   ghi.ims
[End Interconnect Model Group]
```

```
ghi.ims
[Interconnect Model Set] GHI
[Interconnect Model] Pin23
File_IBIS-ISS  jkl.iss  pin23
1 pin_name 23
[End Interconnect Model]
|
[Interconnect Model] Pin24
File_TS        mno.s1p
1 pin_name 24
2 A_gnd
[End Interconnect Model]
[End Interconnect Model Set]
```

EBD: Pins 23, 24 in abc.ebd → def.ibs →ghi.ims
and terminal 1 used for 23 in ghi.ims → jkl.iss
and terminal 1 used for 24 in ghi.ims → mno.s1p

```
jkl.iss
.subckt pin23 1
R_term 1 0
.ends
```

```
mno.s1p
…
0 1 0
2 0.9 0.005
…
```

ibischk7 –ebd abc.ebd checks abc.ebd, def.ibs, ghi.ims

Observations

- 17 or more file format links in IBIS
- 12 or more file formats supported by IBIS Specifications or by format restrictions
  - Restrictions means requirements in certain files such as executable models, parameter passing formats and Ts4file
- ibischk7 and tschk2 check syntax and content of files
  - Individual files by flags –ebd, -pkg, -ami, -ims
  - Top level files AND linked files
  - tschk2 conversions: Touchstone 1.0 ←→ Touchstone 2.0
- Some checking or linking is not defined (e.g., to Touchstone, IBIS-ISS)

Past and Future File Formats

- Past (unused formats)
  - Rail Version 1.2 (ral) and railchk1 (for timing)
  - IBIS Interconnect Modeling Specification (ICM) Version 1.1 (typically icm) and icmchk1
- Possible future file formats and links
  - Electrical Module Description (EMD) with links to emd, ems, ibs, IBIS-ISS, and Touchstone
  - Touchstone advances
- A lot has happened and is happening in the IBIS Committee