Innovations in DDR Memory Simulation

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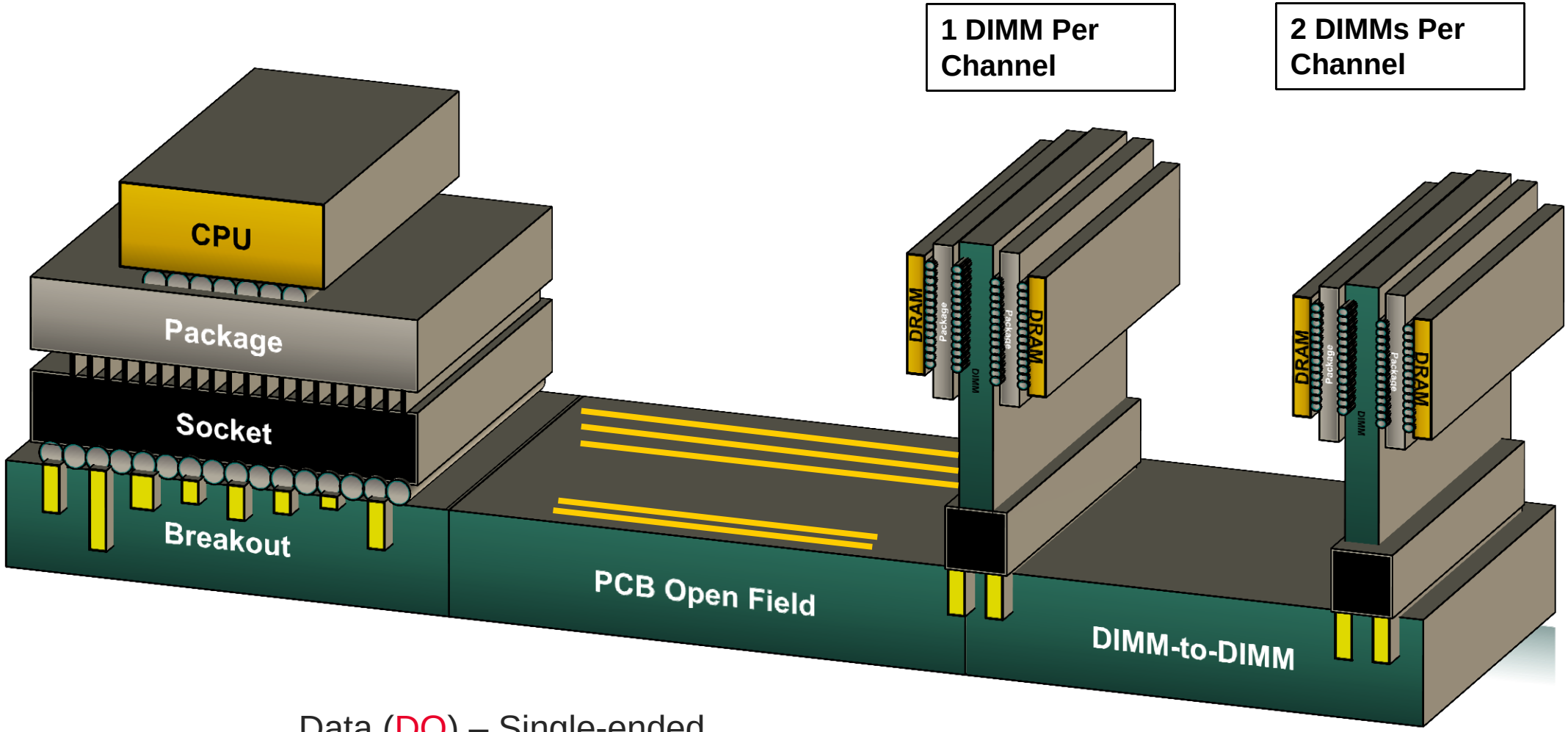
A Typical DDR5 Application



Data (DQ) – Single-ended
Data Strobe (DQS) – Differential
Microstrip & Stripline

What Does it Mean to Succeed?

THE MEASURE OF SUCCESS FOR A PRODUCT WITH DDR5

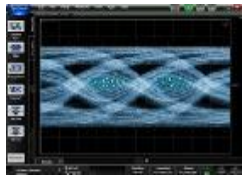
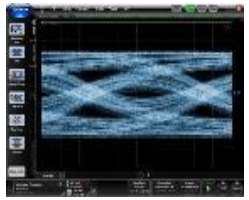
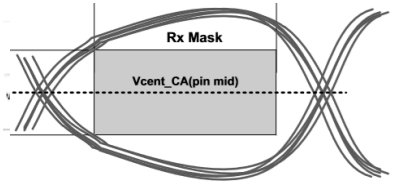
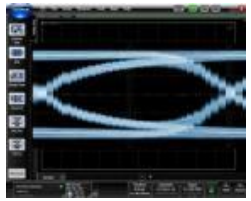
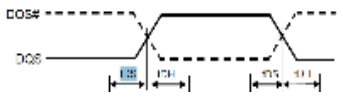
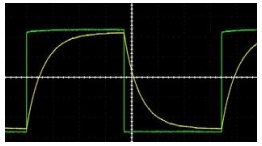
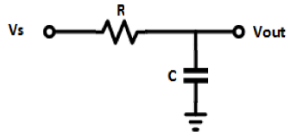
- No system failures, under stress
  - At Max and Min temperatures
  - Using multiple vendors' DIMMs
  - 1 DIMM slot and 2 DIMM slots filled
  - Running diagnostic software that stresses the memory access
  - Graceful performance degradation

"I can stop testing when I'm certain my manager is satisfied with the product quality risk"

Source: Burn-in environment test chambers by EDA-Industries S.p.a

How Did we Get to DDR5?

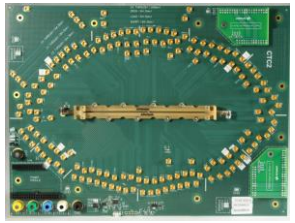
A ROAD PAVED BY INNOVATION

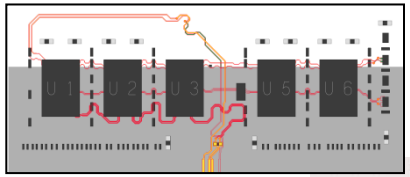
Signal	MT/s	Generation	Characteristics	Specification	Introduction
	4200 – 8000+	DDR5+	"Hyper Speed" • Eye collapses • Impulse response • BER Rj/Dj, Rn/Dn		2019
	1600 – 4200	DDR4	"Serial Speed" • Eye Diagrams • Rx Masks • Bit error rates		2014
	200 – 1600	DDR/2/3	"High Speed Digital" • Transmission lines • Ts / Th, Skew		2002
	33 – 133	SDRAM	"Low Speed" • Fanout • Capacitance		1961

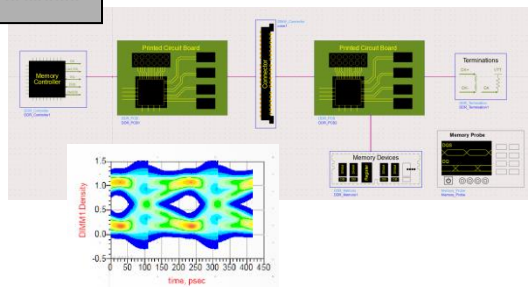
KEYSIGHT TECHNOLOGIES

Ensuring First Pass Success - One Layer Deeper

ENSURING THE SYSTEM IS PERFORMANT AND RELIABLE







Logic / Protocol

Power Integrity

Probing

DDR Methodology

Rx Test

Test Fixtures

Modeling and Simulation

Tx Test

KEYSIGHT TECHNOLOGIES

Change, Challenges and Solutions

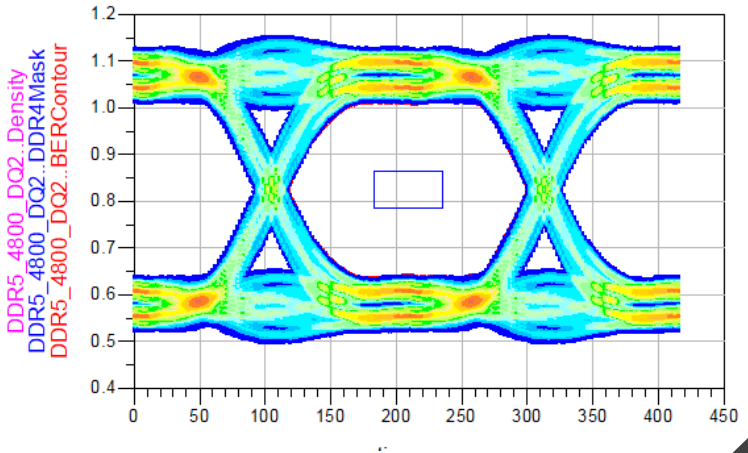
1. Crosstalk, Jitter and Bit-Error-Rate (BER) Specs
2. Closed eyes need equalization and training
3. Innovations in Simulation and Modeling of DDR5 & LPDDR5 systems

1. Crosstalk, Jitter and Bit-Error-Rate (BER) Specs

Crosstalk

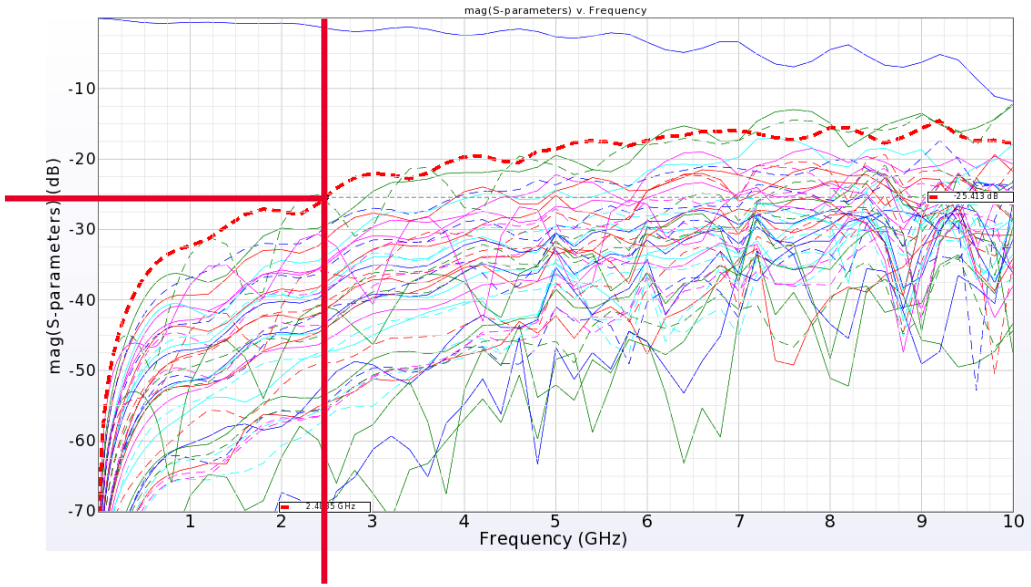
THE IMPORTANCE OF THE SIGNAL RETURN PATH

DDR5-4800

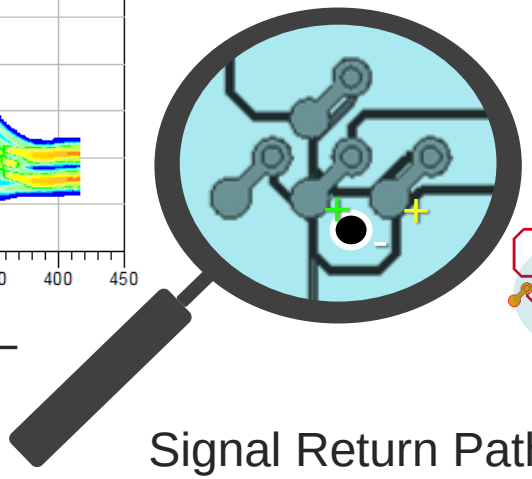


No Crosstalk, No Jitter –
Just ISI from Channel

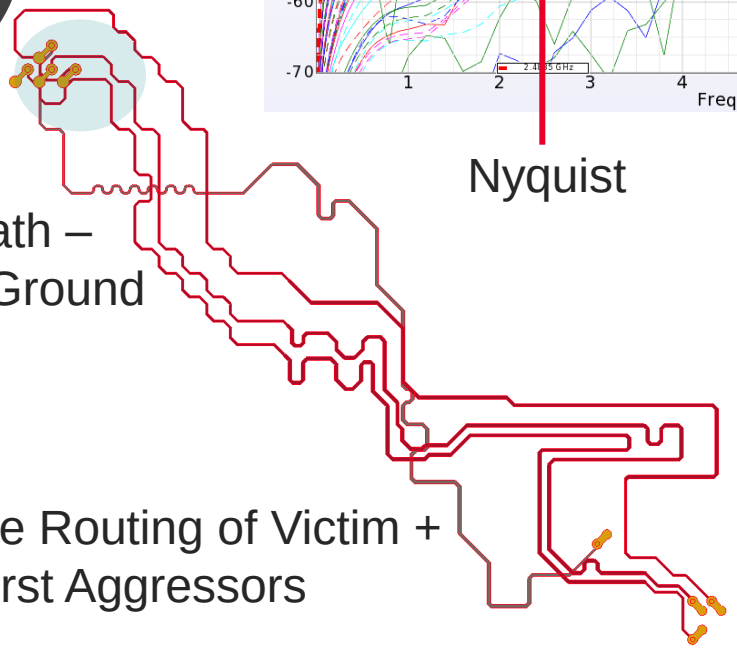
< -25dB



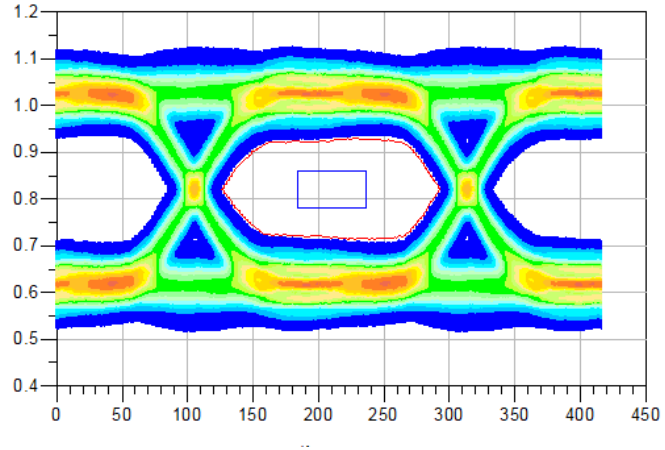
Nyquist



Signal Return Path –
through shared Ground
Pin



PCB Trace Routing of Victim +
Worst Aggressors



With Crosstalk

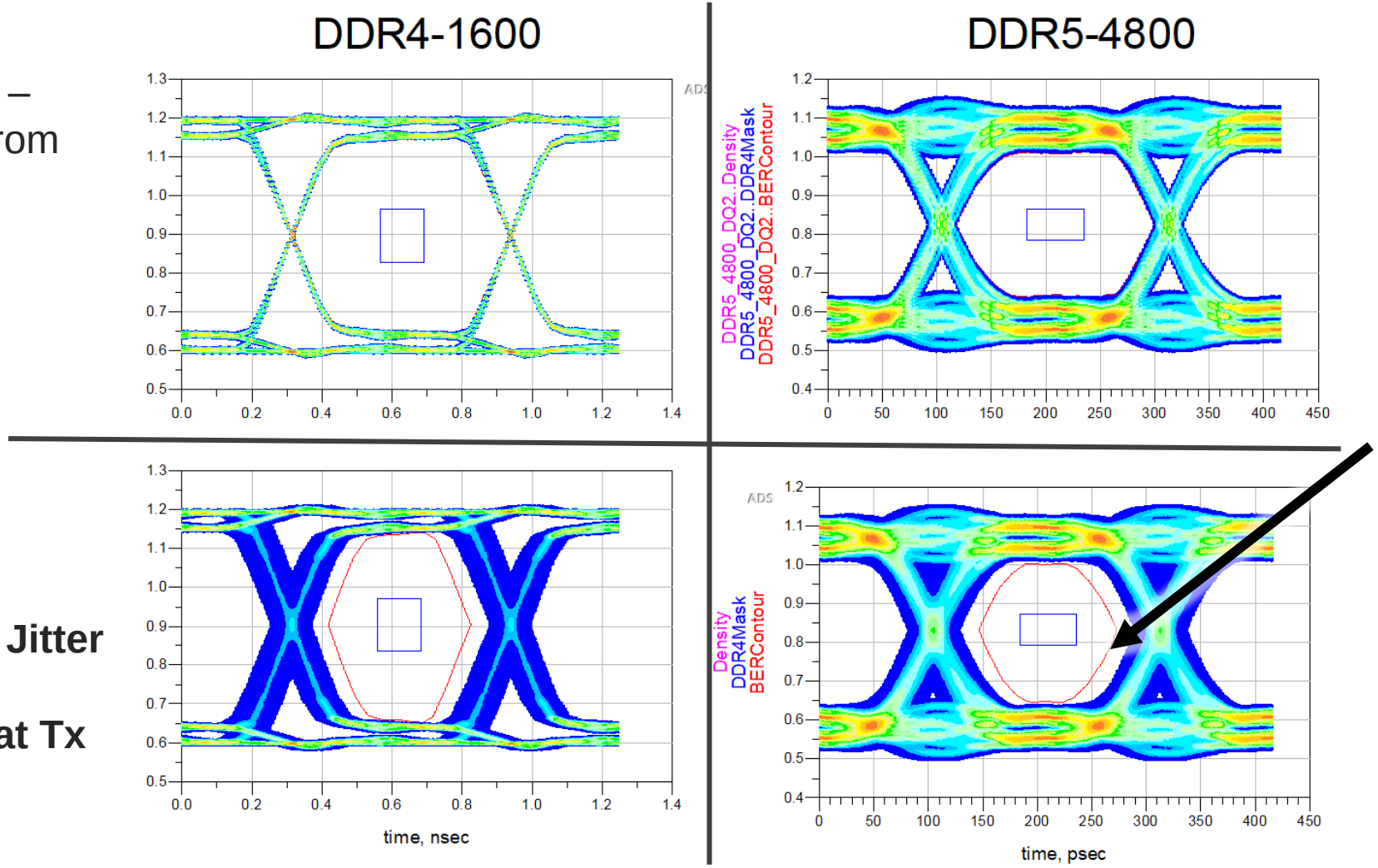
Jitter

Jitter injected at Tx, and eye measured at the DRAM Solder-Ball (Rx Input)

BER CONTOUR AT 1E-16 TELLS US THE REAL MARGIN

No Jitter – Just ISI from Channel

Random Jitter = 0.02 UI Applied at Tx (2%)



No Jitter – More ISI from Channel due to higher speed

47% Reduction in Timing Margin

(27ps less margin to mask)

Specs Becoming More Bit-Error-Rate Focused

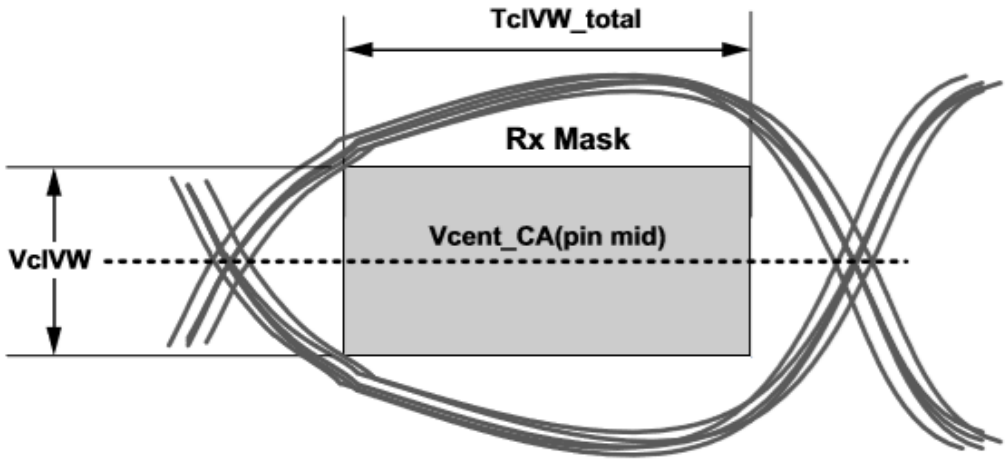


Figure 179 — CA Receiver (Rx) mask

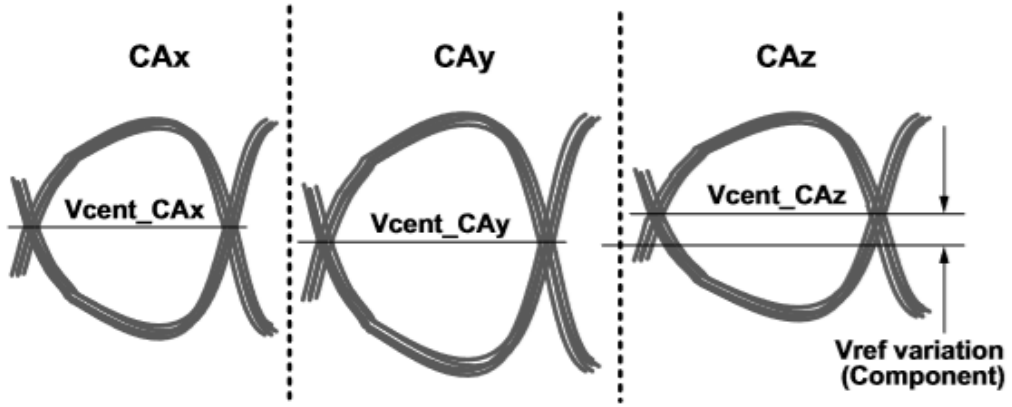


Figure 180 — Across pin $V_{REF}CA$ voltage variation

- From the draft spec:
  - Maximum Jitter (Dj, Rj and DCD) specifications for Tx and Rx components
  - For Tx and Rx Voltage and Timing tests, system BER is e-16 and requires 5.3e9 minimum UIs for validation (99.5% confidence level)
  - New receiver stressed-eye tests for components and DIMMs

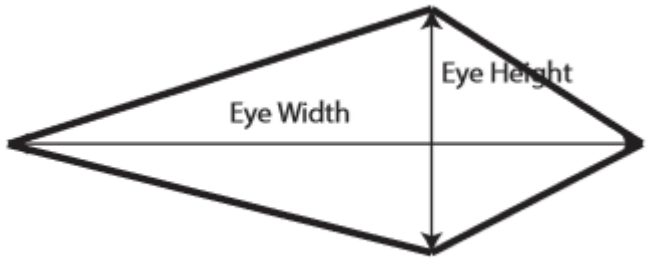


Figure 196 — Example of Rx Stressed Eye Height and Eye Width

Stressed Eye is calibrated to a specified height and width. The DIMM, DRAM or Memory Controller Rx must be able to receive to the system BER

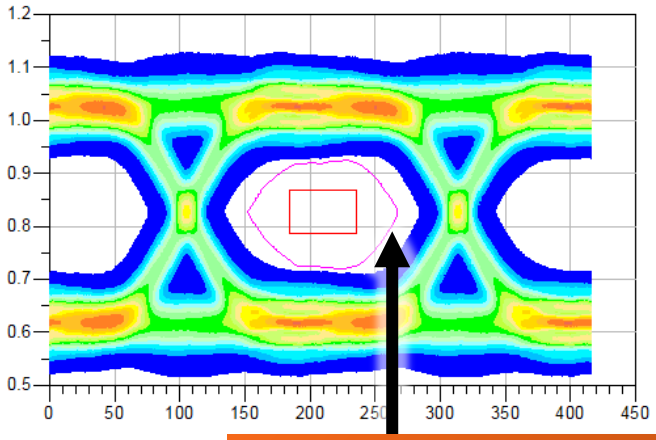
Crosstalk, Jitter & BER Specs

KEY INSIGHTS

- Jitter and Crosstalk are Very Significant
- Simulation must predict Eye closure due to Random Jitter down to the system BER (1e-16) in a practical time
- EM simulation must capture Crosstalk accurately

DDR5-4800

Jitter, crosstalk & Channel ISI



64% Reduction in Voltage Margin

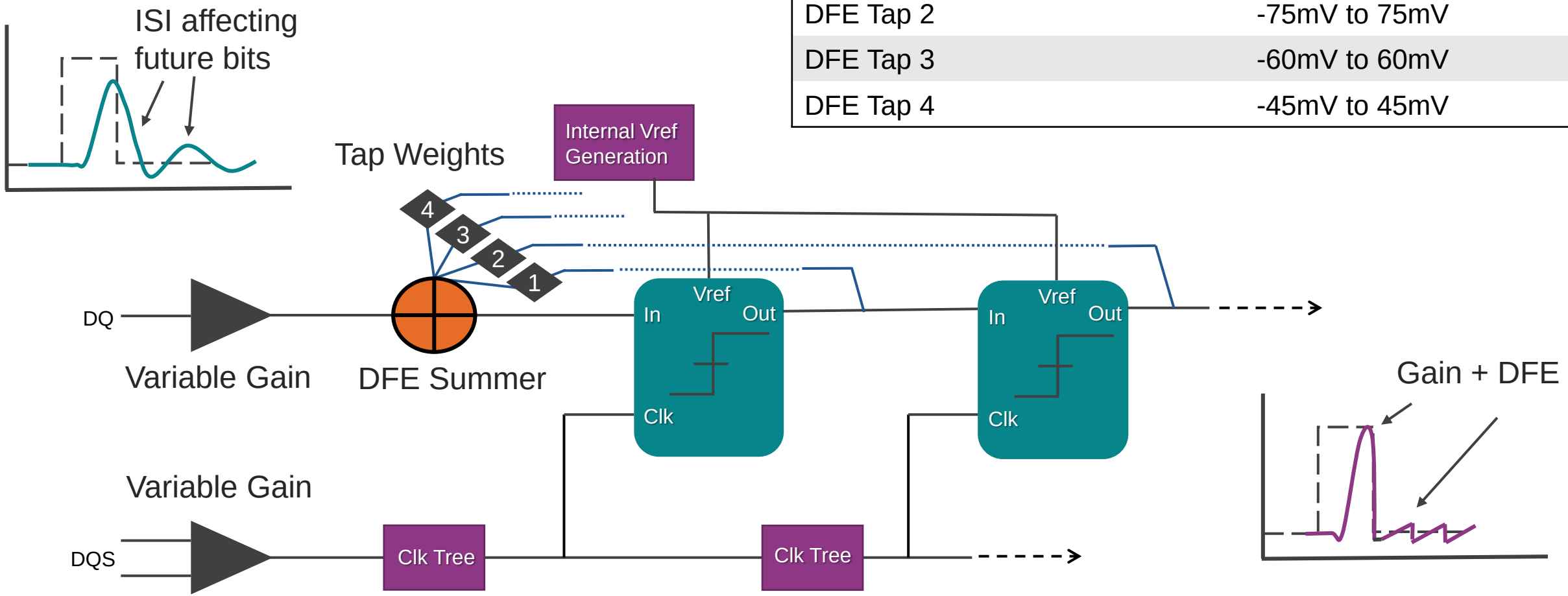
63% Reduction in Timing Margin

2. Equalization and Training

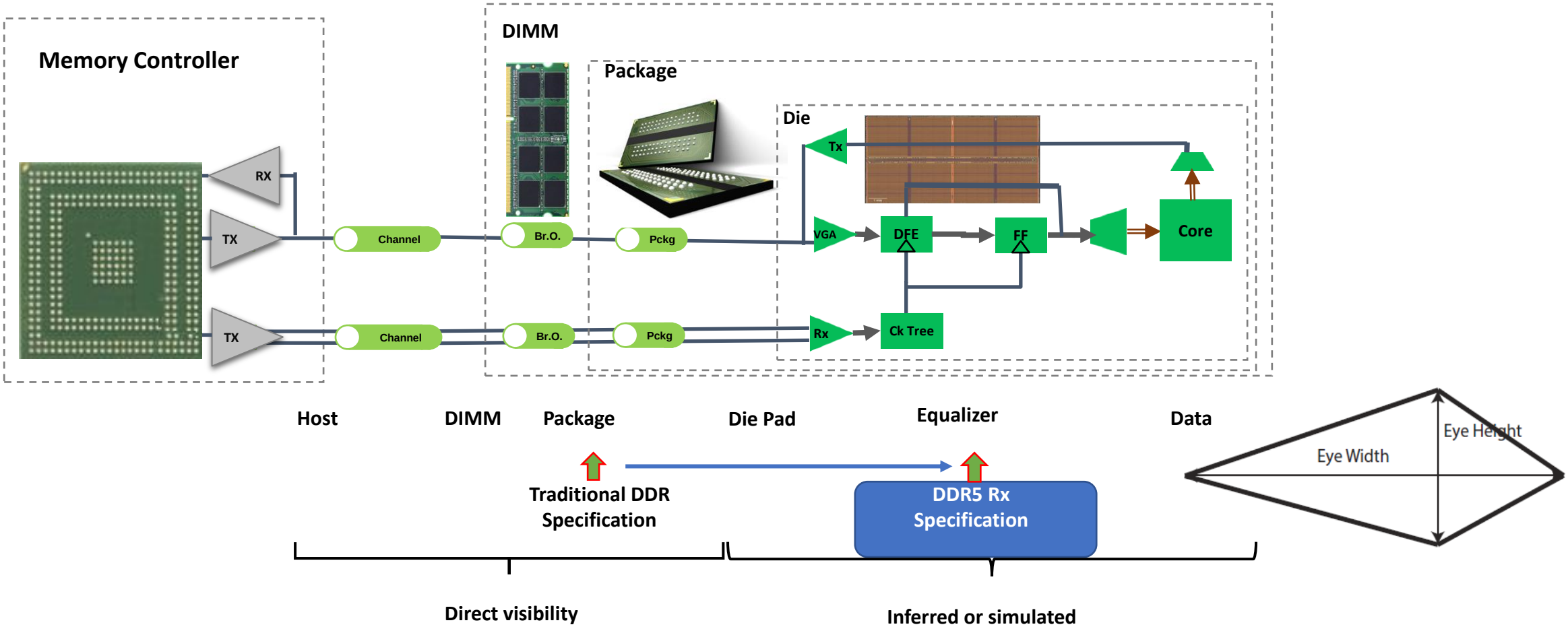
Rx Equalization

FIRST TIME TO HAVE DFE ON DRAM!

Mode Register Settings (per DQ)	*All values subject to change*
Variable Gain	-6dB to 6dB
VrefDQ	-3 to +3 Offset steps
DFE Tap 1	-200mV to 50mV
DFE Tap 2	-75mV to 75mV
DFE Tap 3	-60mV to 60mV
DFE Tap 4	-45mV to 45mV

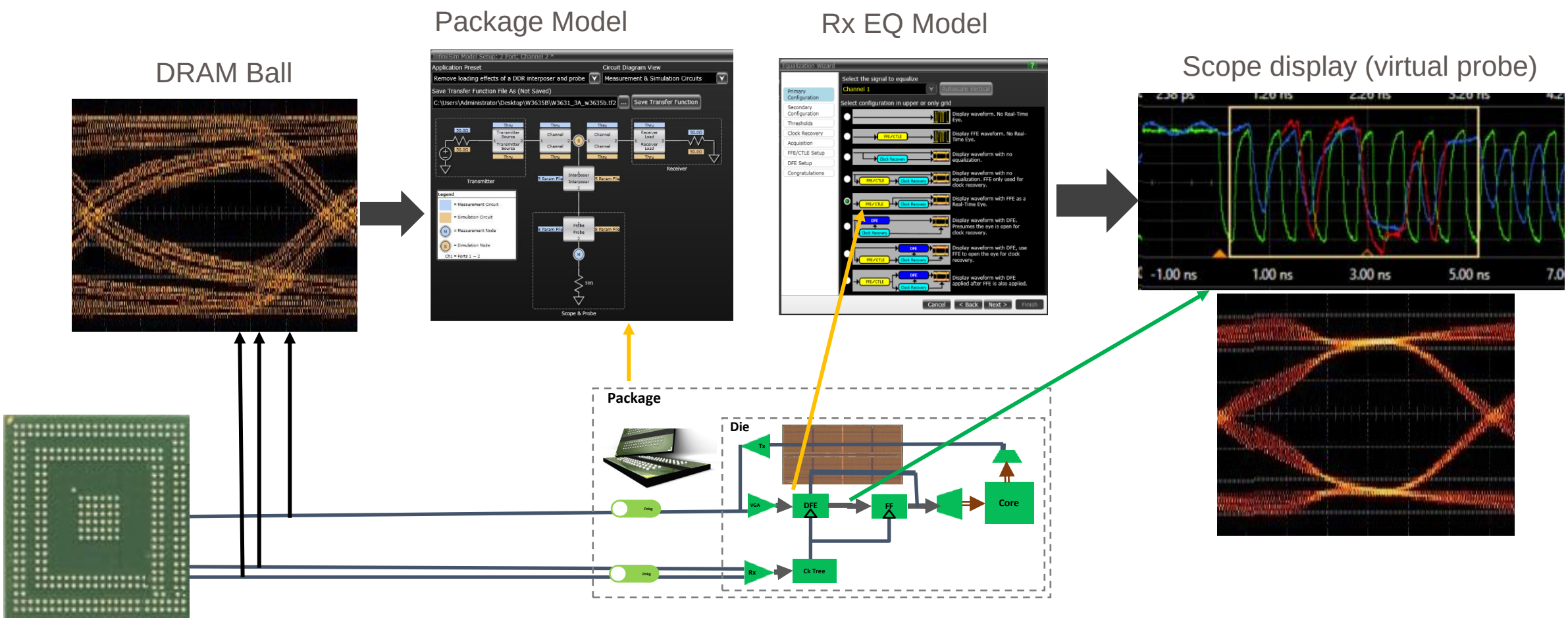


DDR5 Rx Specifications are Inside the Die

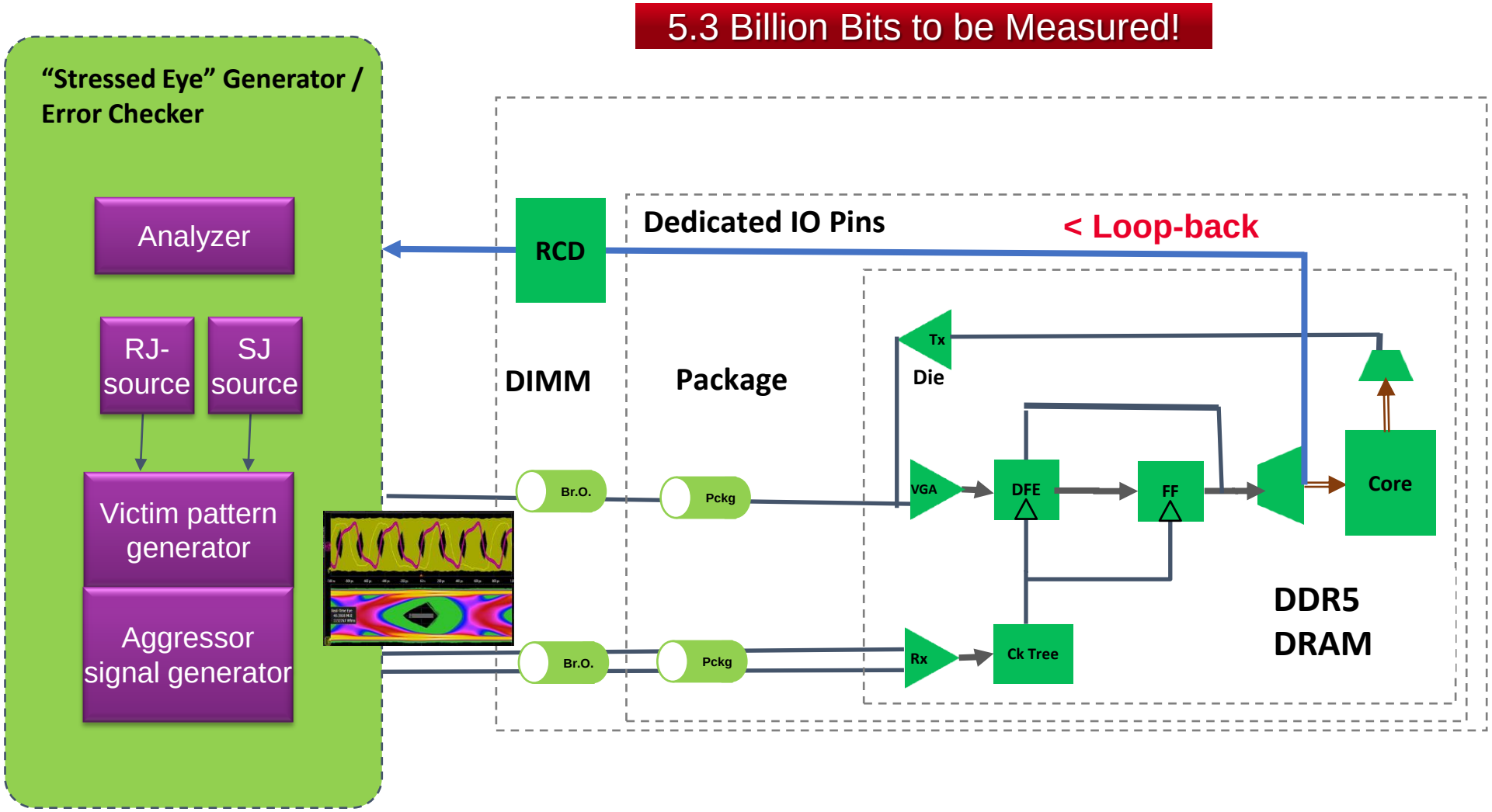


DDR5 Tx Test: New Methodology Needed

VIRTUAL PROBING INSIDE THE DIE



DDR5 Rx Test: New DRAM Feature - Loop-Back Mode



Skew Adjustment with Write-Leveling

- Due to the fly-by topology of the clock for DDR4 & DDR5, the Clock (Clk) is inevitably skewed to the DQS at each of the independent DRAM

- The controller has ability to adjust skew between DQ's, DQS and the Clock signal.
- DQS is adjusted to match the Clk first, then internal alignment of each DQ is performed (via mode register) to remove DQ-to-DQS skew (due to the package and die)

Equalization and Training

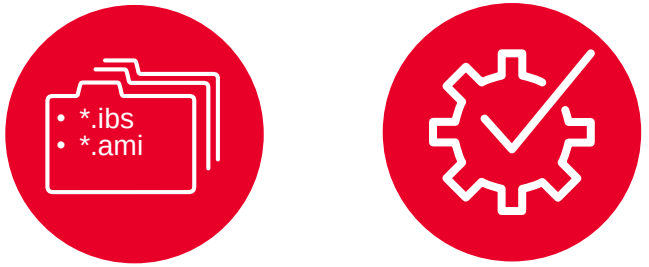
KEY INSIGHTS

- Possible to have a Closed eye at input to Rx
- Optimal Eye opening depends on:
  - Vref setting (per DQ)
  - Gain Setting (per DQ)
  - DFE Tap settings (4 taps per DQ)
  - Timing of DQS to DQ
  - Write-leveling (skew adjustment)

3. Innovations in Simulation and Modeling of DDR5 & LPDDR5 systems

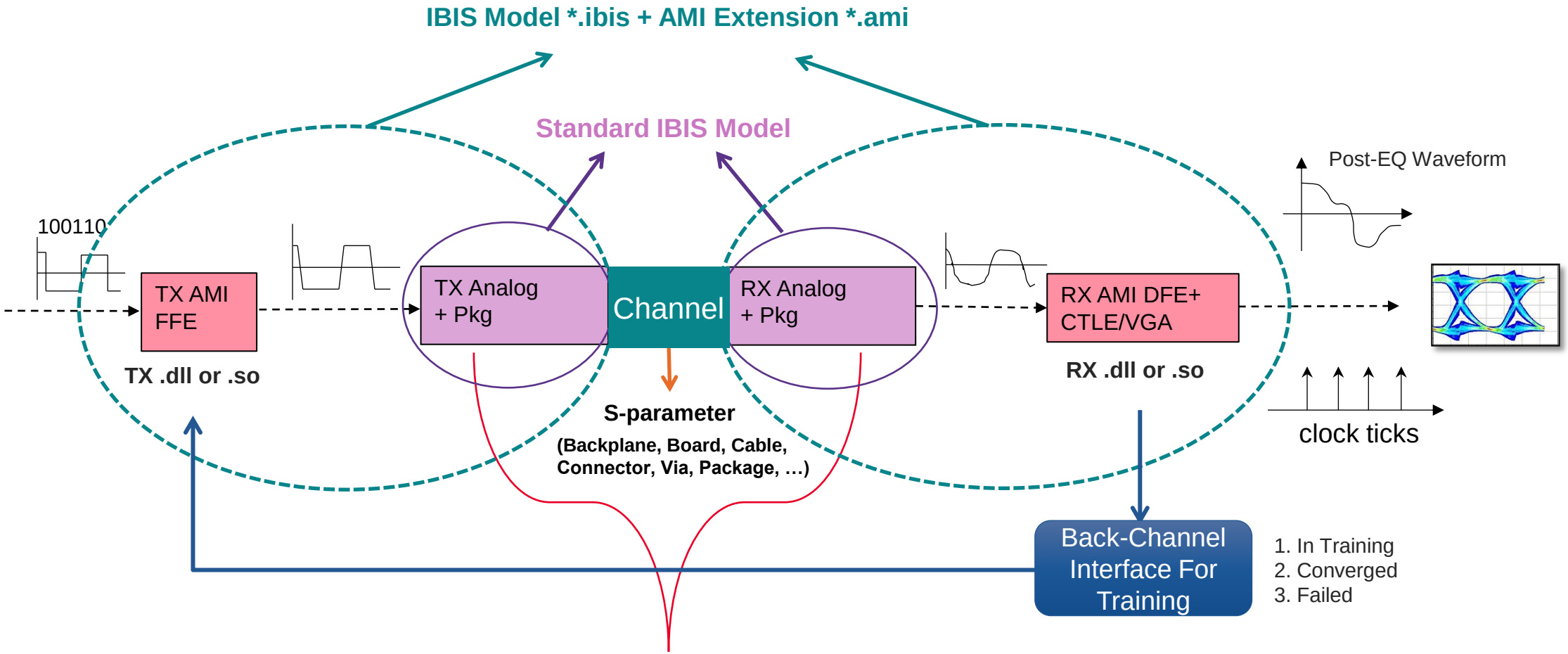
Introducing IBIS AMI for DDR Signals

- EQ Necessary for TX: 3 Tap Pre-Emphasis (Feed Forward Equalization)
- EQ Necessary for RX: CTLE/VGA/DFE
- IBIS-AMI offers
  - Portability – One IBIS-AMI mode can run on many EDA tools
  - IP Protection – Digital signal processing behavior is concealed in model DLL/shared object
  - Interoperability - IC Vendor A🡐🡒IC Vendor B (AMI defines a common interface between the vendor model and the EDA channel simulator)
  - Non-linearity – As complex as the model vendor wishes the model to be
  - Performance – Ultra low BER simulations in seconds not days over the traditional SPICE simulation
- AMI has been widely adopted by IC, system and EDA companies for SerDes signals but this is the first application to DDR single-ended signals.



How Does Standard IBIS-AMI Work?

CHANNEL SIMULATION



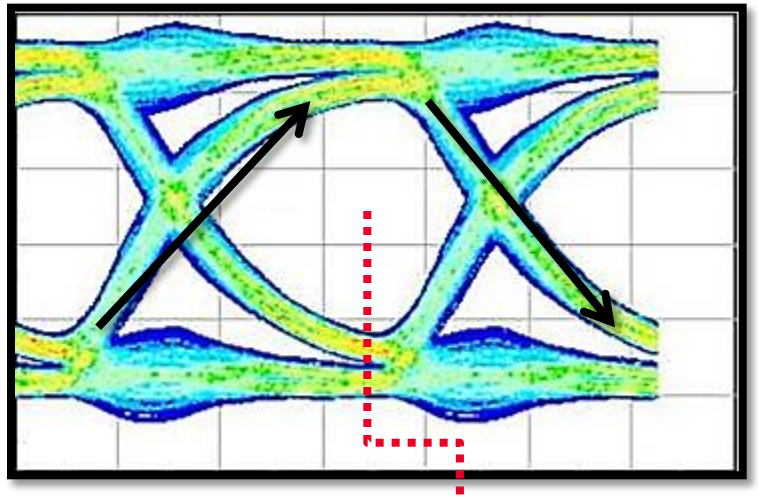
Impulse response of a Linear Time Invariant Network

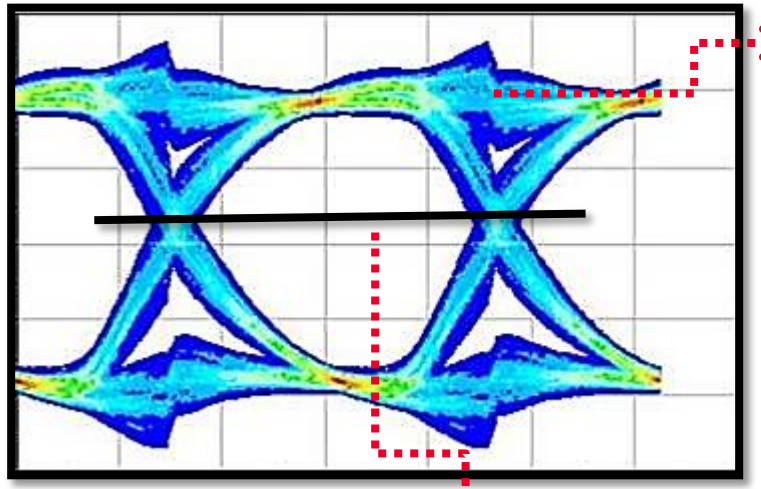
What Do We Need for DDR5 AMI To Work?

SUPPORTING PARALLEL, SINGLE-ENDED SIGNALS WITH EXTERNAL CLOCKS

Input to DRAM

After Gain & 4 Tap DFE





DFE Clocked by DQS:

- Correlated Jitter on DQ & DQS cancels out
- Uncorrelated Jitter on DQS is transferred to DQ

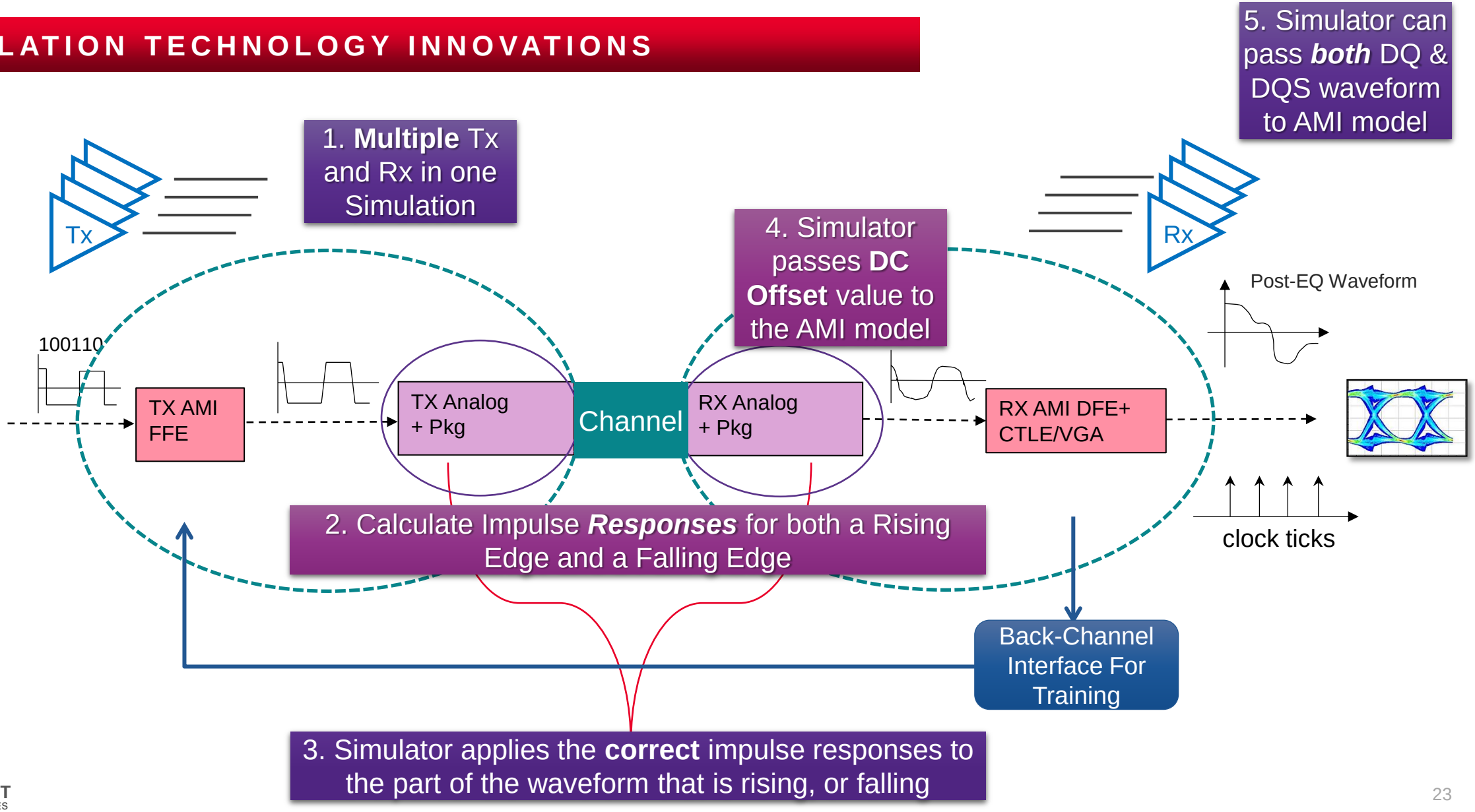
Single-Ended Signal
can have a DC Offset

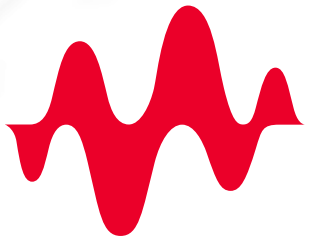
Asymmetric Eye:
Rise Time ≠ Fall Time

Asymmetric Eye:
Crossing Points are shifted in the Equalized Eye

The Solution

SIMULATION TECHNOLOGY INNOVATIONS





KEYSIGHT
TECHNOLOGIES