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shaping tomorrow with you

Expectations for the new package model specification of IBIS 7.0

Masaki Kirinaka
mkirinaka@fujitsu.com
Akiko Tsukada
tsukada.akiko@fujitsu.com
FUJITSU INTERCONNECT TECHNOLOGIES LIMITED

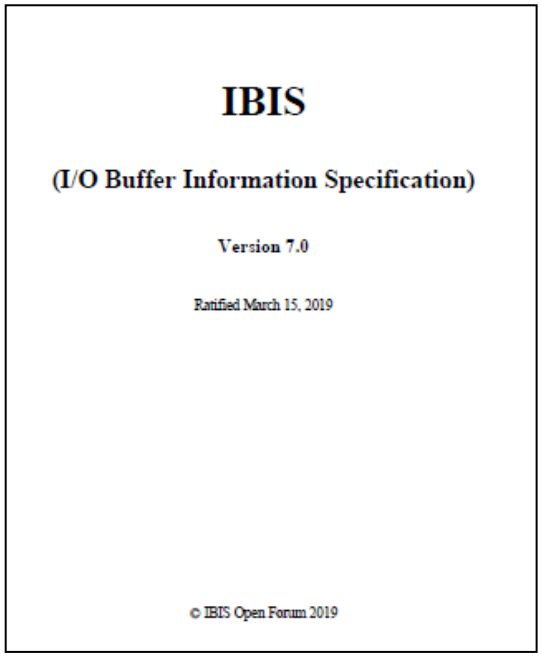
Asian IBIS Summit
Tokyo, JAPAN
November 8, 2019

Agenda

- Introduction
- IBIS 7.0 INTERCONNECT MODELING Outline
- Expectations for IBIS7.0 INTERCONNECT MODELING
- Post-layout simulator issues when using the IBIS 7.0 INTERCONNECT MODEL
- Summary

Introduction

- In March this year, a new interconnect modeling specification was released in IBIS 7.0.
- Therefore, this time, we predicted the superiority of this specification in SI analysis and PI analysis by comparing with the conventional model.
- It also describes the predicted post-layout simulator issues when using the IBIS 7.0 INTERCONNECT MODEL.



IBIS 7.0 INTERCONNECT MODELING Outline

- IBIS 7.0 INTERCONNECT MODELING is a new specification for package modeling.

SIGNAL modeling part

Refer to page 294-295 of ver7_0.pdf

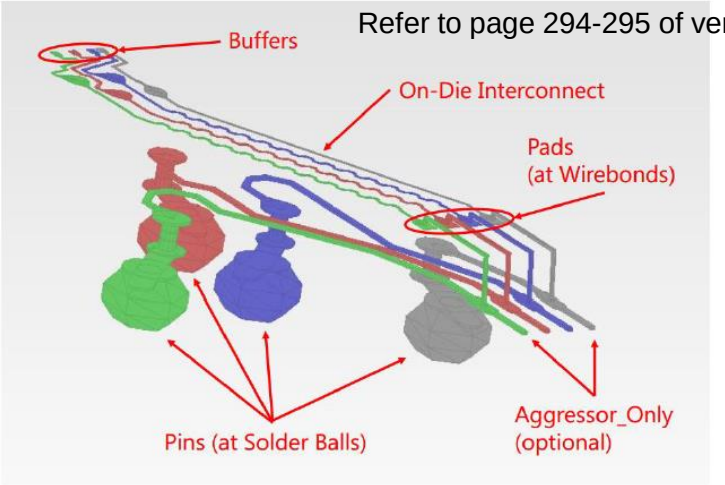


Figure 45 – Package and On-die Substrate I/O Paths

Model path1: (a)Buffer~Pad + (b)Pad~Pin

IBIS Keyword: (a)Buffer_I/O~Pad_I/O
(b)Pad_I/O~Pin_I/O

Model path2: (c)Buffer~Pin

IBIS Keyword: (c)Buffer_I/O~Pin_I/O

PDN modeling part

Refer to page 294-295 of ver7_0.pdf

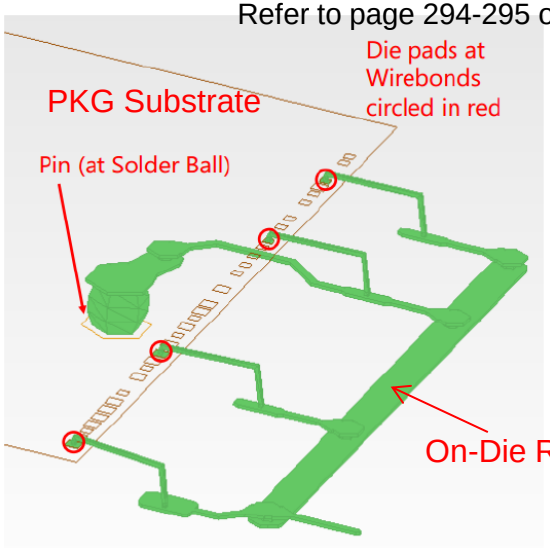


Figure 46 – Package Substrate Rail Terminals

Model path1: (d)Buffer~Pad + (e)Pad~Pin

IBIS Keyword: (d) Buffer_Rail(Pullup_ref, Pulldown_ref)~Pad_Rail
(e)Pad_Rail~Pin_Rail

Model path2: (f)Buffer~Pin

IBIS Keyword: (f)Buffer_Rail(Pullup_ref, Pulldown_ref)~Pin_Rail

IBIS 7.0 INTERCONNECT MODELING Outline

- From single L,C,R value to IBIS-ISS or Touchstone.

Conventional package modeling

```
[Component]     CPU
[Package]
|             typ         min          max
R_pkg     400m      390m       450m
L_pkg     1.90nH   1.40nH     2.20nH
C_pkg     0.40pF    0.30pF     0.80pF
|
[Pin]          signal_name model_name   R_pin       L_pin       C_pin
B7             DQ1         DQ                   390m      1.4nH       0.47pF
|
[Package Model] FBGA_1000
```

The [Define Package Model] is present in the .ibs file or the .pkg file.

```
[Define Package Model] FBGA_1000
[Number of Pins] 500
|
[Pin Numbers]
B7  | DQ1
|
[Inductance Matrix] Sparse_Matrix
|
[Row]  B7
B7    1.4e-9
|
[Capacitance Matrix] Sparse_Matrix
|
[Row]  B7
B7   0.47e-12
|
[Resistance Matrix] Sparse_Matrix
|
[Row]  B7
B7    390e-3
```

IBIS 7.0 INTERCONNECT MODELING Outline

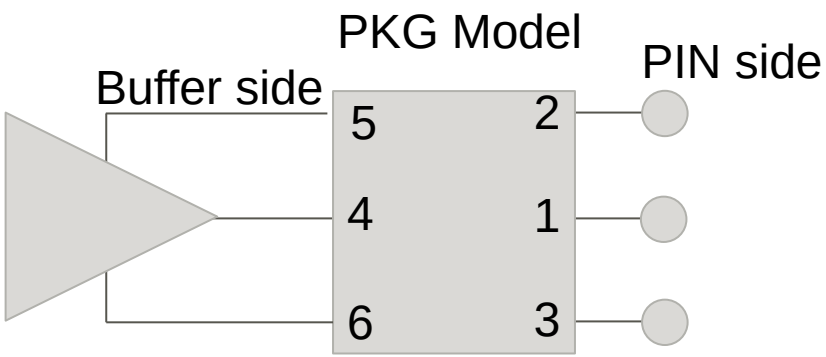
IBIS 7.0 INTERCONNECT MODELING by IBIS-ISS (Spice)

.ibs file

```
[Component]     CPU
[Interconnect Model Group] Full_ISS_PDN_1
Full_ISS_PDN_1     NA
[End Interconnect Model Group]
[Pin] signal_name model_name R_pin L_pin C_pin
A1    DQ1      DQ
P1    VDD      POWER
G1    VSS      GND
```

The [Interconnect Model Set] is present in the .ibs file.
(May be provided as an **.ims** file.)

```
[Interconnect Model Set] Full_ISS_PDN_1
|-----
[Interconnect Model] Full_ISS_buf_pin_1
File_IBIS-ISS full_buf_pin_1.iss full_buf_pin
Number_of_terminals = 6
1   Pin_I/O      pin_name A1 |   DQ1 DQ
2   Pin_Rail     pin_name P1 |   VDD POWER
3   Pin_Rail     pin_name G1 |   VSS GND
4   Buffer_I/O   pin_name A1 |   DQ1 DQ
5   Pullup_ref   pin_name A1 |   DQ1 DQ
6   Pulldown_ref pin_name A1 |   DQ1 DQ
[End Interconnect Model]
[End Interconnect Model Set]
```



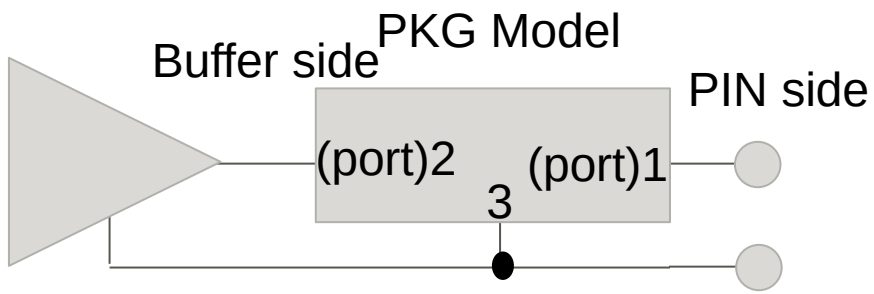
file_type : **FILE_IBIS-ISS (Spice)**
file path and file name : full_buf_pin_1.iss
.subckt name : full_buf_pin

IBIS 7.0 INTERCONNECT MODELING Outline

IBIS 7.0 INTERCONNECT MODELING by Touchstone (S-parameter)

.ibs file

```
[Component]     CPU
[Interconnect Model Group] Full_ISS_PDN_1
A1_TS    NA
[End Interconnect Model Group]
[Pin] signal_name model_name R_pin L_pin C_pin
A1    DQ1    DQ
P1    VDD    POWER
G1    VSS    GND
```



The [Interconnect Model Set] is present in the .ibs file.
(May be provided as an **.ims** file.)

```
[Interconnect Model Set] A1_TS
|-----
[Interconnect Model] A1_TS_buf_pin
File_TS   dq_ts_buf_pin.s2p
Number_of_terminals = 3
1 Pin_I/O        pin_name   A1
2 Buffer_I/O     pin_name   A1
3 Pulldown_ref   pin_name   A1
[End Interconnect Model]
[End Interconnect Model Set]
```

file_type : **FILE_TS (Touchstone file, S-parameter)**
file path and file name : dq_ts_buf_pin.s2p

Expectations for IBIS7.0 INTERCONNECT MODELING

- Get a more accurate simulation waveform
- Package Crosstalk modeling
- Package PDN modeling

Get a more accurate simulation waveform

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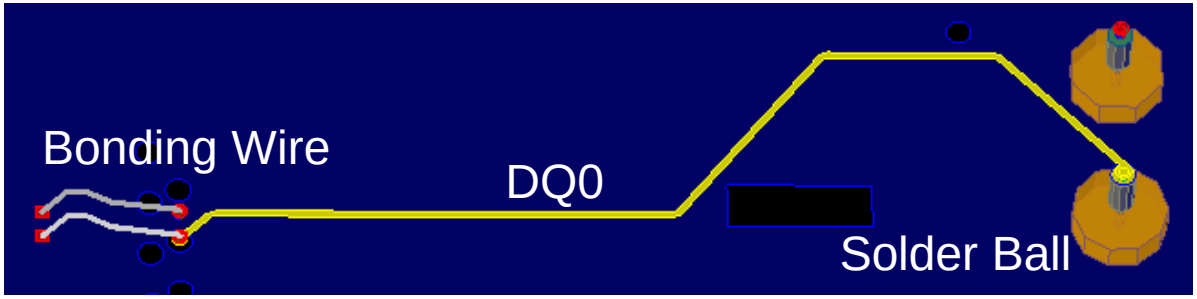
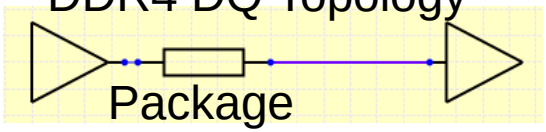
Single Line
Package Model



Conventional
IBIS model

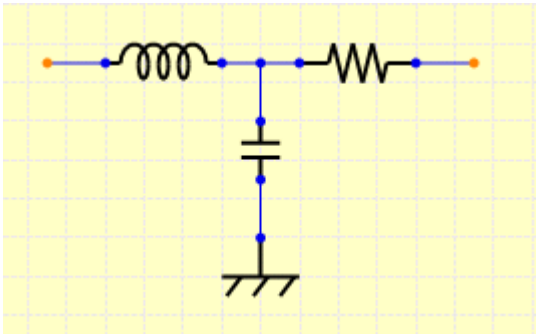
[Pin]	signal_name	model_name	R_pin	L_pin	C_pin
A1	DQ0	DQ	712.75m	8.95nH	3.42pF

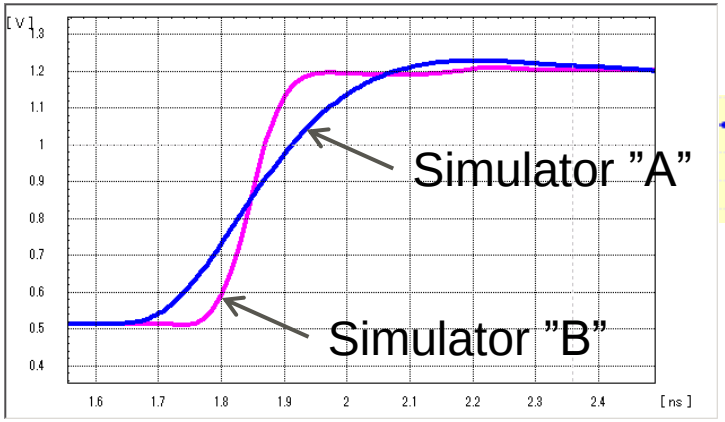
DDR4 DQ Topology



Simulator “A”

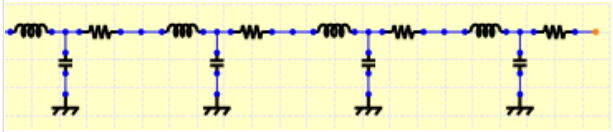
Lumped Circuit Model

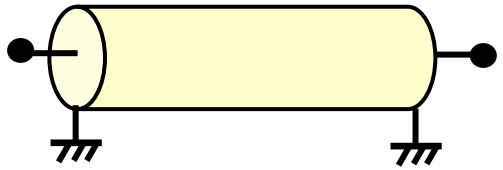




Simulator “B”

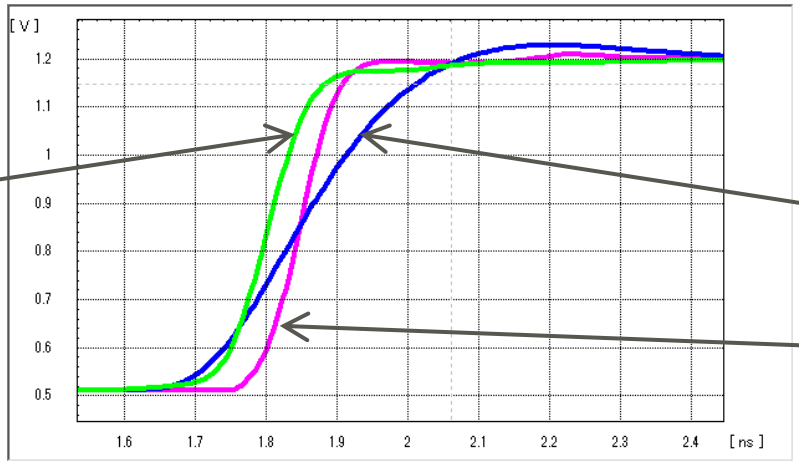
Distributed Circuit Model
(W-element RLGC Model)





Get a more accurate simulation waveform

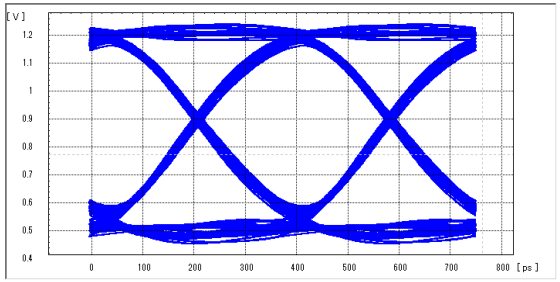
IBIS 7.0 Touchstone
or IBIS-ISS Model



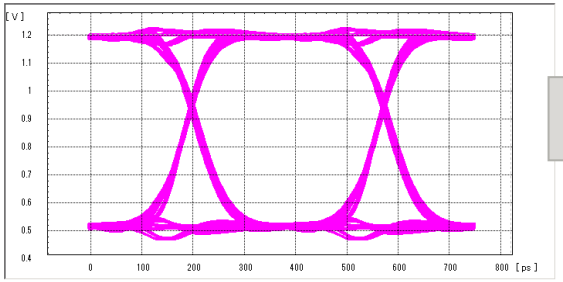
Lumped Circuit Model

Distributed Circuit Model

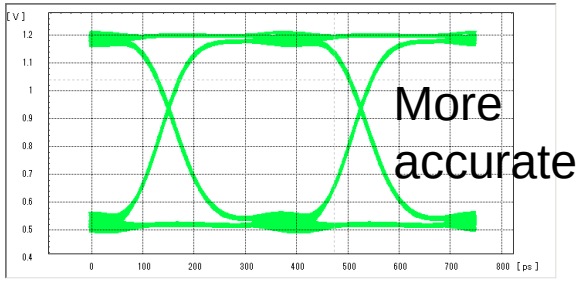
Simulator “A”
Lumped Circuit Model



Simulator “B”
Distributed Circuit Model



Simulator “A” and “B”
IBIS 7.0 Touchstone or IBIS-ISS



There is no difference due to simulator modeling, and more accurate waveforms can be obtained.

Package Crosstalk modeling

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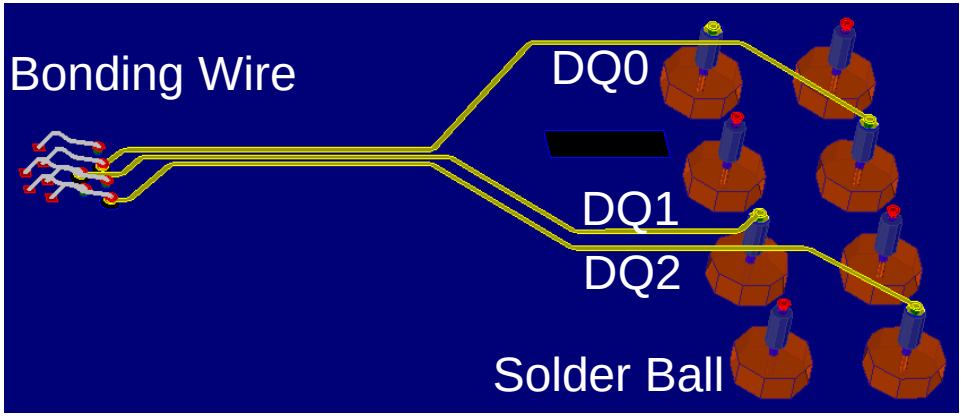
Multi Line Package Model



Conventional IBIS model

[Define Package Model] FBGA_PKG
[Manufacturer] FUJITSU
[OEM] FUJITSU
[Description]
[Number of Pins] 3
|
[Pin Numbers]
A1 | DQ0
B1 | DQ1
C1 | DQ2
|
[Model Data]
|

[Inductance Matrix] Sparse_Matrix
|
[Row] A1
A1 3.013e-09
B1 0.0877e-09
C1 0.0106e-09
|
[Row] B1
B1 2.663e-09
C1 0.0208e-09
|
[Row] C1
C1 2.923e-09

[Capacitance Matrix] Sparse_Matrix
|
[Row] A1
A1 7.904e-12
B1 -5.27e-12
C1 -0.764e-12
|
[Row] B1
B1 7.484e-12
C1 -5.27e-12
|
[Row] C1
C1 3.144e-12

[Resistance Matrix] Sparse_Matrix
|
[Row] A1
A1 2.98e-01
|
[Row] B1
B1 2.54e-01
|
[Row] C1
C1 2.92e-01
|
[End Model Data]
[End Package Model]

Package Crosstalk modeling

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Conventional IBIS model
[Define Package Model]

Simulator is not supported

Create SUBCKT by hand

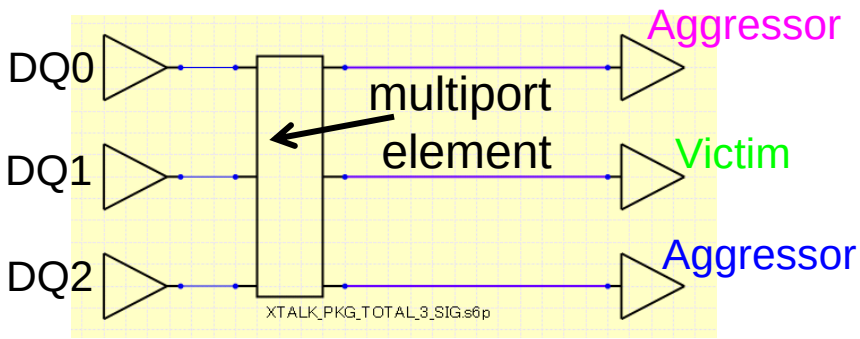
Modeling with W element of IBIS-ISS

```
.SUBCKT PKG_XTALK_MODEL 1 3 5 2 4 6
Wpkg N=3 1 3 5 0 2 4 6 0 RLGCMODEL=pkg_rlc l=1
.MODEL pkg_rlc W MODELTYPE=RLGC N=3
+ Lo=
+ 3.013e-9
+ 0.0877e-9   2.663e-9
+ 0.0106e-9   0.0208e-9  2.923e-9
+ Co=
+ 7.904e-12
+ -5.27e-12     7.484e-12
+ -0.764e-12   -5.27e-12   3.144e-12
+ Ro=
+ 0.298
+ 0        0.254
+ 0        0        0.292
.ENDS PKG_XTALK_MODEL
```

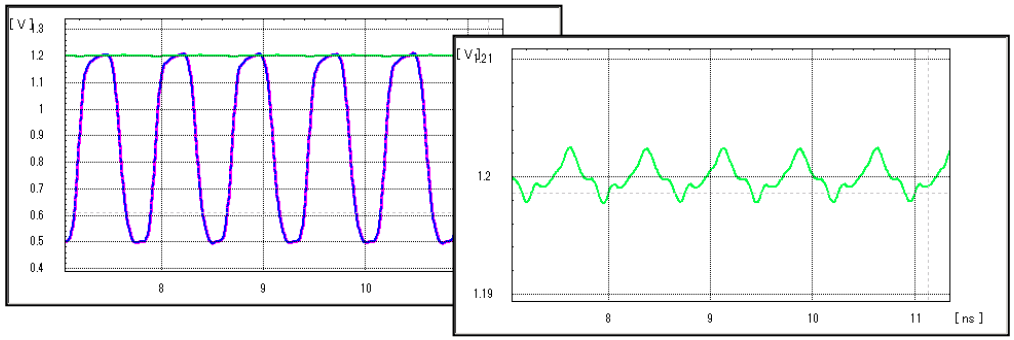
Very troublesome work.

IBIS 7.0 Touchstone or IBIS-ISS

Only incorporate Touchstone into the simulator's multiport element



Simulation results



Get faster and more accurate results.

Package PDN modeling

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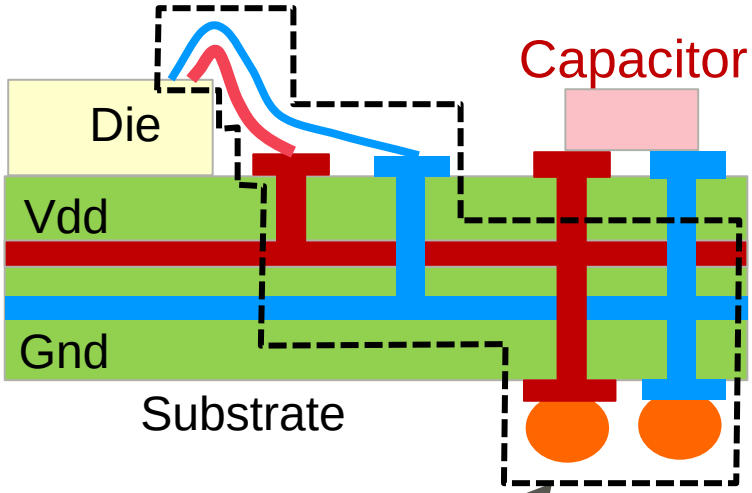
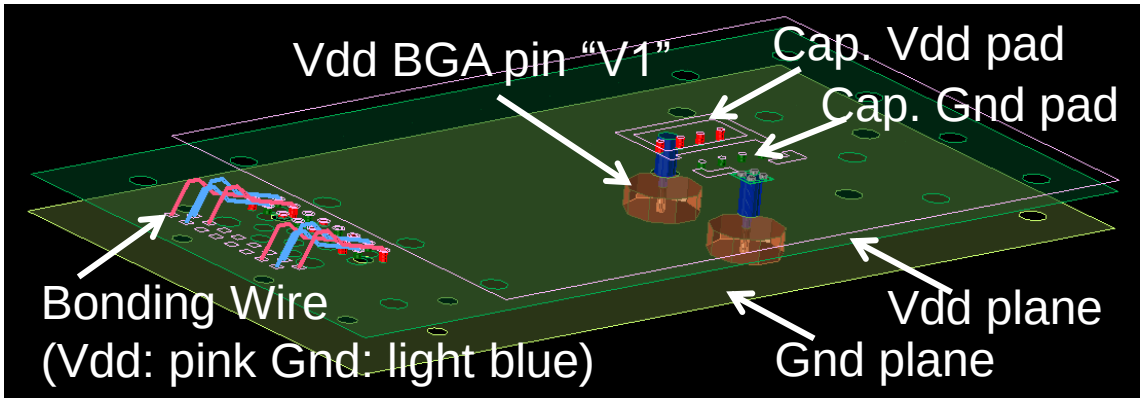
Package PDN structure





Conventional IBIS modeling part

```
[Pin]   signal_name   model_name   R_pin   L_pin      C_pin
|
V1   VDDQ   POWER                  9m      0.326nH    70pF
```

Cannot put Package Capacitor model

Package PDN modeling

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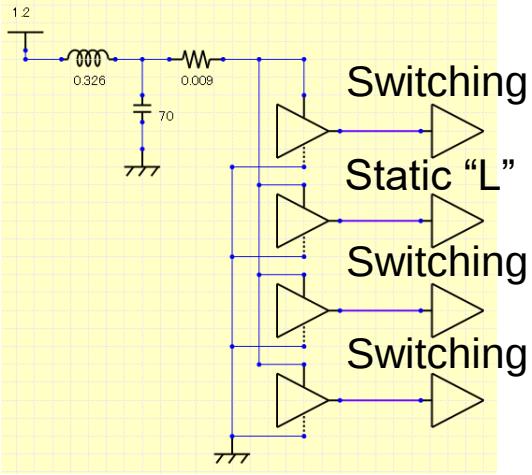
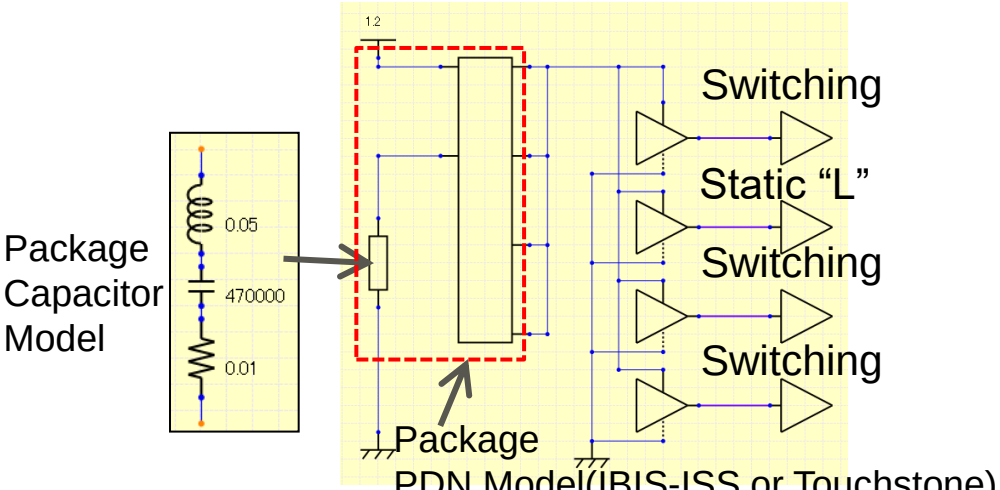
Conventional IBIS SSO simulation topology without Package Decoupling Capacitor

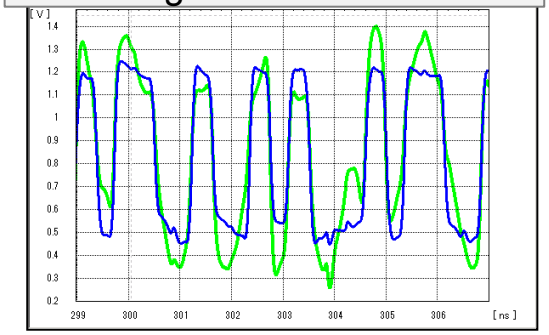


IBIS 7.0 SSO simulation topology with Package Decoupling Capacitor

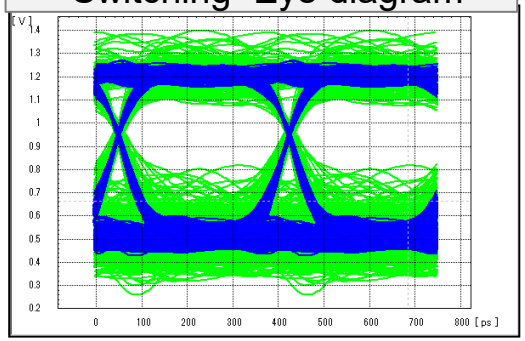


Light Green: Conventional IBIS, Blue: IBIS 7.0

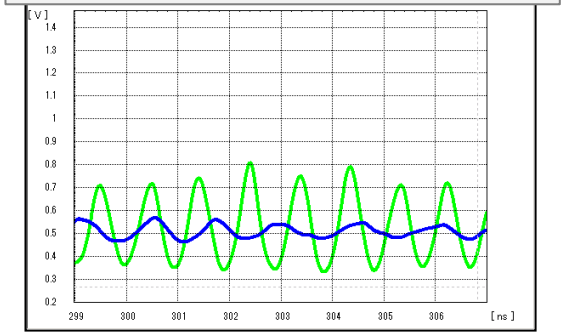
"Switching" Transient waveform



"Switching" Eye diagram



"Static L" Transient waveform



Enables accurate simulation with capacitor effects.

Post-layout simulator issues when using the IBIS7.0 INTERCONNECT MODEL

- Post-layout simulator issues
- Support for Local GND reference waveform output
- Support for Touchstone Version 2.0
- Support for S-element with N reference nodes

Post-layout simulator issues

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- The post-layout simulator verifies a large number of nets in a short time. Therefore, the power and GND nets are treated as an ideal, and the transmission waveform viewed from the ideal GND (node 0 in Spice) is output.

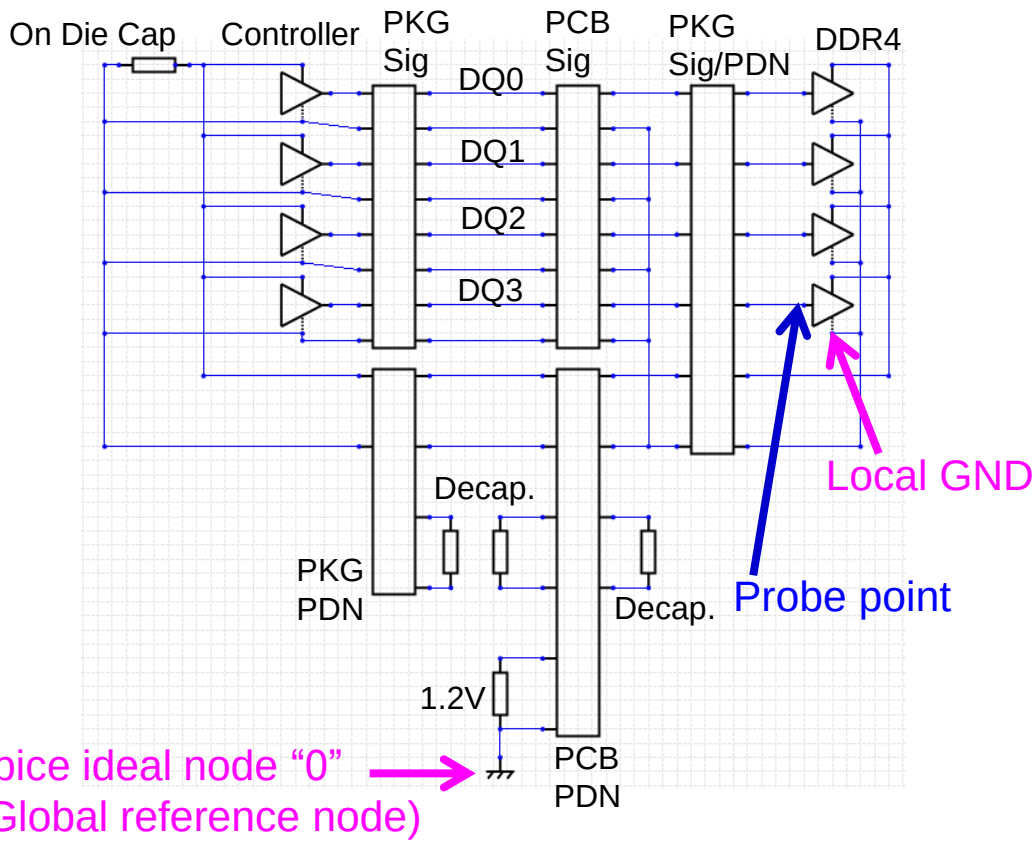
- However, since the IBIS 7.0 INTERCONNECT MODEL includes a high-accuracy Package PDN model, SI simulation considering PI (power-aware simulation) is possible.

- Therefore, the functions required for the simulator in the post-layout simulation using the IBIS 7.0 INTERCONNECT MODEL are described below.

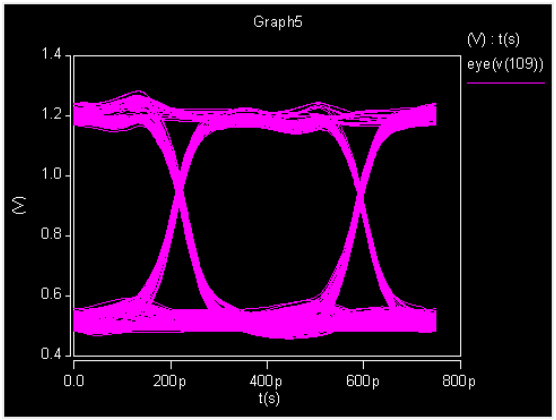
Support for Local GND reference waveform output

- Enable to output waveform not only with Node 0 reference but also with local GND reference to observe true receiver waveform.

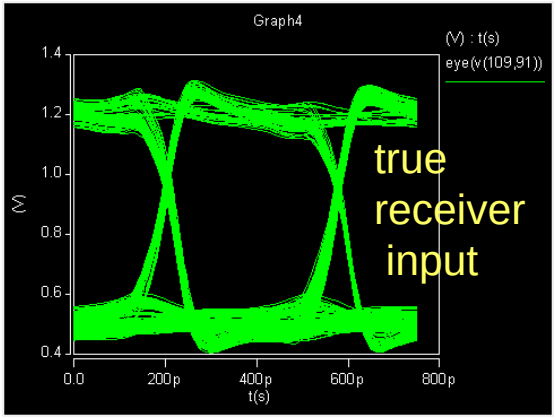
DDR4-2666 SSO Simulation Topology



Node “0” reference waveform



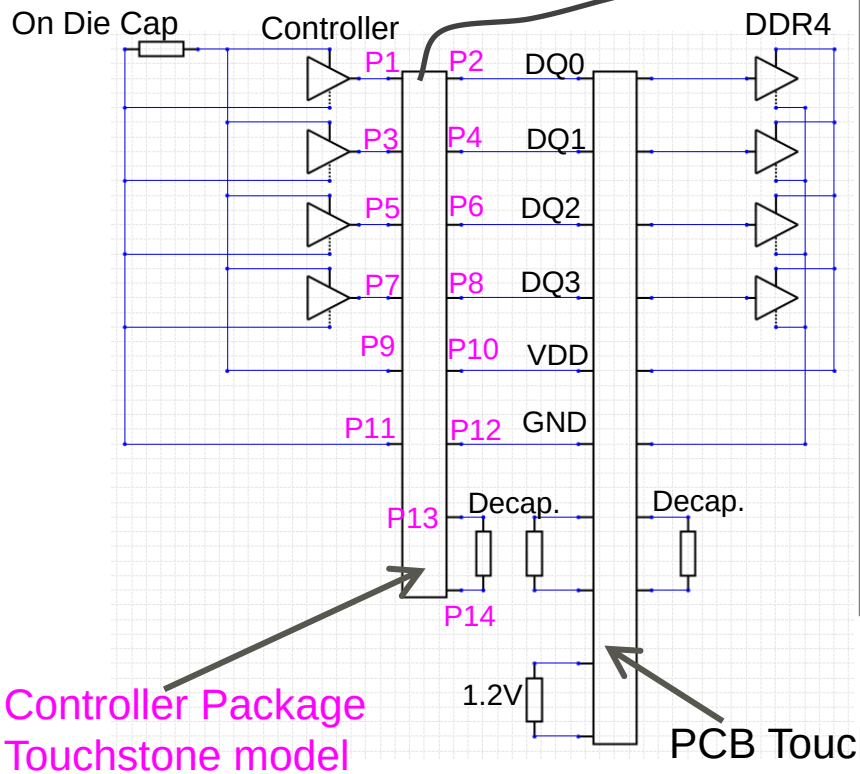
Local GND reference waveform



Support for Touchstone Version 2.0

- S-parameter Port Impedance: Signal→50Ω　PDN→0.01Ω
- IBIS 7.0 Package model may include Signal and PDN models together.
- S-parameter with Signal and PDN→Modeling by Touchstone Version 2.0
- Therefore, Simulator must be able to handle Touchstone Version 2.0.

DDR4-2666 SSO Simulation Topology



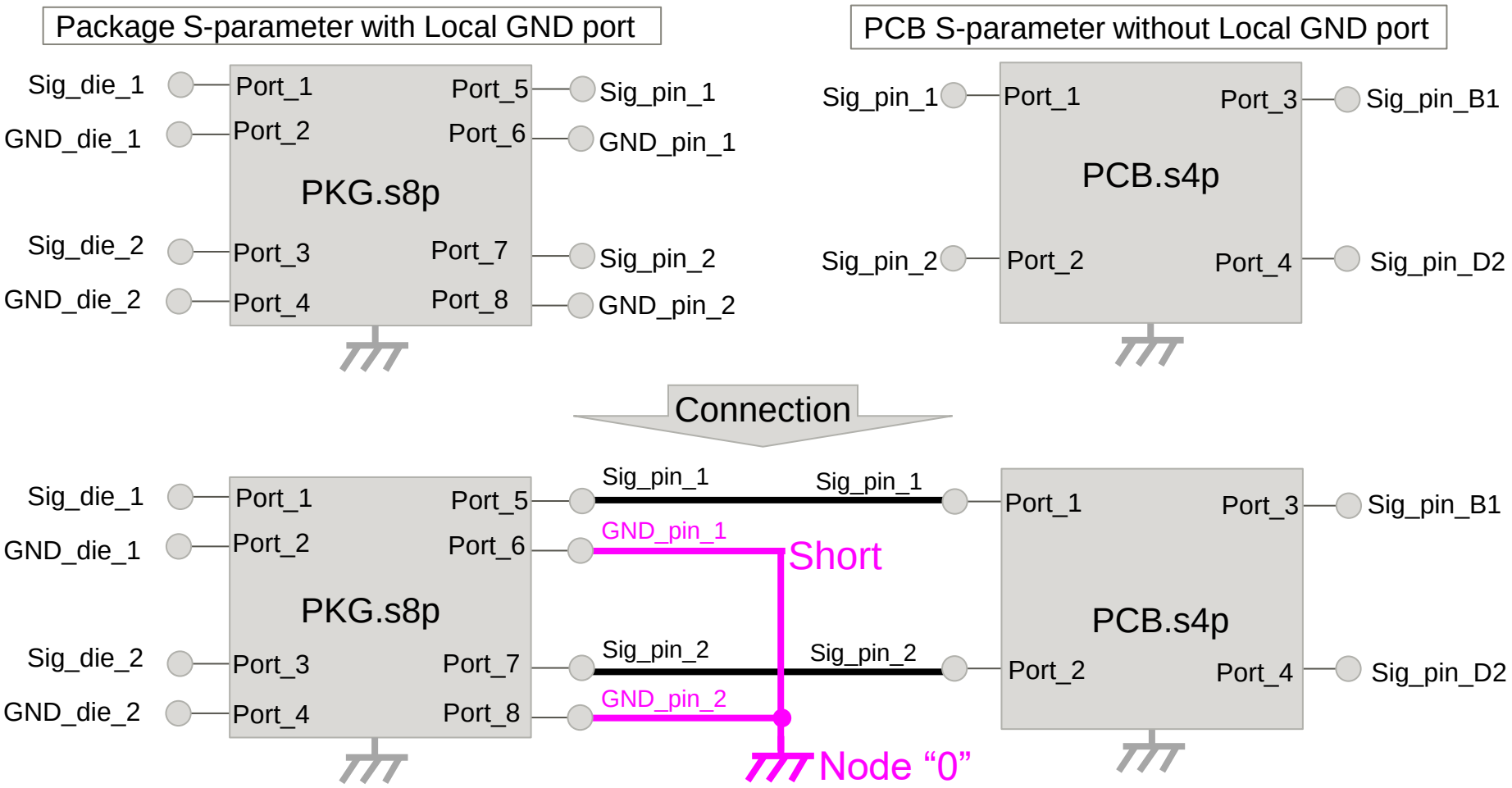
Touchstone Version 2.0 File Format

! 14-port S-parameter data
[Version] 2.0
GHz S MA R 50
[Number of Ports] 14
[Number of Frequencies] 100
[Reference] 50 50 50 50 50 50 50 50 0.01 0.01 0.01 0.01 0.01 0.01
[Matrix Format] Full
[Network Data]

0	0.00248230077	0	0.997517699	0	6.26736291e-16	0	1.7368305e-16	180
	8.63261663e-17	0	9.58509958e-17	180	3.17940593e-16	0	1.95386528e-16	0
	3.97693164e-14	0	1.0544507e-12	0	3.97635386e-14	0	1.05549902e-12	0
	9.54043922e-17	180	9.40660628e-17	0	2.00075118e-16	0	3.16842798e-16	0
	3.98112805e-14	0	1.05636301e-12	0	3.9899421e-14	0	1.05747895e-12	0
	3.98980676e-14	0	1.05749522e-12	0				
	6.26736291e-16	0	1.69291648e-16	180	0.00291113079	0	0.997088869	0
	1.72969382e-14	0	1.70927782e-14	0	1.10345768e-15	180	1.21350716e-15	180
	3.61044345e-14	0	1.23159098e-12	0	3.60900023e-14	0	1.2328187e-12	0
	3.60921621e-14	0	1.23283725e-12	0				
	1.7368305e-16	180	5.78685688e-16	0	0.997088869	0	0.00291113079	0
	1.70720495e-14	0	1.7234413e-14	0	1.20973279e-15	180	1.11337482e-15	180

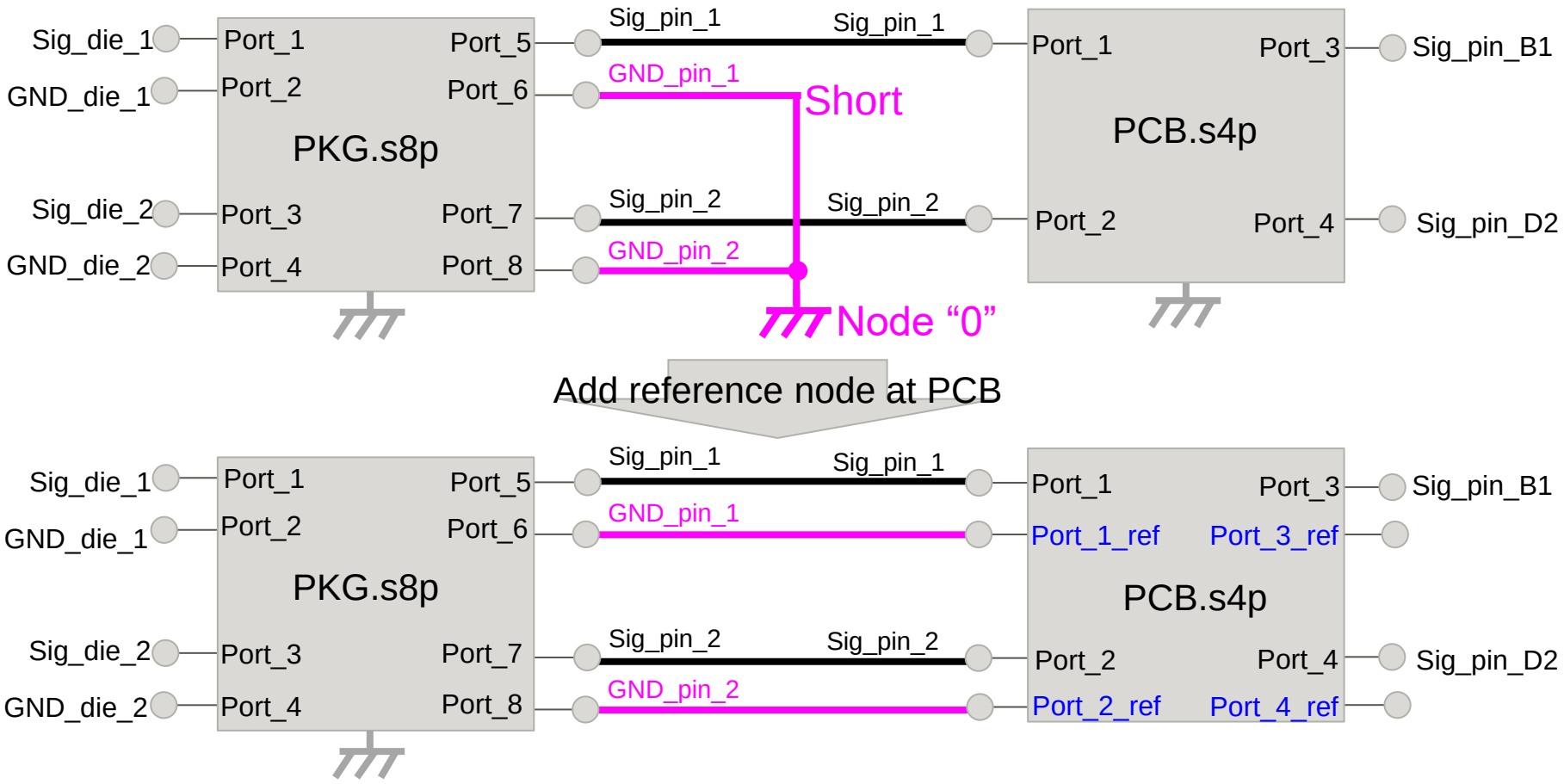
Support for S-element with N reference nodes

- Connecting PKG's Local GND to the Ideal GND when connecting PKG S-para with Local GND port to PCB S-para without Local GND port is inaccurate for Power-aware Simulation.



Support for S-element with N reference nodes

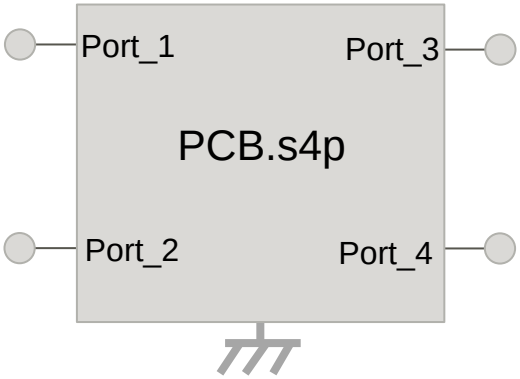
- Therefore, when assigning the S-para of the PCB to the S-element, add a reference node corresponding to each port.
  Then connect PKG's local GND to that node.



Support for S-element with N reference nodes

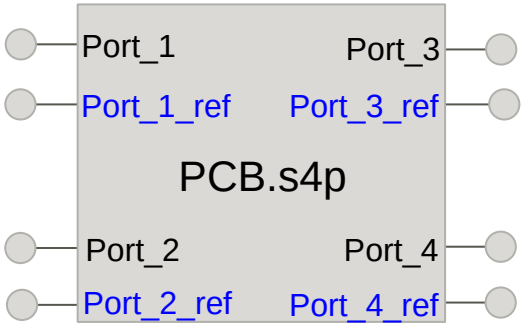
- S-element description before and after reference node addition

Before addition




```
S1
+ Port_1
+ Port_2
+ Port_3
+ Port_4
+ 0
+ mname=PCB_SPARA
.model PCB_SPARA S
+ N=4
+ tstonefile= PCB.s4p
```

After addition

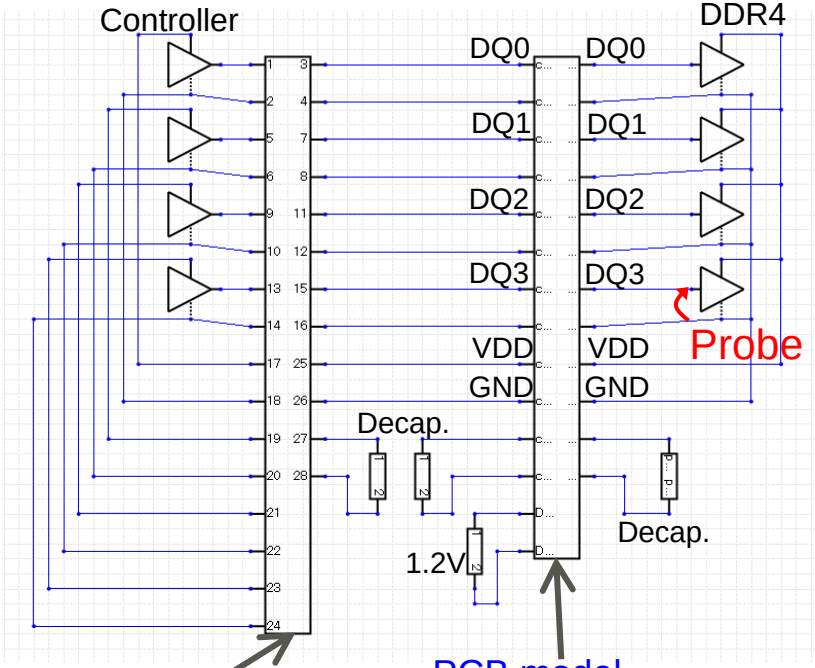



```
S1
+ Port_1 Port_1_ref
+ Port_2 Port_2_ref
+ Port_3 Port_3_ref
+ Port_4 Port_4_ref
+ mname=PCB_SPARA
.model PCB_SPARA S
+ N=4
+ tstonefile= PCB.s4p
```

Support for S-element with N reference nodes

- Waveform comparison between S-parameter PCB model with local GND port and S-element PCB model with N reference node.
- Both eye diagrams are almost the same.

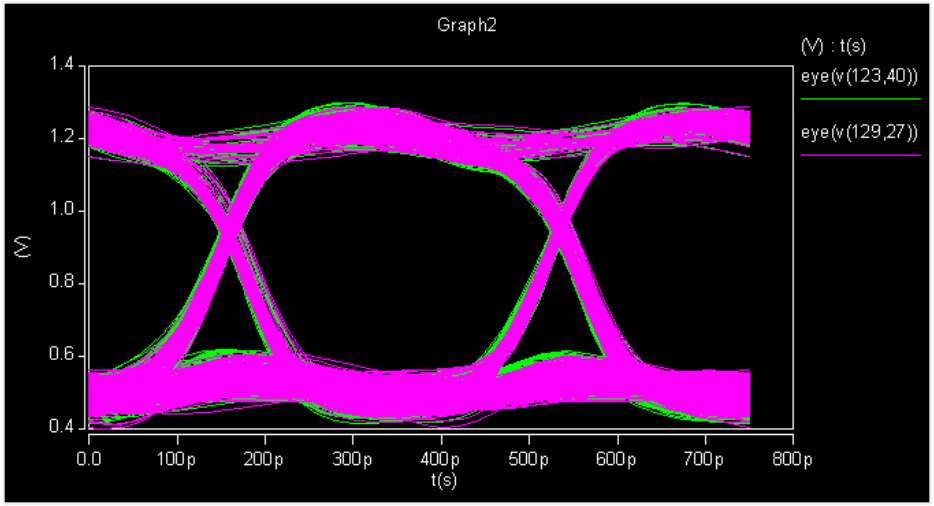
DDR4-2666 SSO Simulation Topology



Controller Package model
Touchstone model
with LOCAL GND port

PCB model
(a) Touchstone model
with LOCAL GND port
or
(b) S-element with N reference node

Light Green: PCB model is (a)Touchstone with LOCAL GND port
Pink: PCB model is (b)S-element with N reference node



Summary

- Highly accurate simulation results are expected by the package model based on the IBIS 7.0 INTERCONNECT MODEL.
- The IBIS 7.0 package model can be applied to power-aware simulation. Therefore, the post-layout simulator must also support power-aware simulation.

References

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  IBIS Open Forum April 24, 2009
  https://ibis.org/touchstone_ver2.0/touchstone_ver2_0.pdf

- “IBIS Interconnect SPICE Subcircuit (IBIS-ISS) Specification Version 1.0”,
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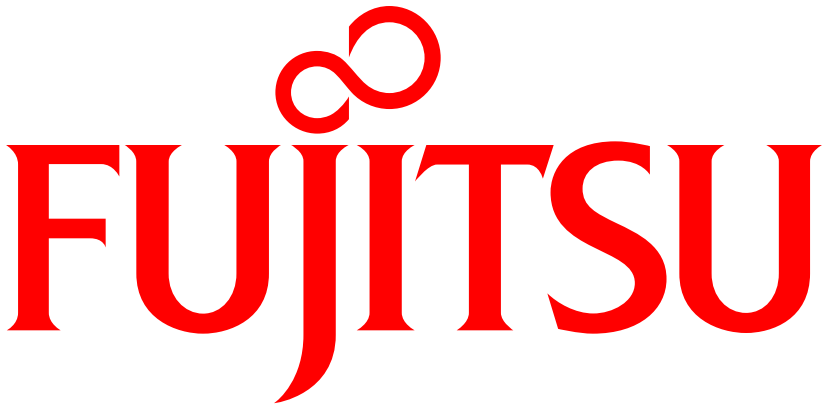
  https://ibis.org/ibis-iss_ver1.0/ibis-iss_ver1_0.pdf



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