

Asian IBIS Summit
Tokyo, JAPAN
November 8th, 2019

The On Die Decap modeling proposal (BIRD198)

JEITA

Semiconductor & System design technical committee

Semiconductor design technology subcommittee

Presenter : Megumi Ono (Socionext Inc).

Co-Author: Atsushi Tomishima (Toshiba Electronic Devices & Storage Corporation)



Agenda

- Background
- Proposal for On die De-cap model
- Feedback and updating
- Conclusion

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- **Background**
- Proposal for On die De-cap model
- Feedback and updating
- Conclusion

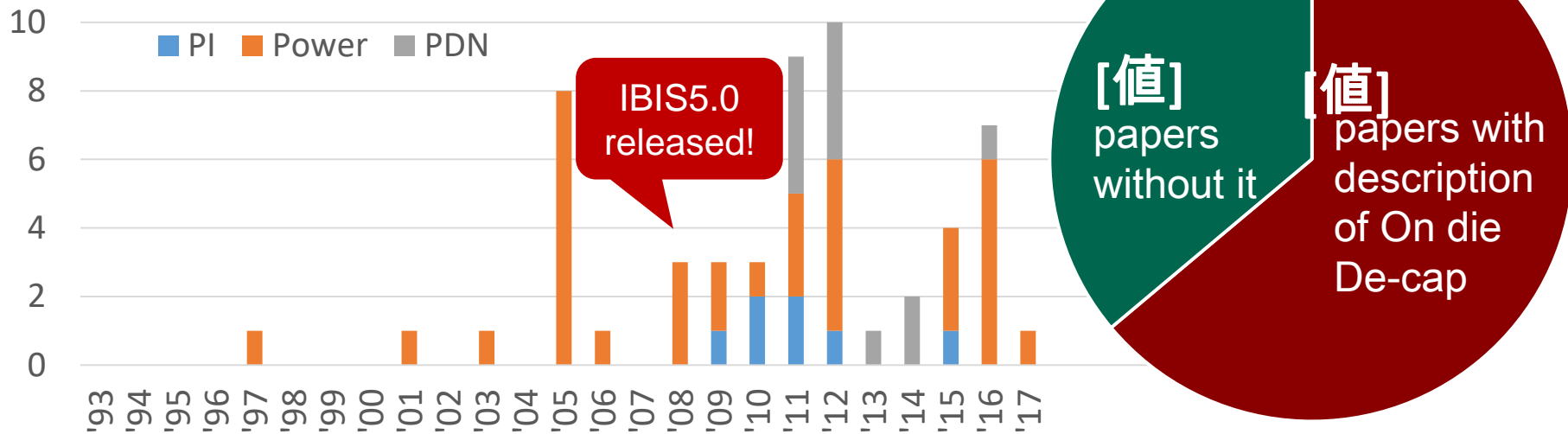
Chip PDN characteristic

■ Chip PDN characteristic

- **On die Resistance** affects IR-Drop and Q factor
- **On die De-cap** affects High frequency power-supply noise

Many papers reported in IBIS Summit describe importance of **On die De-cap**, because it is one of the few solution that reduce high frequency power-supply noise

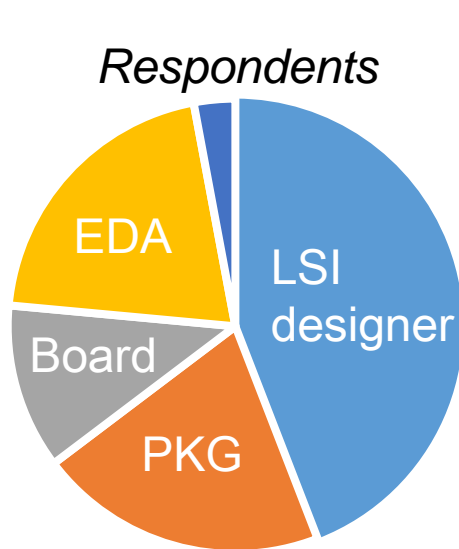
IBIS Summit papers, the title of which have the below words



A Survey of On die De-cap model

- However, board and system designers can hardly obtain On die De-cap model

A Survey by JEITA LPB-SC MDL-WG @LPB developers workshop 2017.9.2

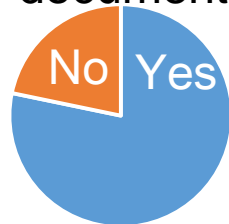


Q1. to All

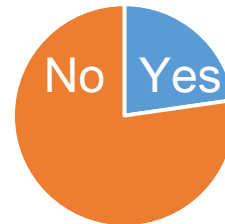
“Can you obtain information about Chip PDN?”

Answer

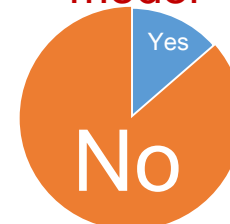
Guideline documents



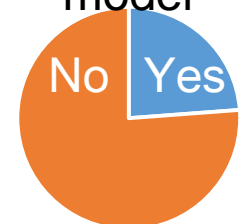
Target Z



On die De-cap model



PKG PDN model



Q2. to LSI designer

“What are you concerned about when you offer PDN model”

Answer

“Which model format is suitable for our customer?”

History of our proposal

Nov. 17, 2017 Asian IBIS Summit Tokyo, JAPAN

Proposal(Draft1)

Asian IBIS Summit
Tokyo, JAPAN
November 17, 2017

On die De-cap Modelin

Murata Kazuki (RICOH COM
JEITA

Semiconductor & System Design T
LPB Interoperable Design Su
Modeling Working G



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<https://ibis.org/summits/nov17c/murata.pdf>

Sep. 8, 2018 LPB workshop

Proposal(Draft2)

オンチップデキャップ考慮の
必要性と測定方法

坂田和之 (ルネサスエレクトロニクス)、村田和
JEITA半導体&システム設計技術委員

LPB相互設計サブコミッティ
モデリングワーキンググループ



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Feb. 1, 2019 DesignCon 2019 IBIS Summit

Proposal(Final)

DesignCon 2019 IBIS Summit
Santa Clara, CA
February 1, 2019

On Die De-cap Modeling Proposal

Kazuki Murata (Ricoh Co.,Ltd.), Megumi Ono (Socionext Inc.)
JEITA
Semiconductor & System Design Technical Committee
LPB Interoperable Design Sub-Committee
Modeling Working Group



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<https://ibis.org/summits/feb19/murata.pdf>



History of our proposal

March 11, 2019 Submitted <https://ibis.org/birds/>

Buffer Issue Resolution Documents (BIRD)

To submit a BIRD to the IBIS Open Forum, please use the [BIRD Template, Rev. 1.3](#).

ID#	Issue Title	Requester	Date Submitted	Date Accepted	Supporting Version
200	C_comp Model Using IBIS-ISS or Touchstone	Randy Wolff, Micron Technology, Inc. Walter Katz, Signal Integrity Software, Inc.	July 9, 2019	September 27, 2019	
199	Fix Rx Receiver Sensitivity Inconsistencies	Arpad Muranyi, Mentor a Siemens Business	March 19, 2019	June 7, 2019	
198	Keyword additions for On Die PDN (Power Distribution Network) Modeling	Kazuki Murata; Ricoh Co., Ltd.; Miyoko Goto; Ricoh Co., Ltd.; Kazuyuki Sakata; Renesas Electronics Corporation; Kazunori Yamada; Renesas Electronics Corporation; Kouji Ichikawa; Denso Corporation; Atsushi Tomishima; Toshiba Electronic Devices & Storage Corporation; Takashi Hasegawa; Sony LSI Design Inc.; Koichi Seko, Panasonic Industrial Devices Systems and Technology Co., Ltd.; Toshiki Kanamoto; Hirotsuki University Megumi Ono; Socionext Inc.	March 11, 2019		

IBIS Specification Change Template, Rev. 1.3^v

BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)-

BIRD NUMBER: 198-
ISSUE TITLE: Keyword additions for On Die PDN (Power Distribution Network) Modeling-
REQUESTOR: Kazuki Murata, Ricoh Co., Ltd.^v
Miyoko Goto, Ricoh Co., Ltd.^v
Kazuyuki Sakata, Renesas Electronics Corporation.^v
Kazunori Yamada, Renesas Electronics Corporation.^v
Kouji Ichikawa, Denso Corporation.^v
Atsushi Tomishima, Toshiba Electronic Devices & Storage Corporation.^v
Takashi Hasegawa, Sony LSI Design Inc.^v
Koichi Seko, Panasonic Industrial Devices Systems and Technology Co., Ltd.^v
Toshiki Kanamoto, Hirotsuki University^v
Megumi Ono, Socionext Inc.^v

DATE SUBMITTED: March 11, 2019-
DATE REVISED: -
DATE ACCEPTED: -

DEFINITION OF THE ISSUE:-
To resolve the power-supply noise issue, especially high frequency range, on die decap should be taken account into the simulation. With current IBIS versions, "On Die PDN" can be defined by using the keyword [Series Pin Mapping] and "Model_type Series".
However, this method seems not to be widely recognized, because the keyword [Series Pin Mapping] and "Model_type Series" don't make imagine to describe the on die PDNmodel. To ease usage of "On Die PDN" in the IBIS model, this BIRD proposes to add the new keywords [PDN Model Mapping], "Model_type PDN", [C pdn], [R pdn], [R leak], [C pdn corner], [R pdn corner] and [R leak corner] for PDN model only. -

SOLUTION REQUIREMENTS:-
The IBIS specification must meet these requirements:-
• Table 1: Solution Requirements.

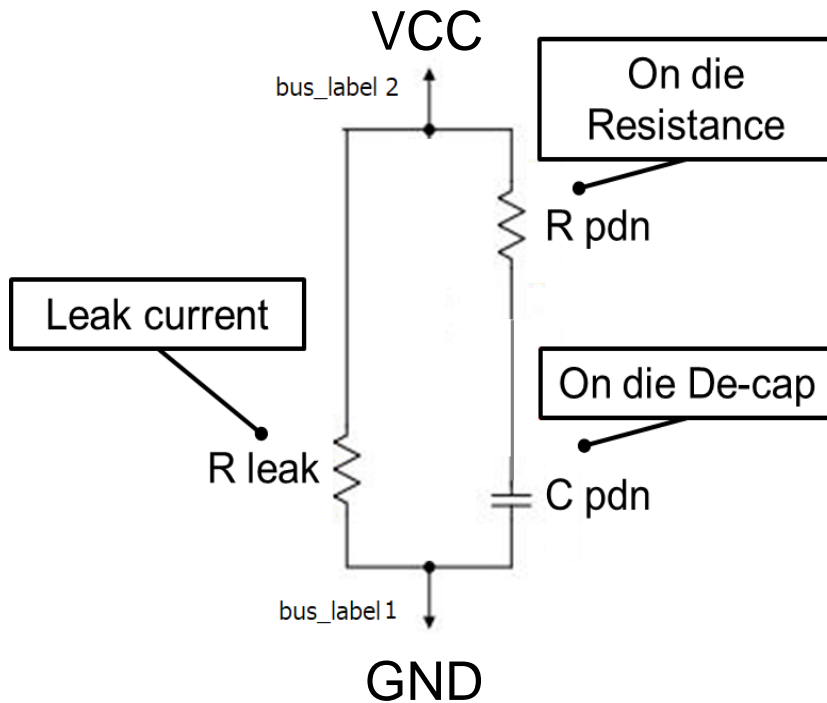
Requirement ^v	Notes ^v
1. A new keyword is defined under [Component]- [PDN Model Mapping]-	-
2. A new sub parameter is defined under [Model]: "Model_type PDN" -	-

Agenda

- Background
- **Proposal for On die De-cap model**
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Proposal

Model



New Keyword

```
[Model] OnChipDecapA
Model_type On_Die_PDN

[C pdn]          3n    2.9n    3.1n
[R pdn]          0.1    0.1    0.1
[R leak]         200    200    200
```

```
[PDN Model Mapping]

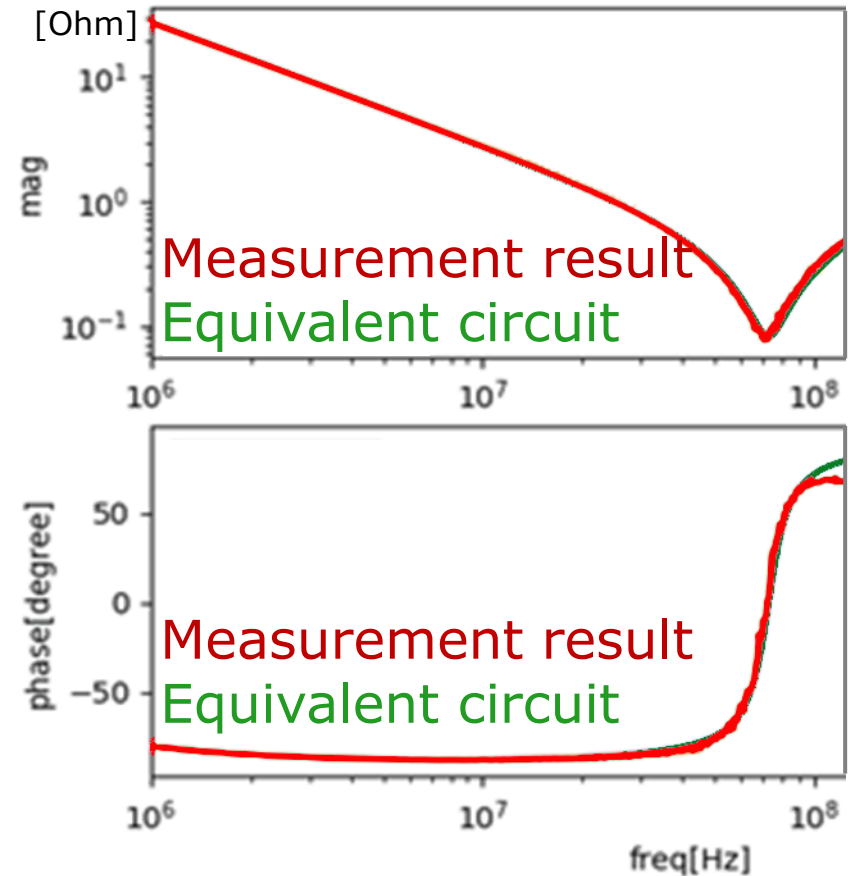
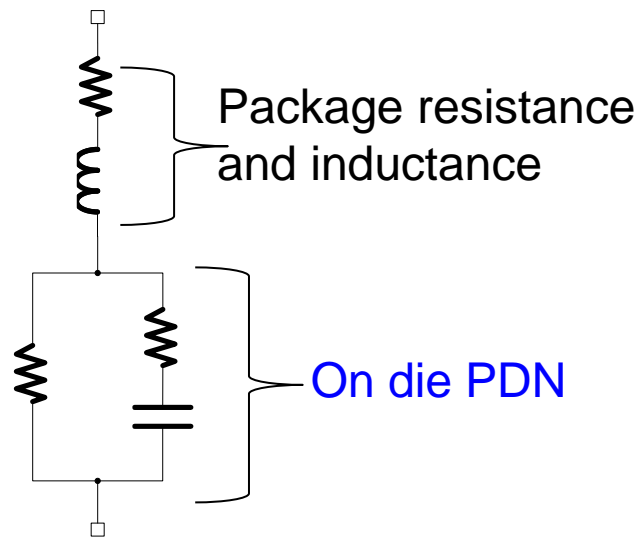
C3  A1  OnChipDecapA
D4  D1  OnChipDecapB
D3  D1  OnChipDecapC
A4  A5  model_selector_for_PSO
```

A little modification to existing IBIS Keyword “Series Model”

Correlation between measurement and model

- Our proposed model is correlated with the measurement results.

Equivalent circuit

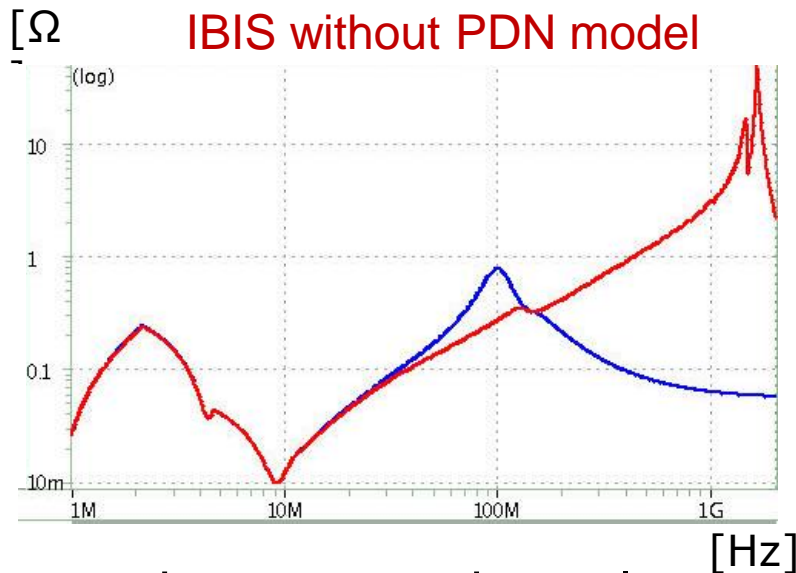


Simulation Result

- Simulation result using the IBIS model that we proposed

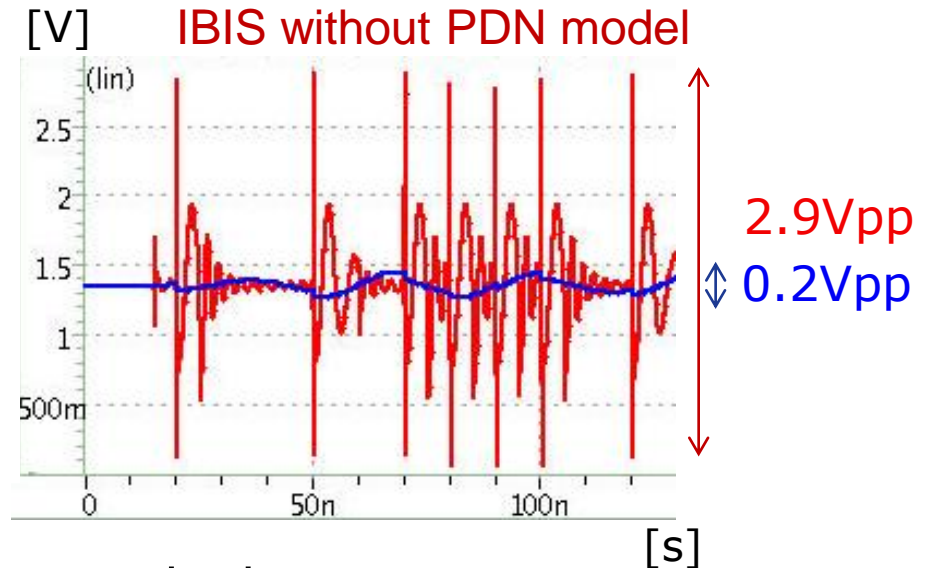
AC analysis result
= PDN input impedance

IBIS with PDN model
IBIS without PDN model



Transient analysis result
= IO switching VDD noise @DIE

IBIS with PDN model
IBIS without PDN model



- The expected result was obtained when using a certain simulator

Agenda

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List of syntax candidates

	Syntax A	Syntax B	Syntax C
	Updated BIRD198	New Proposal from IBIS Open Forum (Ex.1)	New Proposal from IBIS Open Forum (Ex.2)
Connection	Bus_label	Bus_label	Bus_label
Parent	[Model]	[Component]	[Component]
Model selecting Method	✓ [Model Selector]	✓ Alternative method	✓ Alternative method
Corner definition	The order of the values does not have to be typ / min / max	Define for C/R parameter names aligned by corner (C_pdn_corner, etc.) or not related to a corner (C_pdn, etc.).	Define typ / min / max values separately each in [PDN Model]
Base structure	Series Model	[Interconnect Model]	[Interconnect Model]
EDA Vendor	Difficult implementation	easy implementation	easy implementation

List of syntax candidates

	Syntax A	Syntax B	Syntax C
	Updated BIRD198	New Proposal from IBIS Open Forum (Ex.1)	New Proposal from IBIS Open Forum (Ex.2)
Connection	Bus_label	Bus_label	Bus_label
Parent	[Model]	[Component]	[Component]
Model selecting Method	✓ [Model Selector]	✓ Alternative method	✓ Alternative method
Corner definition	The order of the values does not have to be typ / min / max	Define for C/R parameter names aligned by corner (C_pdn_corner, etc.) or not related to a corner (C_pdn, etc.).	Define typ / min / max values separately each in [PDN Model]
Base structure	Series Model	[Interconnect Model]	[Interconnect Model]
EDA Vendor	Difficult implementation	easy implementation	easy implementation

1st Feedback from IBIS Open Forum

To Authors of IBIS BIRD198:¶

BIRD198 has been discussed in the IBIS ATM (Advanced Technology Modeling Task Group) meetings. In this letter we would first like to discuss our understanding of the intent of BIRD198, and how EDA tools would implement it. We would be happy to then continue the conversation about how to best model PDN elements in IBIS.¶

We believe that the intent of BIRD198 is to describe an on-die decoupling model between pairs of power/ground rail signals.¶

- The [PDN Model Mapping] defines a model between two pins in the [Pin] section, but our understanding is that it defines a model connected either between the die pads associated with those pins, or power/ground rail signal networks associated with those pins.¶
- Our understanding is that this model would be limited to on-die decoupling capacitance connected between rail signals. Any decoupling capacitance between rail signals on the package (for example, package decoupling capacitors) would not be included in this model. That capacitance would have to be included in a package model.¶
- We also understand that BIRD198 implies that the on-die pads and on-die buffer connections to each rail supply voltage are short-circuited, so that there is a direct connection. That is, no interconnect circuit elements are connected between the supply rail die pads and the buffer supply rails.¶

Please let us know if our understanding of BIRD198 is correct. If this is correct, we believe it might be useful for the BIRD to state additional clarifications or restrictions. For background, IBIS currently describes the internal connections of power and ground rails by these means:¶

1. **[Pin Mapping]** – This keyword supports descriptions of power and ground buses connecting die pads, associating these buses with groups of POWER and GND pins, and also with the supply terminals of buffers connected to signal pins. Given a pin name, it is possible to determine the other pins that share the same POWER bus or GND bus. The February 2019 presentation by Ono-san mentions [Pin Mapping].¶
2. **[Interconnect Model]** – The connections between pins and the internal power and ground structures are exactly described in detail using IBIS-ISS or Touchstone. In one form, an [Interconnect Model] can connect pin terminals to buffer supply terminals without an explicit connection to a supply die pad. In this case there is no knowledge of supply rails. Also, an [Interconnect Model] may connect any number of pin terminals to any number of named [Die Supply Pads] terminals, although the details of which pins are strongly connected to which die pads are described only by the IBIS-ISS or Touchstone elements. In this case the [Die Supply Pad] terminals might constitute supply rails, but it may not be known to which of those a particular pin is associated. [Interconnect Model] does however have syntax allowing rail connections to be well understood.¶
3. **No [Pin Mapping] and no [Interconnect Model]** – It must be assumed that any rail connections between POWER pins, if there is more than one POWER pin, are unknown. The same applies for GND pins. The connections between buffer supply terminals and

power and ground rails are also unknown, therefore buffers are connected to ideal supply voltages.¶

In each case above an EDA tool must form a circuit to represent the connections. It will be necessary for the tool to determine the nodes of the circuit to which the PDN capacitor models must be attached. IBIS must be clear about the connection expectations.¶

To assist EDA tools, BIRD198 should be clear about how the PDN capacitor models would be connected to simulation circuits in combination with each of the three cases above. Since [PDN Model Mapping] defines its connections by pin names, please consider the ideas below, numbered as above:¶

1. In the case where [Pin Mapping] is used, the rail nodes for attaching PDN capacitor models are well understood.¶
2. The rules for using [PDN Model Mapping] for pins connected to [Interconnect Model] might need to be carefully defined. Depending on the [Interconnect Model] syntax used, power and ground rail terminals might not be defined at all, or it might be difficult to associate them exactly with specific pins. Also, it would be important to avoid having duplicate capacitance in [PDN Model Mapping] and [Interconnect Model].¶
3. With no [Pin Mapping] and no [Interconnect Model], no supply rail buses are defined. In this case a [PDN Model Mapping] entry would connect the PDN capacitor model to the internal package nodes of the specified pins only. Those capacitors would serve to decouple the power/ground signals on the board, but no buffers or other die pads inside the chip would be connected to them.¶

Please let us know your thoughts on these ideas.¶

We wish to continue this discussion by e-mail for some time. Later, the ATM task group would also be willing to set up a special meeting at 5 PM EST on a Tuesday (or some other time convenient to most of us) to have a phone discussion on these topics. Please let us know if that would be convenient, and please suggest a date that would work well for you, if such a meeting is desired.¶

Thank you for your contribution to IBIS.¶

Mike LaBonte, Chair, IBIS Open Forum¶

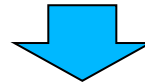
Arpad Muranyi, Chair IBIS Advanced Technology Modeling Task Group¶

Update of BIRD198

1. Added "**On die**" to clearly identify "on die pdn"

[PDN Model Mapping]

C3	A1	OnChipDecapA
D4	D1	OnChipDecapB
D3	D1	OnChipDecapC
A4	A5	model_selector_for_PSO



[On Die PDN Model Mapping]

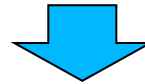
C3	A1	OnChipDecapA
D4	D1	OnChipDecapB
D3	D1	OnChipDecapC
A4	A5	model_selector_for_PSO

Update of BIRD198

2. Pin name → **Bus label** (required description from IBIS7.0)

[PDN Model Mapping]

C3	A1	OnChipDecapA
D4	D1	OnChipDecapB
D3	D1	OnChipDecapC
A4	A5	model_selector_for_PSO



[On Die PDN Model Mapping]

VDDA	VSS	OnChipDecapA
VDDB	VSSB	OnChipDecapB
VDDA	VSSB	OnChipDecapC
VDP	VSSC	model_selector_for_PSO

Update of BIRD198

3. [Model Selector] support

```
[Component]    AAA
  [Pin Mapping]
    pin_name1   NC           bus_label1
    pin_name2   bus_label2  NC
  [On Die PDN Model Mapping]
    bus_label1  bus_label2  DDRRAIL
  [Model Selector]  DDRRAIL
    DDR3_mode
    DDR4_mode
  [Model]      DDR3_mode
    Model_Type  On_Die_PDN
    [C pdn]    3.0n    3.6n    2.1n
    [R pdn]    0.02    0.03    0.01
    [R leak]   15k     15k     15k
  [Model]      DDR4_mode
    Model_Type  On_Die_PDN
    [C pdn]    2.0n    2.5n    0.9n
    [R pdn]    0.02    0.03    0.01
    [R leak]   15k     15k     15k
```

Almost the same as
"Series model"

The order of the
values does not have to
be typ / min / max

Update of BIRD198

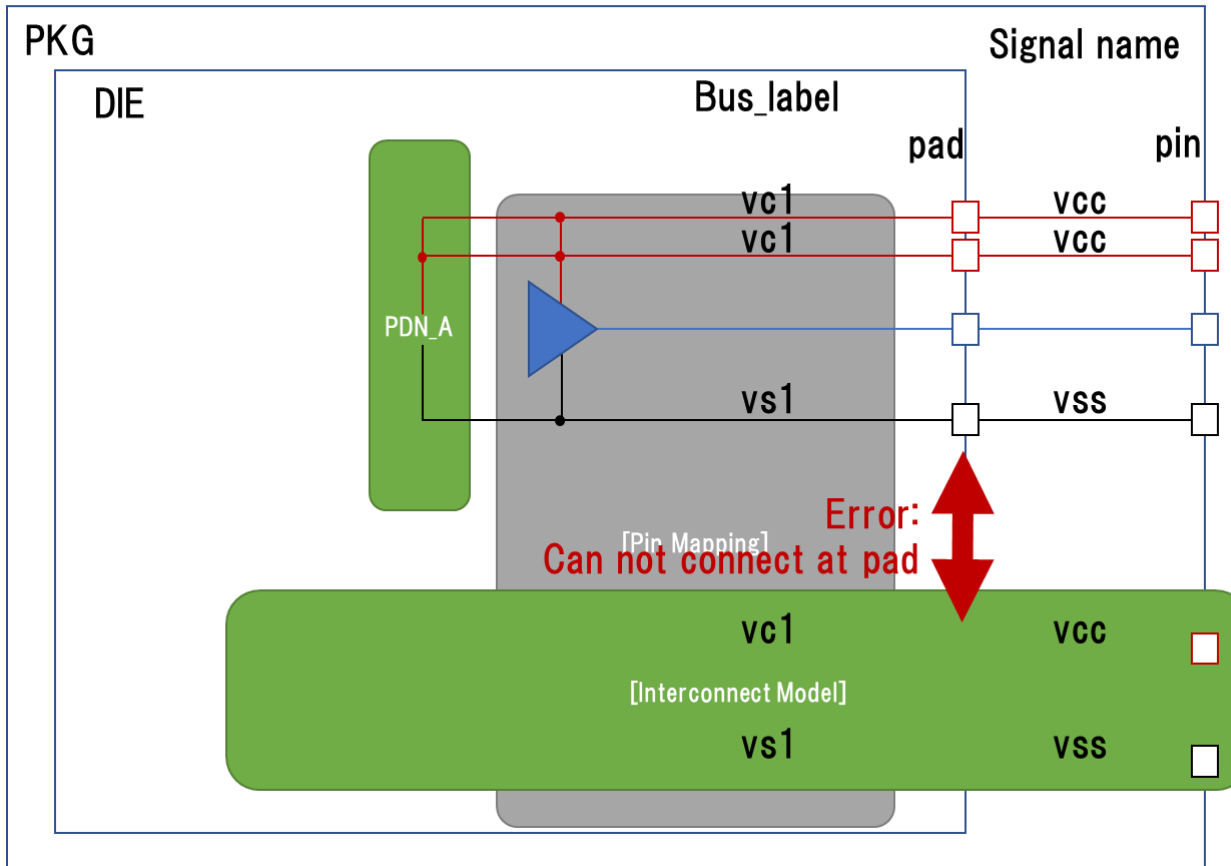
4. We have listed the case of using [On Die Decap Modeling Mapping] and/or [Interconnect Model]

The cases of using [On Die PDN Model Mapping]

Condition A	Condition B	Condition C	Condition D	Fig.	Notes
Whether or not [Pin Mapping] exists.	Whether or not [Interconnect Model] exists.	When condition B is ✓, whether or not the bus_label of the Interconnect Model terminals and that of the On-Die PDN Model terminals are the same.	When condition C is ✓, whether or not the Interconnect Model has pads whose bus_labels are the same as condition C.		
✓(exist) / ✗(not)	✓(exist) / ✗(not)	✓(same) / ✗(not)	✓(same) / ✗(not)		<> :Category of IBISCHK message. (JEITA proposal)
✗	✗	N/A	N/A	Fig.1	1, On_Die_PDN_Model connects the rail pads. 2, The rail has no connection to the buffers. <Warning>
✗	✓	✗	N/A	Fig.2a Fig.2b	1, On_Die_PDN_Model connects the rail pads. 2, The rail has no connection to the buffers. <Warning> 3, The Interconnect Model and On_Die_PDN_Model exist independently.
✗	✓	✓	✗	Fig.3	1, There is no connection between the Interconnect Model and On_Die_PDN_Model. <Error>
✗	✓	✓	✓	Fig.4a Fig.4b	1, On_Die_PDN_Model and the Interconnect Model connect the rail pads. 2, The rail between the pads and buffer terminals is assumed to be connected with an ideal short by [Pin Mapping] (to be confirmed) 3, There is a possibility of double counted PDN model. <Warning>
✓	✗	N/A	N/A	Fig.5a Fig.5b	1, On_Die_PDN_Model connects the rail pads. 2, The rail between the pads and buffer terminals is assumed to be connected with an ideal short by [Pin Mapping] 3, There is a rail that is not connected to the buffers.(Fig.5b) <Warning>
✓	✓	✗	N/A	Fig.6	1, On_Die_PDN_Model connects the rail pads. 2, The rail between the pads and buffer terminals is assumed to be connected with an ideal short by [Pin Mapping] 3, The Interconnect Model and On_Die_PDN_Model exist independently.
✓	✓	✓	✗	Fig.7	1, There is no connection between the Interconnect Model and On_Die_PDN_Model. <Error>
✓	✓	✓	✓	Fig.8	1, On_Die_PDN_Model and the Interconnect Model connect the rail pads. 2, The rail between the pads and buffer terminals is assumed to be connected with an ideal short by [Pin Mapping] (to be confirmed) 3, There is a possibility of double counted PDN model. <Warning>

Example 1

fig.7



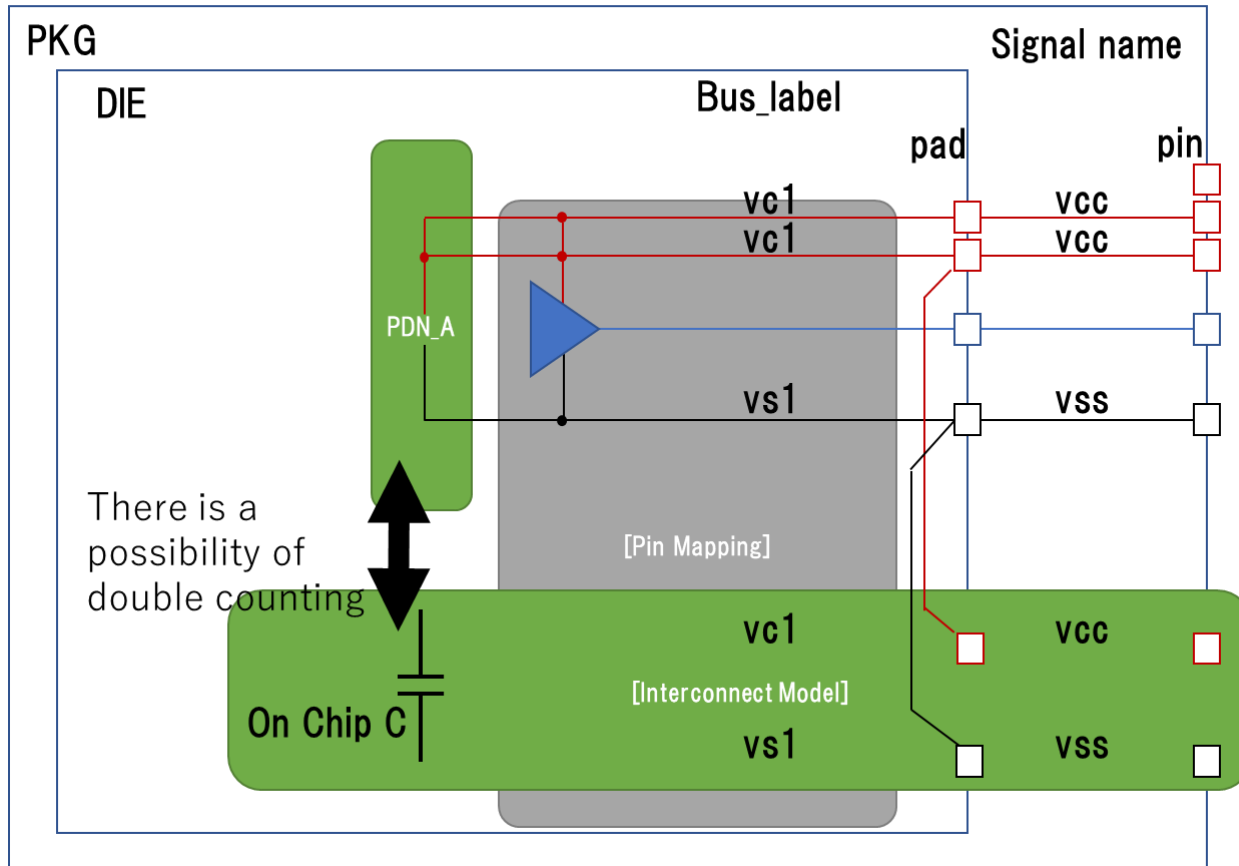
```

[Pin] signal_name model_name
2 vcc POWER
3 vcc POWER
4 sig buf1
5 vss GND
7 vcc POEWR
8 vss GND
|
[Pin Mapping]
2 NC vc1
3 NC vc1
5 vs1 NC
7 NC vc1
8 vs1 NC
4 vs1 vc1 NC NC NC
|
[On Die PDN Model Mapping]
vc1 vs1 OnChipDecapA
|
[Model] OnChipDecapA
Model_type On_Die_PDN
[C pdn] 3n 2.9n 3.1n
[R pdn] 0.1 0.1 0.1
[R leak] 200 200 200
|
[Interconnect Model] model_2
File_TS sample2.s4p
Number_of_terminals = 4
1 Pin_Rail signal_name vcc
2 Pin_Rail signal_name vss
3 Pad_Rail bus_label vc1
4 Pad_Rail bus_label vs1

```

Example 2

fig.8



```
[Pin] signal_name model_name
2 vcc POWER
3 vcc POWER
4 sig buf1
5 vss GND
7 vcc POEWR
8 vss GND
|
[Pin Mapping]
2 NC vc1
3 NC vc1
5 vs1 NC
7 NC vc1
8 vs1 NC
4 vs1 vc1 NC NC NC
|
[On Die PDN Model Mapping]
vc1 vs1 OnChipDecapA
|
[Model] OnChipDecapA
Model_type On_Die_PDN
[C pdn] 3n 2.9n 3.1n
[R pdn] 0.1 0.1 0.1
[R leak] 200 200 200
|
[Interconnect Model] model_1
File_TS sample1.s2p
Number_of_terminals = 2
1 Pin_Rail signal_name vcc
2 Pin_Rail signal_name vss
```

List of syntax candidates

	Syntax A	Syntax B	Syntax C
	Updated BIRD198	New Proposal from IBIS Open Forum (Ex.1)	New Proposal from IBIS Open Forum (Ex.2)
Connection	Bus_label	Bus_label	Bus_label
Parent	[Model]	[Component]	[Component]
Model selecting Method	✓ [Model Selector]	✓ Alternative method	✓ Alternative method
Corner definition	The order of the values does not have to be typ / min / max	Define for C/R parameter names aligned by corner (C_pdn_corner, etc.) or not related to a corner (C_pdn, etc.).	Define typ / min / max values separately each in [PDN Model]
Base structure	Series Model	[Interconnect Model]	[Interconnect Model]
EDA Vendor	Difficult implementation	easy implementation	easy implementation

2nd Feedback from IBIS Open Forum

We were very impressed with your detailed solutions to address previous comments as well as your thorough descriptions of BIRD198 and BIRD189 interactions in the PowerPoint document. We have now had two good discussions on the BIRD198.1 draft proposal. I will attempt to summarize our questions, comments, and an alternate syntax idea proposed by Walter Katz.

Questions/comments:

1. We are wondering why the BIRD allows use of [Model Selector] for the [Model] name included in the [On Die PDN Model Mapping] keyword. Is this for consistency with all other [Model] types or is there a real technical need for it? If the latter, do you have an example for where more than one selection of an On Die PDN Model could be useful?
2. Are the [R pdn], [C pdn], [R leak] and [R pdn corner], [C pdn corner], [R leak corner] keywords included for consistency with the existing structures for C_comp modeling ([Model] C_comp* subparameters vs. [C Comp Corner] C_comp* subparameters)? We think it would be simpler to have only one method of including these keywords. The 'corner' method to associate the values with the typ/min/max corners rather than by magnitude seems like the better approach to ensure consistent use of the model in simulation.
3. Interactions between BIRD189 and BIRD198 were discussed. There was agreement that allowing both to co-exist would simplify rules and IBISCHK parsing. Language could be added to the BIRD to clarify that it is the burden of the model maker to ensure that on-die decoupling is not double counted. The examples in Fig. 3 and Fig. 7 of the bird198p1_fig_20190820.pptx document would not be errors in this case. These cases could be real examples where a model maker is modeling on-package decoupling with BIRD189 syntax and on-die decoupling with BIRD198 syntax.
4. Requiring the existence of [Pin Mapping] seems appropriate and would simplify parser checking.

Some of the EDA vendors expressed their opposition to the addition of a new [Model] type to represent the on-die PDN model. Implementing a new type of [Model] in existing EDA software is rather difficult, requiring major code changes, schematic symbol changes, GUI changes, etc. Walter Katz proposed a simplified alternative syntax which would place the on-die PDN models under the scope of the [Component] keyword with the addition of a few simple keywords, such as [R pdn], [C pdn], [R leak]. This appears to be easier to implement and support in EDA tools. Putting the keywords under the [Component] scope is also good because (unlike [Model]) this structure is bus_label centric, not pin-centric.

Walter's draft syntax proposal looks like this:

```
[On Die PDN Models]

[PDN Model] VDDAVSS
[Rail Bus Labels] VDDA VSS | (Note) Bus_Labels can be Rail signal_names
[C pdn] 3n 2.9n 3.1
[R pdn] 0.1 0.1 0.1
[R leak] 200 200 200
[End PDN Model]

[PDN Model] VDDBVSS
[Rail Bus Labels] VDDB VSS
[C pdn] 3n 3.1n 2.9n
[R pdn] 0.1 0.1 0.1
[R leak] 200 200 200
[End PDN Model]
```

A new syntax proposal from the IBIS Open Forum for easy implementation by EDA vendors.

3rd Feedback from IBIS Open Forum

We have had a lot of discussion about the meaning of corner cases for the C_pdn, R_pdn, and R_leak parameters. In my experience, there is not typically a correlation between the PDN corner parameters and the transistor corner parameters. The PDN decoupling capacitance can be fabricated with many technologies such as MOS cap, MIM cap, DRAM storage cap, etc. So, the min/max values of the PDN capacitance usually are not related to the same slow/fast (min/max) transistor process corners. It's also difficult to say what becomes the best/worst case model for the PDN, since this can have a lot to do with the resonant frequency of the PDN C with package L, and what frequency the buffer is switching at. For example, in a SSO simulation, you might need to sweep all the PDN corners with the slow/fast transistor model corners to see what corner case generates the worst simultaneous switching noise.

So, we think it is necessary to include syntax supporting:

1. A PDN model with C_pdn, R_pdn, and R_leak parameters for 3 corners, where the corners are correlated with the Model typ/min/max corners.
2. Multiple PDN models (like the Model Selector concept) with single C_pdn, R_pdn, and R_leak parameter values (not supporting corners, not correlated to Model typ/min/max corners). The EDA tool would see these models as selected by group.

We also discussed another syntax proposal from Walter that would align better to the BIRD189 syntax. We would like your feedback on the idea presented below:

Notes:

1. The [PDN Group] is scoped under [Component].
2. Multiple [PDN Model] sections can exist with a [PDN Group]/[End PDN Group] section, for example to model VDD-VSS and VDDQ-VSS.
3. There is different syntax for C/R parameter names aligned by corner (C_pdn_corner, etc.) or not related to a corner (C_pdn, etc.).
4. If there are "corners" not correlated with process, then we can have one [PDN Group] for each of these uncorrelated "corners". There could be 1 PDN corner, 2 PDN corners, 3 PDN corners, and more than 3 PDN corners (implemented as separate [PDN Group]s).
5. This syntax also changes some keywords to subparameters within the [PDN Model]/[End PDN Model] section.
6. The EDA tool would have a single PDN Group selector. Once any group is selected then all is automatic.

```
| Example 1, one group correlated with typ/slow/fast IV/VT
| curves - one group, three corners
|-----
```

```
-----
[PDN Group] ProcessCorners
[PDN Model] VDDVSS_Corner
Rail_Bus_Labels VDD VSS
C_pdn_corner    100f  150f  50f
R_pdn_corner    0.1   0.05  0.15
R_leak_corner   200   300   100
[End PDN Model]
[End PDN Group]
```

```
| Example 2, two groups, not correlated with process corners
|-----
```

```
-----
[PDN Group] LargeCap
[PDN Model] VDDVSS_LargeCap
Rail_Bus_Labels VDD VSS
C_pdn = 150f
R_pdn = 0.05
R_leak = 300
[End PDN Model]
[End PDN Group]
```

```
[PDN Group] SmallCap
[PDN Model] VDDVSS_SmallCap
Rail_Bus_Labels VDD VSS
C_pdn = 50f
R_pdn = 0.15
R_leak = 100
[End PDN Model]
[End PDN Group]
```


3rd Feedback from IBIS Open Forum

Syntax B: 3rd feedback (Example 1)

```
[Component]      AAA
  [PDN Group] PDN_for_DDR3
    [PDN Model] VDDVSS_for_Core
      Rail_Bus_Labels VDD VSS
      C_pdn_corner      100n    150n    50n
      R_pdn_corner      0.1    0.05   0.15
      R_leak_corner    200    300    100
    [End PDN Model]
    [PDN Model] VDDQVSS_for_DDRIO
      Rail_Bus_Labels VDDQ VSS
      C_pdn_corner      10n    2n     25n
      R_pdn_corner      10m    15m    5m
      R_leak_corner    500    800    50
    [End PDN Model]
  [End PDN Group]
  [PDN Group] PDN_for_DDR4
    [PDN Model] VDDVSS_for_Core
      Rail_Bus_Labels VDD VSS
  ...
```

1. The [PDN Group] is scoped under [Component].
2. Multiple [PDN Model] sections can exist with a [PDN Group]/[End PDN Group] section, for example to model VDD-VSS and VDDQ-VSS.
3. There is different syntax for C/R parameter names aligned by corner (C_pdn_corner, etc.) or not related to a corner (C_pdn, etc.).
4. This syntax also changes some keywords to subparameters within the [PDN Model]/[End PDN Model] section.
5. The EDA tool would have a single PDN Group selector. Once any group is selected then all is automatic.

3rd Feedback from IBIS Open Forum

Syntax C: 3rd feedback (Example 2)

```
[Component]      AAA
  [PDN Group] LargeCap_for_DDR3
    [PDN Model] VDDVSS_for_core
      Rail_Bus_Labels VDD VSS
      C_pdn = 150n
      R_pdn = 0.05
      R_leak = 300
    [End PDN Model]
    [PDN Model] VDDQVSS_for_DDRIO
      Rail_Bus_Labels VDDQ VSS
      C_pdn = 25n
      R_pdn = 15m
      R_leak = 800
    [End PDN Model]
  [End PDN Group]
  [PDN Group] SmallCap_for_DDR3
    [PDN Model] VDDVSS_for_core
      Rail_Bus_Labels VDD VSS
      C_pdn = 50n
```

...

1. The [PDN Group] is scoped under [Component].
2. Multiple [PDN Model] sections can exist with a [PDN Group]/[End PDN Group] section, for example to model VDD-VSS and VDDQ-VSS.
3. If there are “corners” not correlated with process, then we can have one [PDN Group] for each of these uncorrelated “corners”. There could be 1 PDN corner, 2 PDN corners, 3 PDN corners, and more than 3 PDN corners (implemented as separate [PDN Group]s).
4. This syntax also changes some keywords to subparameters within the [PDN Model]/[End PDN Model] section.
5. The EDA tool would have a single PDN Group selector. Once any group is selected then all is automatic.

List of syntax candidates

	Syntax A	Syntax B	Syntax C
	Updated BIRD198	New Proposal from IBIS Open Forum (Ex.1)	New Proposal from IBIS Open Forum (Ex.2)
Connection	Bus_label	Bus_label	Bus_label
Parent	[Model]	[Component]	[Component]
Model selecting Method	✓ [Model Selector]	✓ Alternative method	✓ Alternative method
Corner definition	The order of the values does not have to be typ / min / max	Define for C/R parameter names aligned by corner (C_pdn_corner, etc.) or not related to a corner (C_pdn, etc.).	Define typ / min / max values separately each in [PDN Model]
Base structure	Series Model	[Interconnect Model]	[Interconnect Model]
EDA Vendor	Difficult implementation	easy implementation	easy implementation

Agenda

- Background
- Proposal for On die De-cap model
- Feedback and updating
- **Conclusion**

Conclusion

Chip PDN model is still not widespread. Therefore, we proposed to add an **explicit keyword** of chip PDN to IBIS.

Our proposal was registered as BIRD198 and it has been discussing in IBIS Open Forum since this March.

We will continue to work to accept BIRD198 in the next version of IBIS.

We would like to get your feedback from JAPANESE USER!

Please access “JEITA semiconductor and system design Technical Committee (JEITA-SDTC)” Web site and send comment!

Thank you!

JEITA-SDTC Web Site&Inquiry

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[Comments on BIRD198]

[Application period]
Nov. 8, 2019~Nov.22, 2019



<http://jeita-sdtc.com/>

Thank you for your support and feedback!
We really appreciate all of the IBIS Open Forum
members



Reference: Series Model

```
[Component]    AAA
  [Pin Mapping]
    pin_name1   NC    bus_label1
    pin_name2   bus_label2  NC
  [Series Pin Mapping]
    pin_name1 pin_name2 CCC
[Model Selector]   CCC
  DDD
  EEE
[Model]    DDD
  Model_Type   Series
  [R Series]   100 80 120
  ...

[Model]    EEE
  Model_Type   Series
  [R Series]   120 100 140
  ...
```