A potential application of IBIS to CISPR25 based EMI analysis of DCDC converter

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Agenda

- Motivation and objective
- Impedance modeling of DCDC converters
- Measurement settings and results
- Simulation results and comparison with measurement
- Discussion
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Motivation and objective

- EMI simulation of IBIS modeled DCDC converter

✓ Study on modeling to comply with CISPR25

✓ Initial trial with bare IBIS descriptions

→ Simulation results show discrepancies from measurements

- Make discussions on source of errors and solutions

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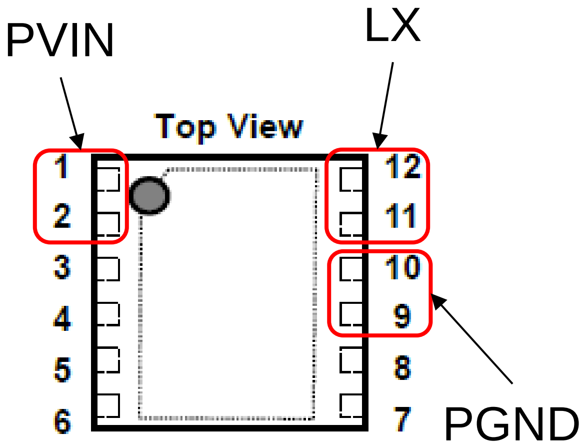
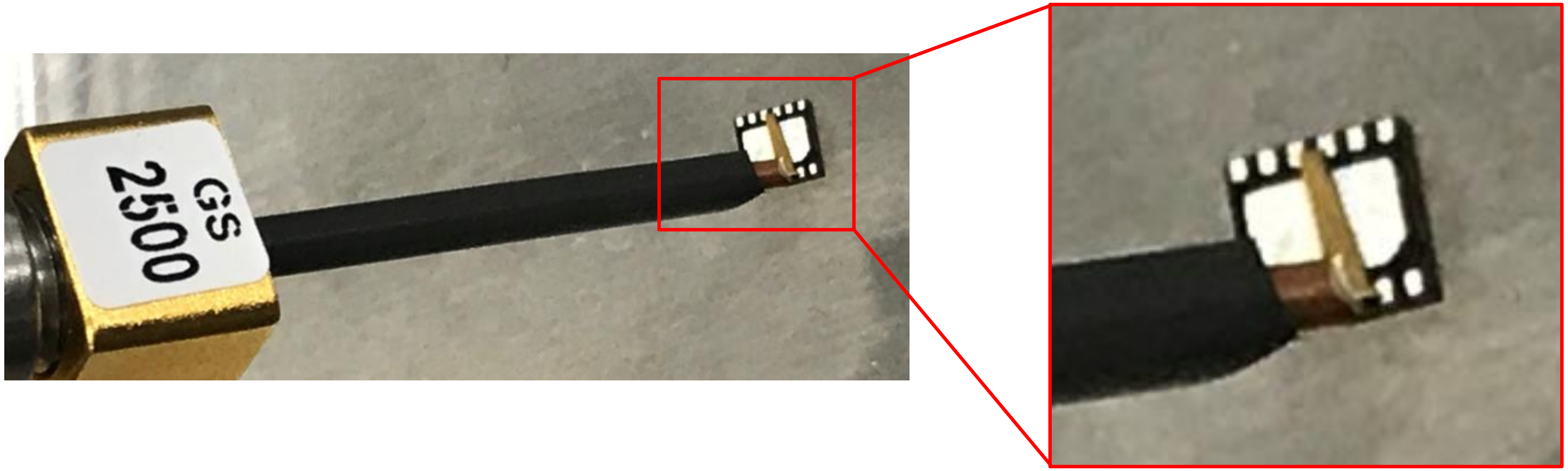
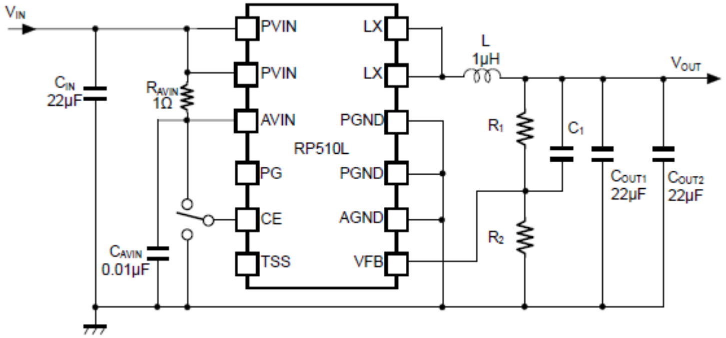
DCDC converter impedance measurement

DCDC converter: RICOH RP510L004N-TR-A







Typical Application Circuit

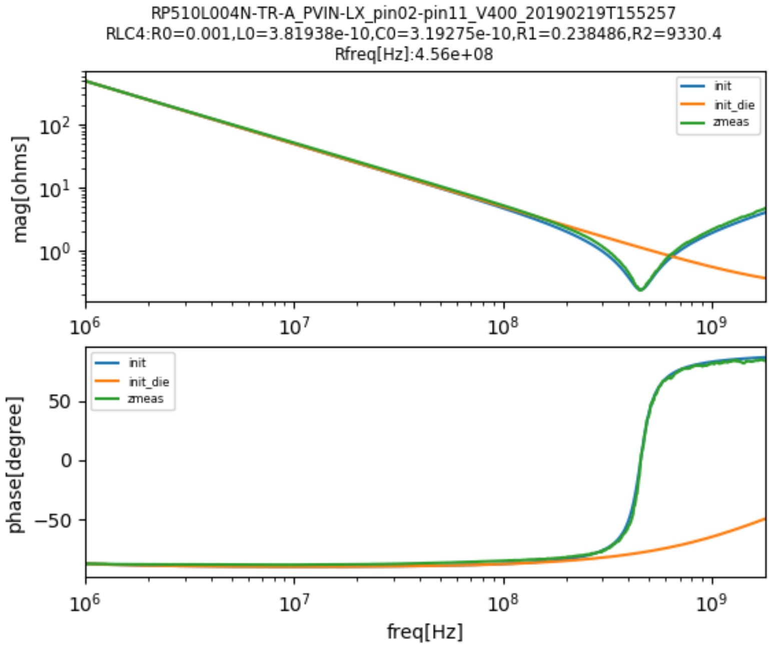
IO Pins for impedance measurement

Pin（S-G）	No.（S-G）	Pitch(mm)	Bias voltage（V）	Freq.（Hz）※
PVIN-PGND	PIN2-PIN10	2.65mm±0.3mm	0,0.3,0.6,1,2,3,3.6,4,5,5.5	1k-3G
PVIN-LX	PIN2-PIN11	2.6mm±0.3mm	0,0.3,0.6,1,2,3,3.6,4,5,5.5	1k-3G
LX-PGND	PIN11-PIN10	0.5mm±0.1mm	0,0.3,0.6,1,2,3,3.6,4,5,5.5	1k-3G

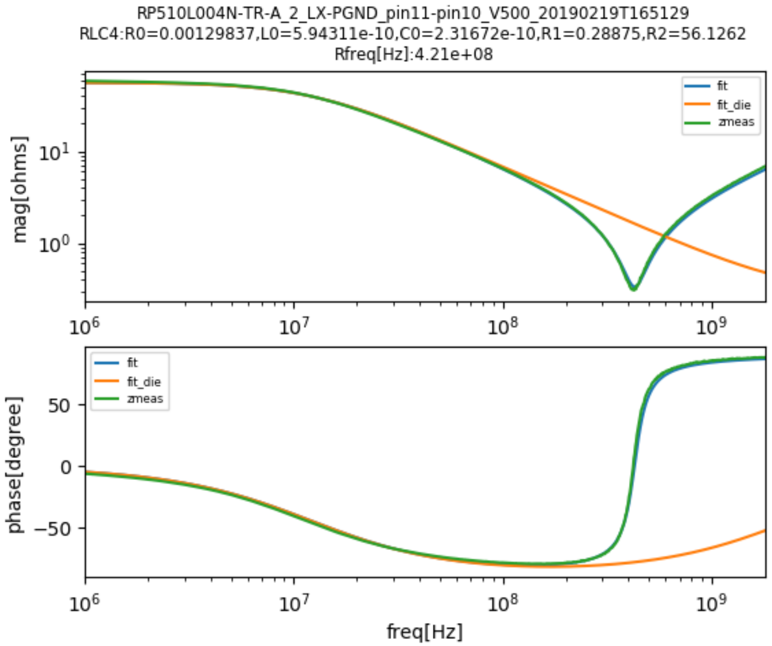
※Frequency depends on equipments

cf.) https://www.e-devices.ricoh.co.jp/en/products/power/dcdc/rp510/rp510-ea.pdf

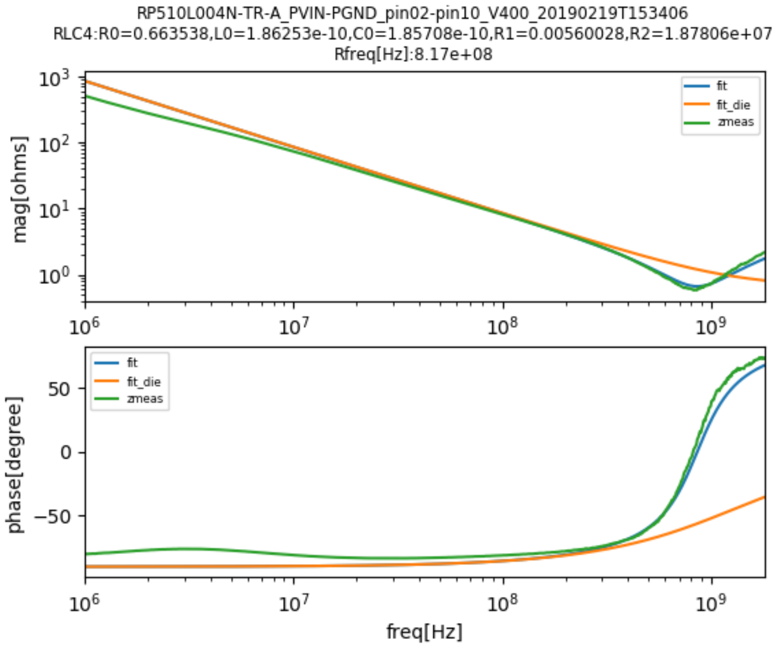
Impedance measurement and equivalent circuit



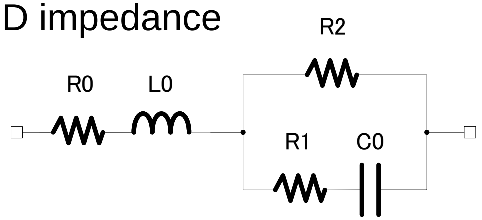
PVIN-LX impedance



LX-PGND impedance



PVIN-PGND impedance



	L(nH)	C(pF)	R(Ω)	Rleak(Ω)
PVIN-PGND	0.19	186	0.66	1.87e7
PVIN-LX	0.38	319	0.24	9339
LX-PGND	0.59	232	0.29	56.12

Series cap.
134pF

PVIN-PGND
186p-134p=52pF

Capacitance description in IBIS format

Specify the measured caps as C_comp_pullup, C_comp_pulldown in the IBIS format.

```
[Model]    bbb
Model_type        I/O
Polarity          Non-Inverting
Vinl            = .72000000
Vinh            = 2.88000000
Vmeas           = 1.80000000
|C_comp           5.53197e-10 4.65065e-10 7.07186e-10 | CDL
C_comp_pullup     319e-12     NA          NA          | Measurement
C_comp_pulldown   232e-12     NA          NA          | Measurement
```

In case that large discrepancy appear in the total capacitance, need to regenerate IBIS model adding supplemental capacitance to the spice netlist.

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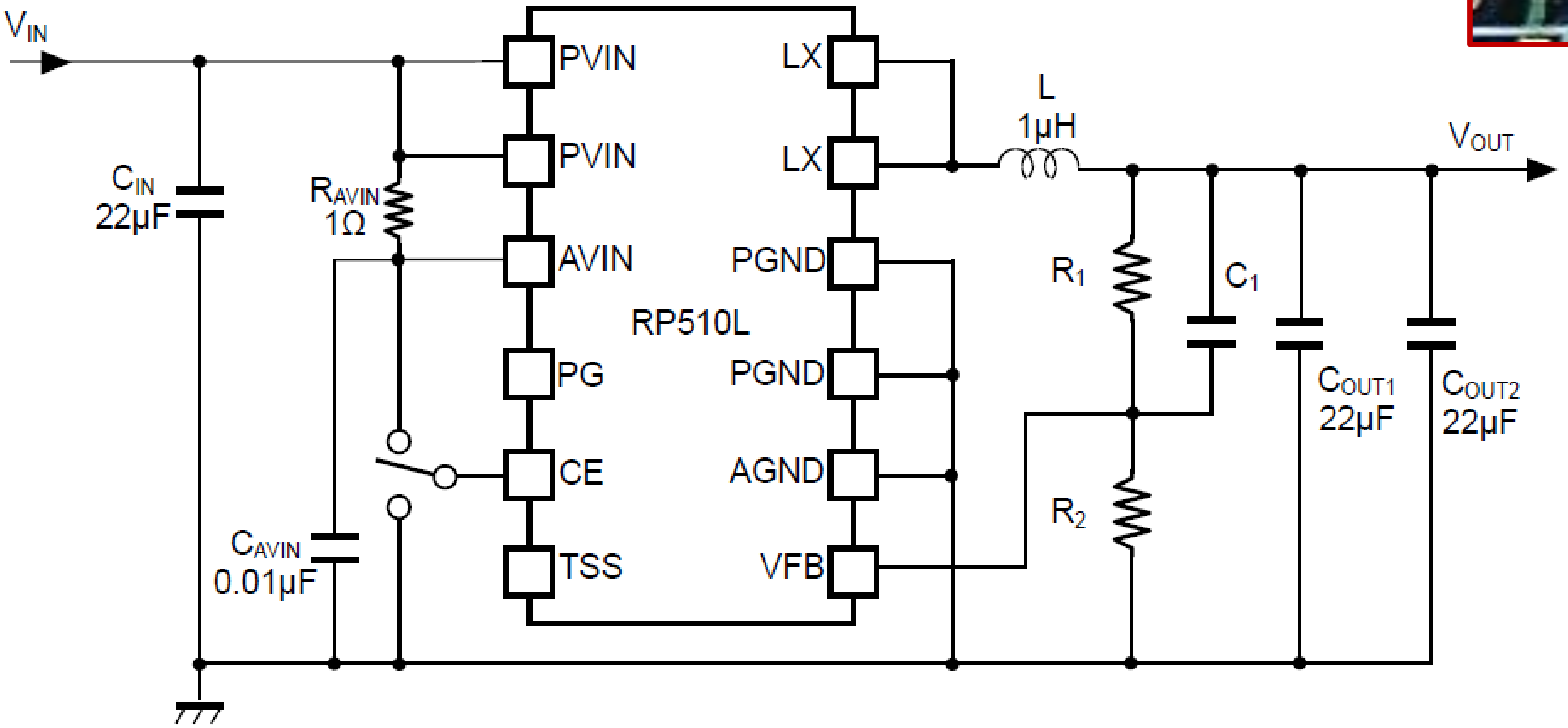
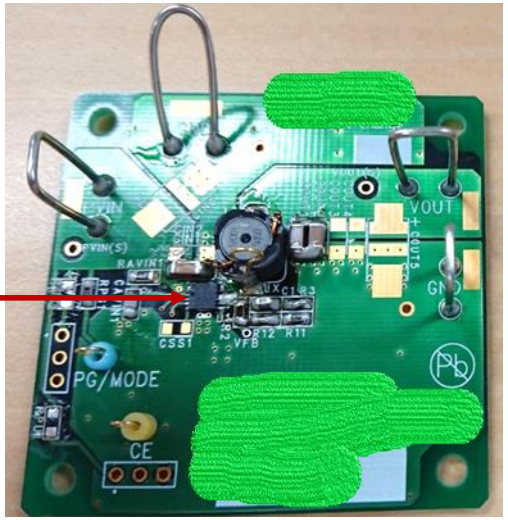
LPB

Measurement circuit construction



DUT



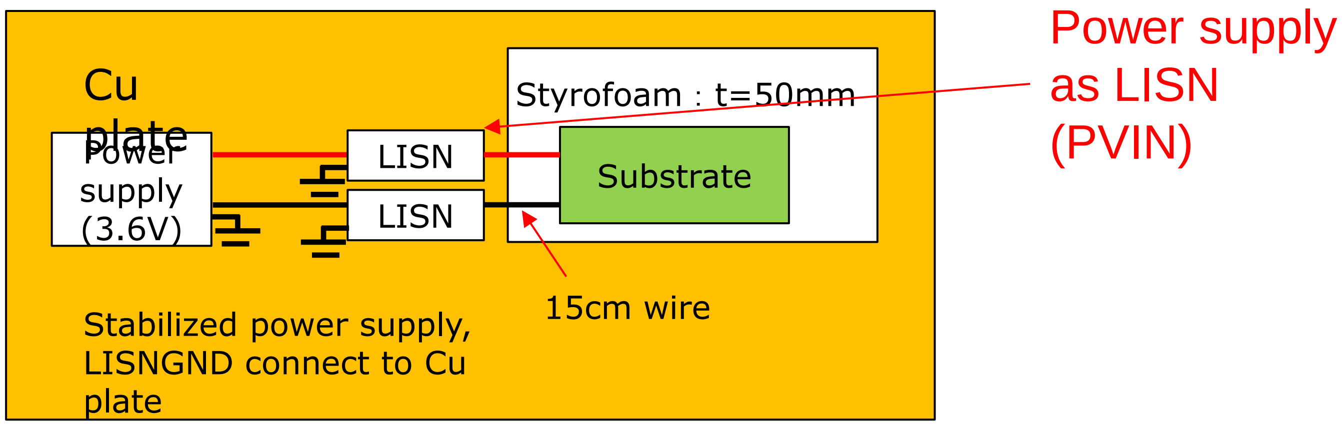
Evaluation board

Vout load

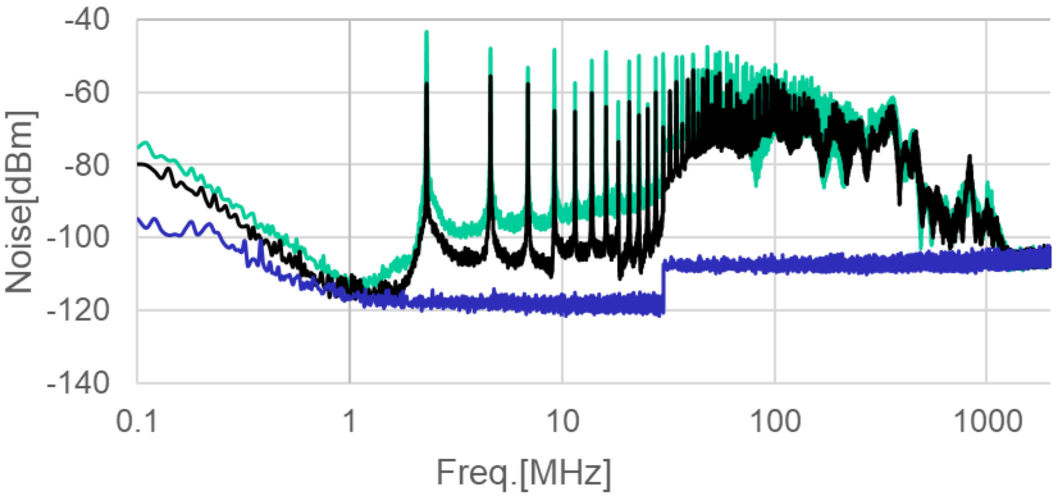
①Open

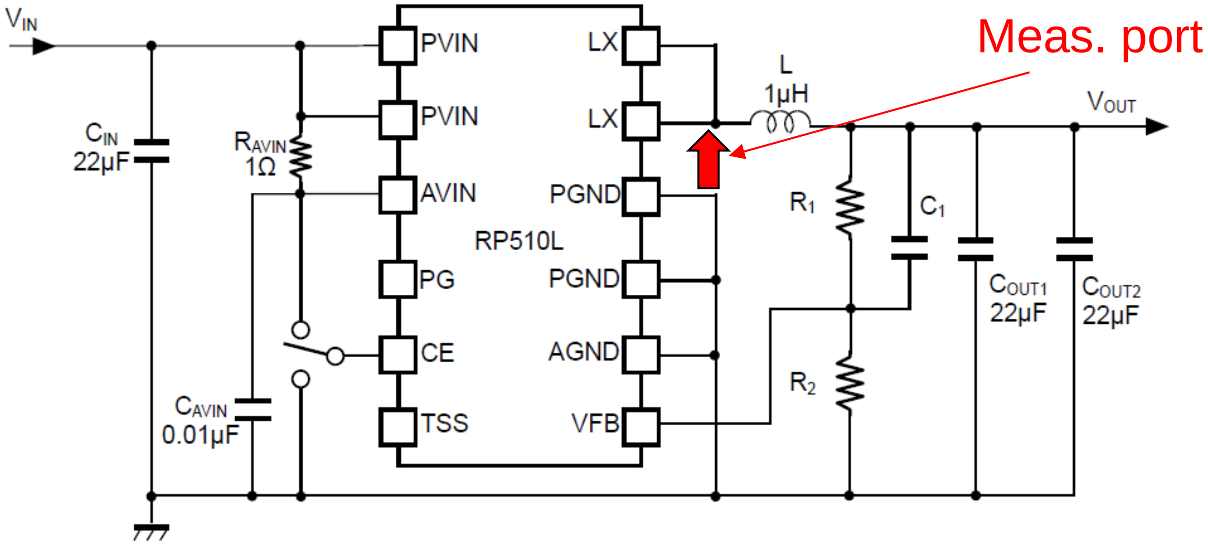
②2.2Ω

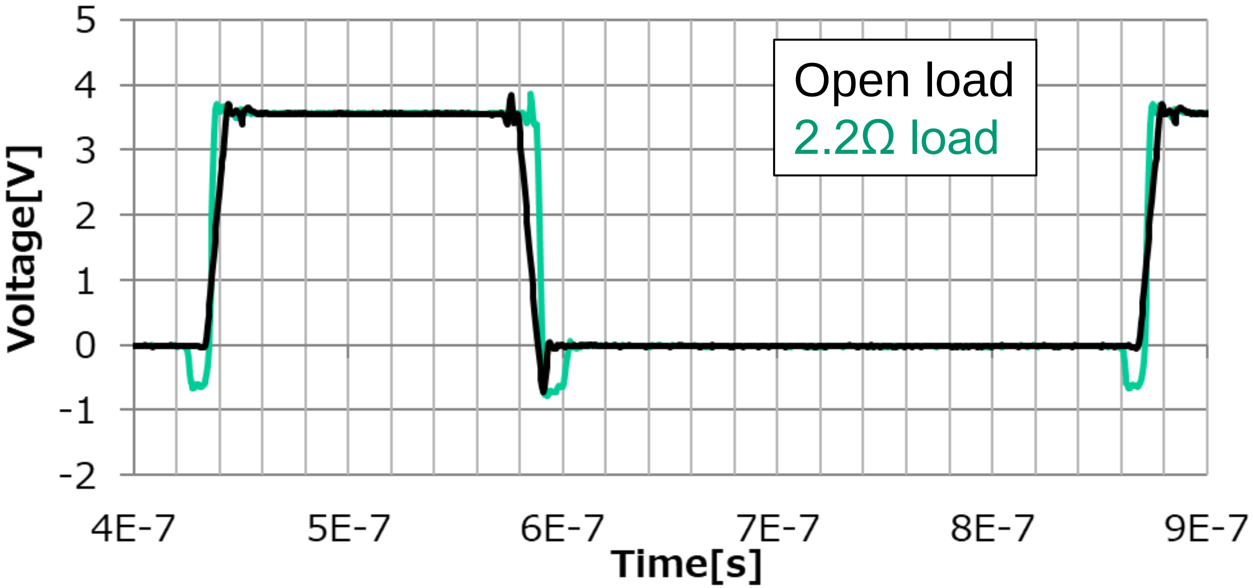
Measurement environment and results



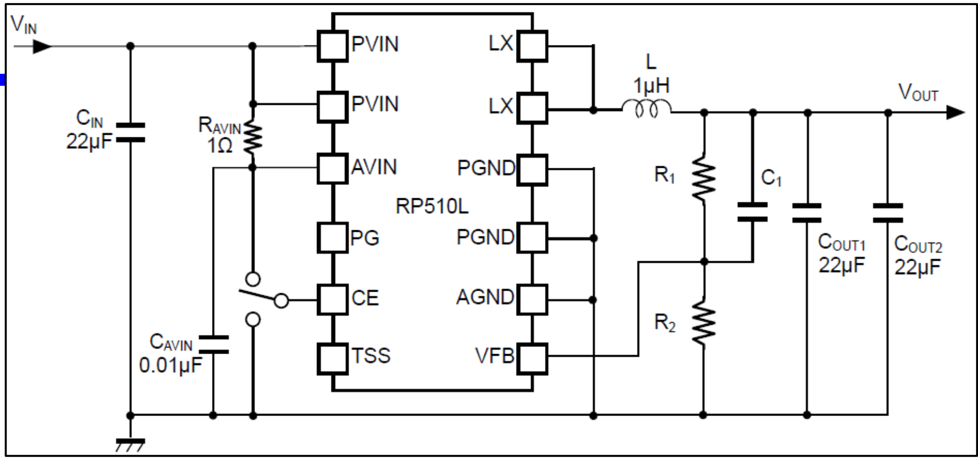
Measurement equipment inside shield





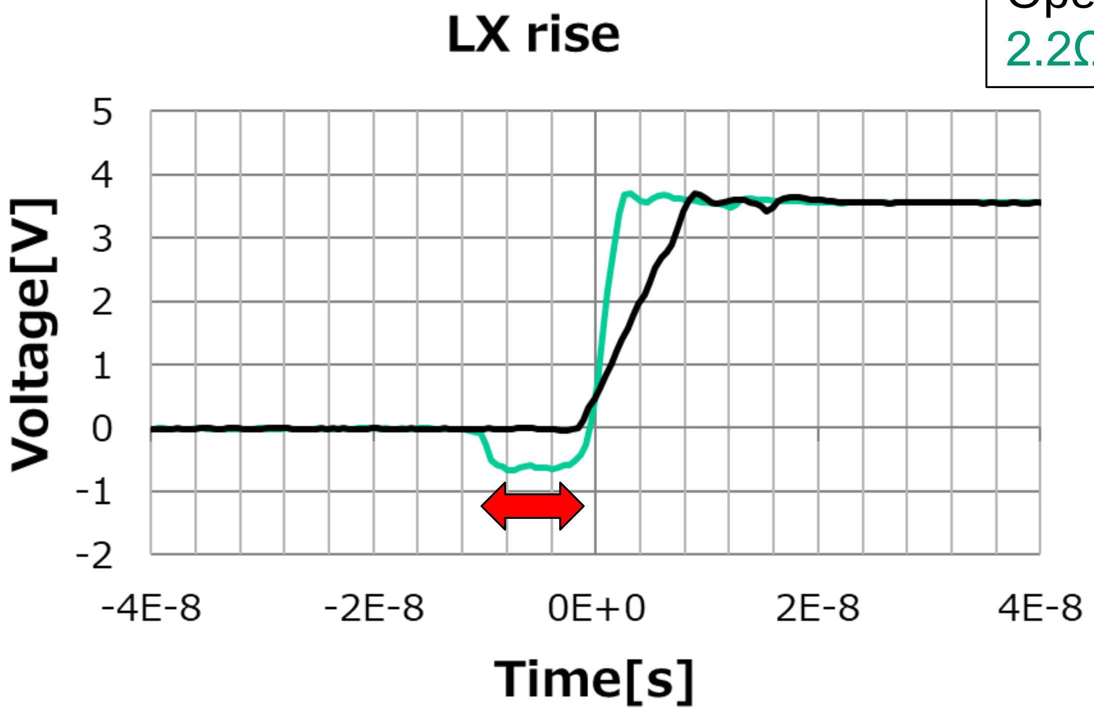


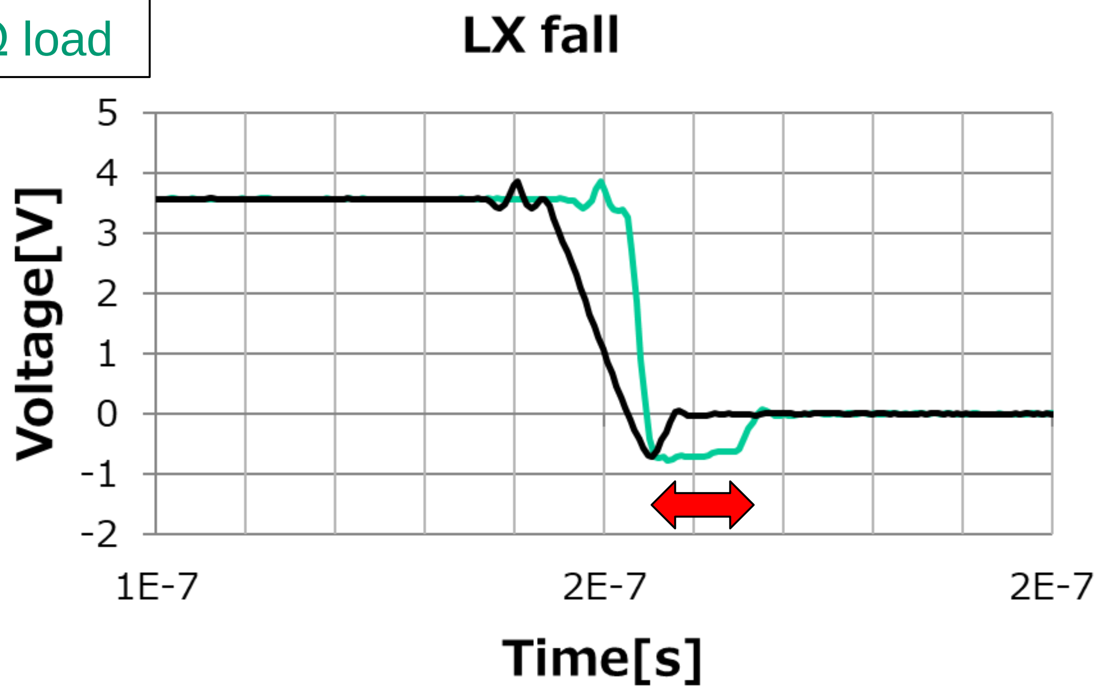
Measured LX waveform



Dead time appears in LX waveform with resistive load

Open load
2.2Ω load





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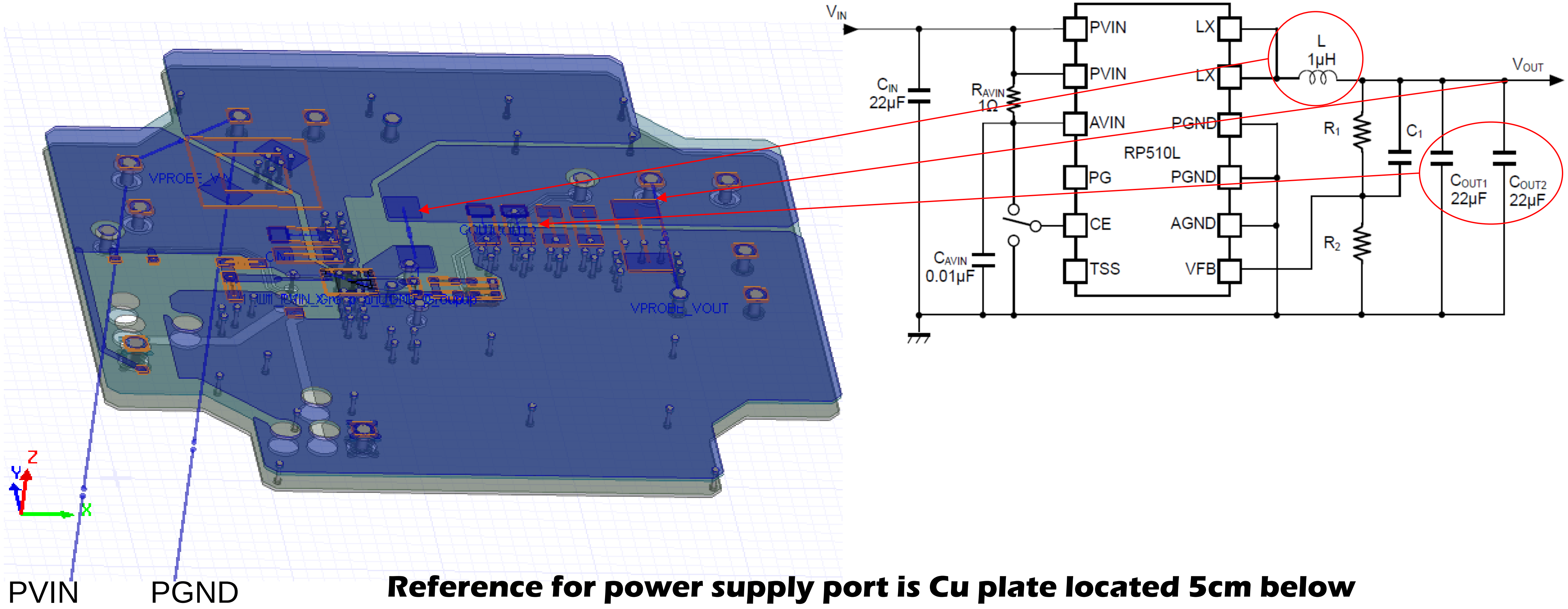
Printed circuit board model

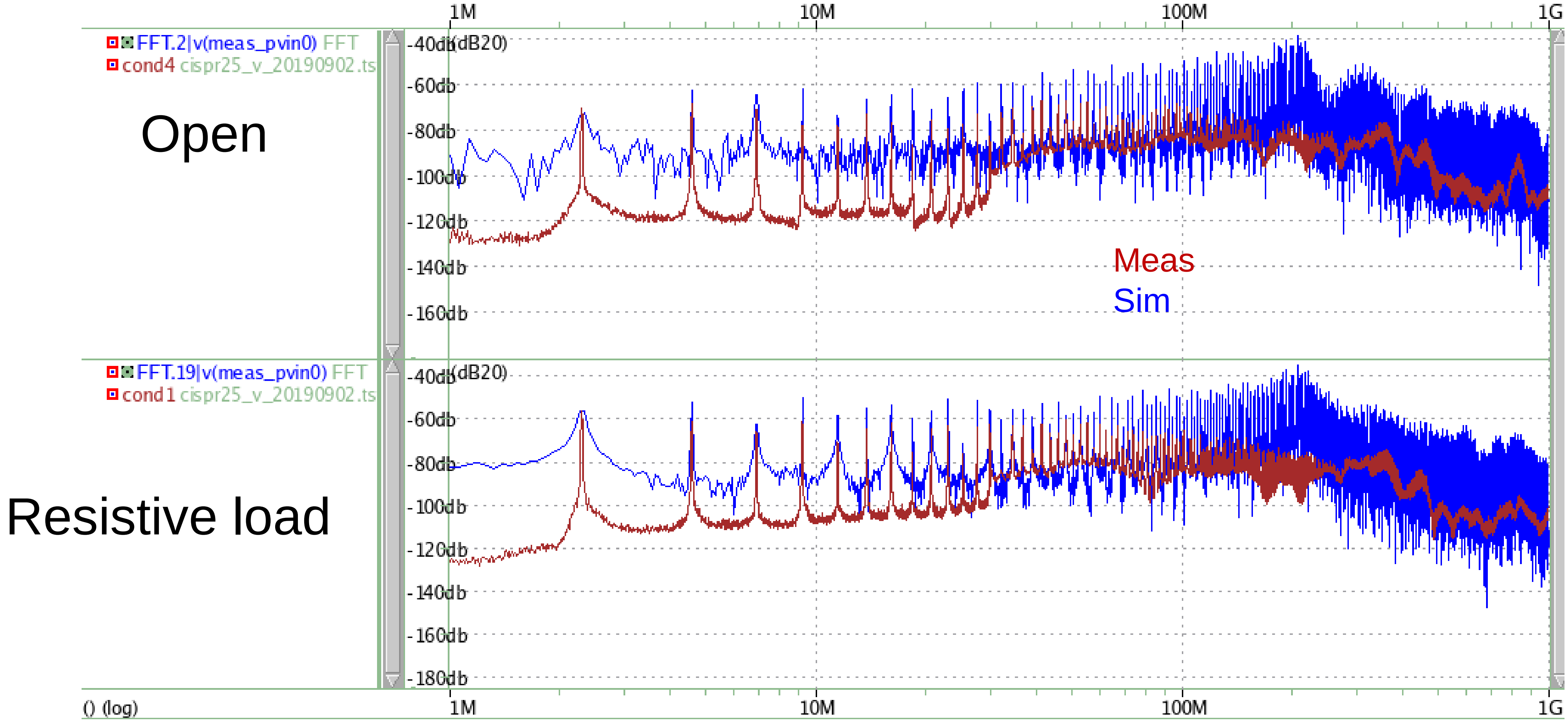
Modeling printed circuit board by electromagnetic analysis



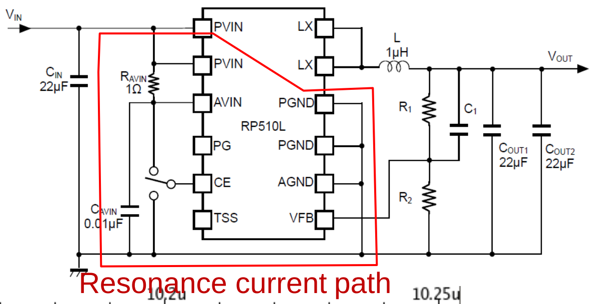
Reference for power supply port is Cu plate located 5cm below

Simulation results vs Measurement

The difference between simulation and actual measurement is very large



Simulation results：Open



Large ringing appear in the simulation results unlike measurements.

IBIS input

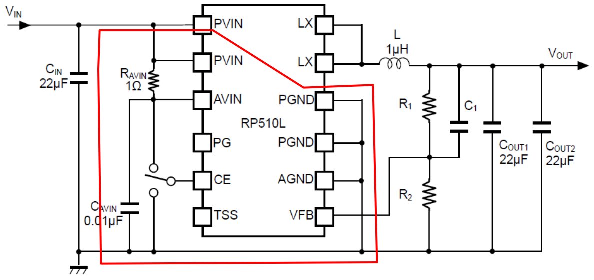
LX
（DCDC converter output）

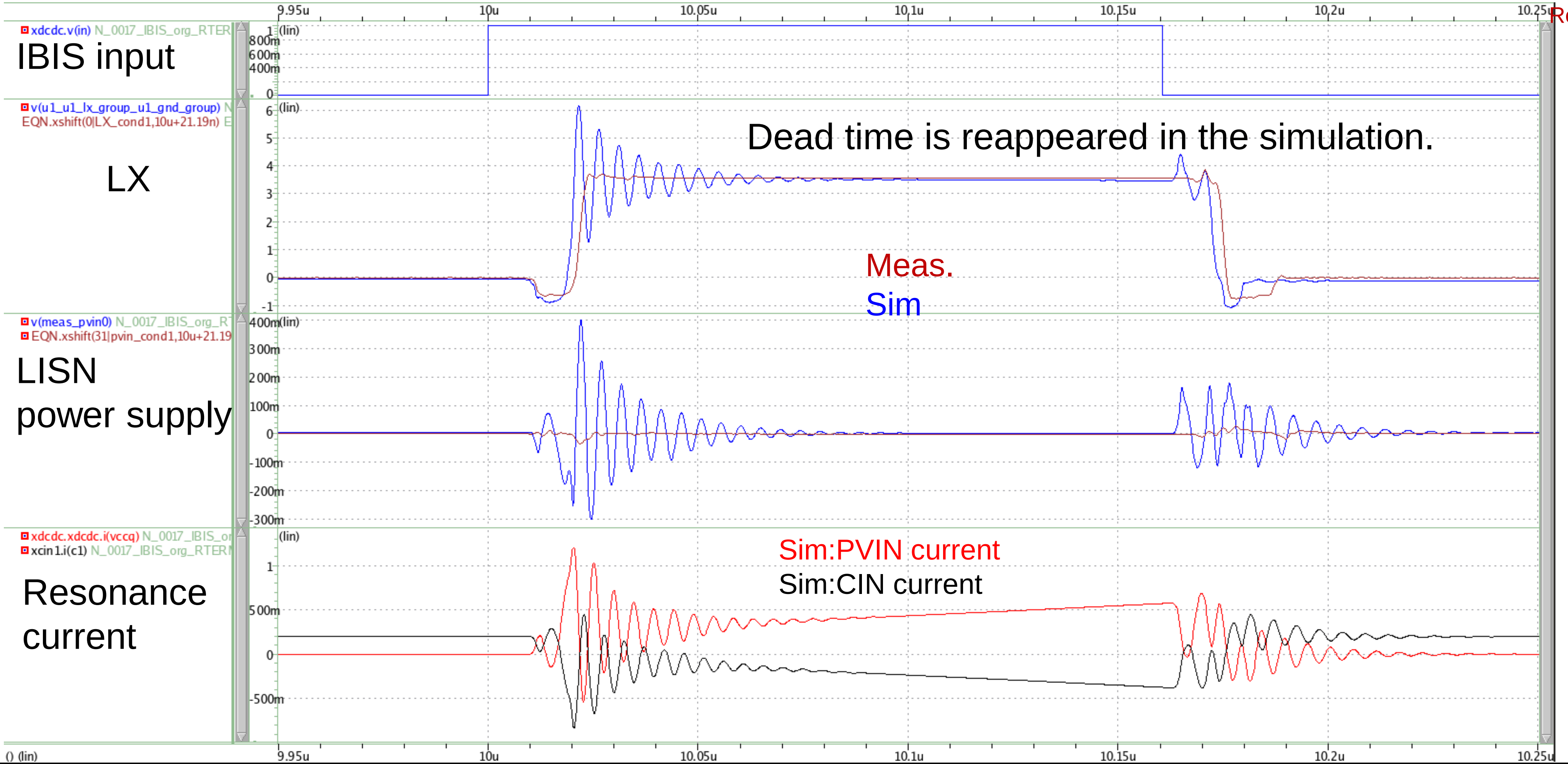
LISN power supply

Resonance current

Simulation results：Resistive load

Large ringing appear in the simulation results unlike measurements, as well.

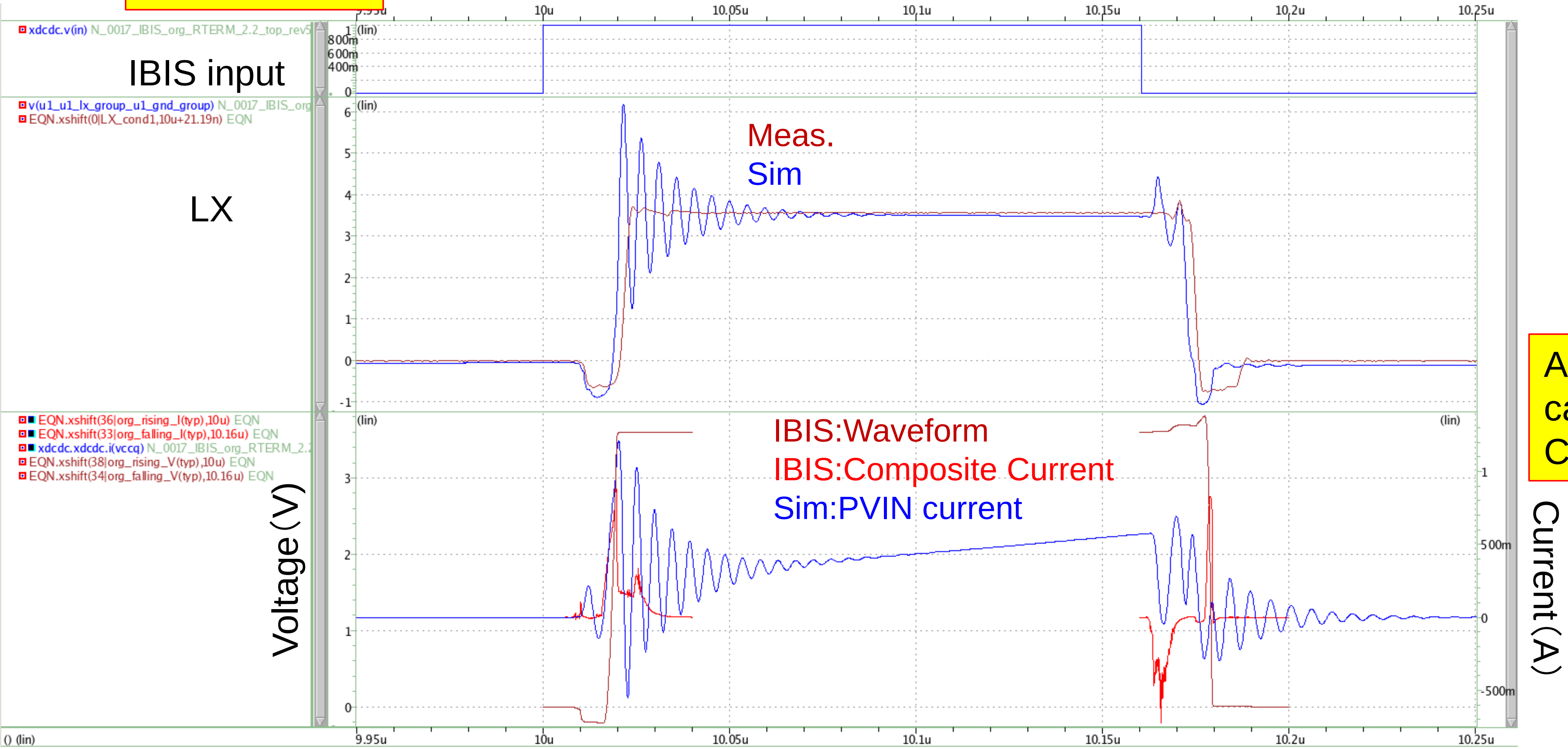




Ringing caused by resonance current path through PVIN,PGND,CIN

Dependence on Rising/Falling Waveform, composite current defined in IBIS

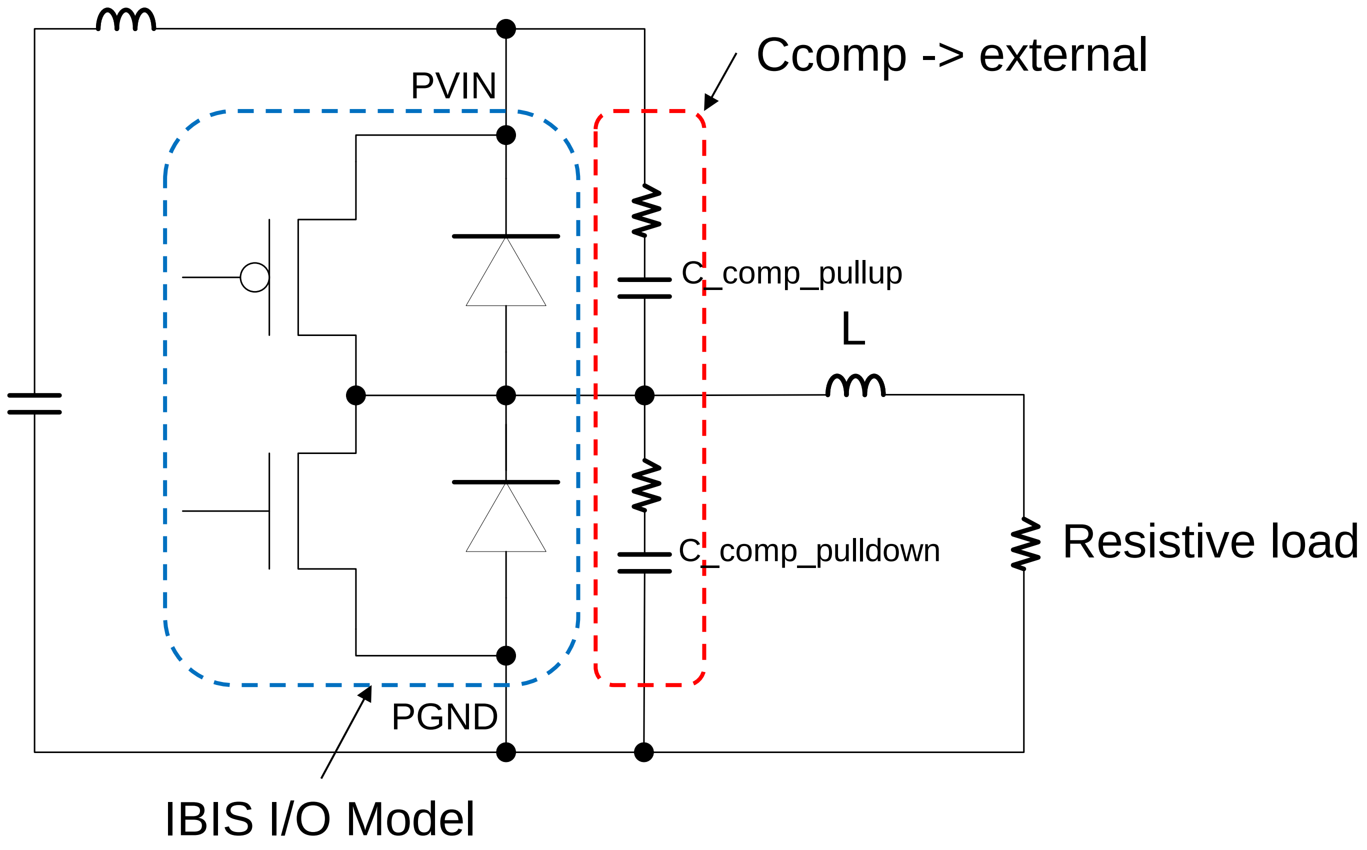
Resistive load



Appears if ringing caused by Composite Current

Changing Rising/Falling Waveform, Composite current

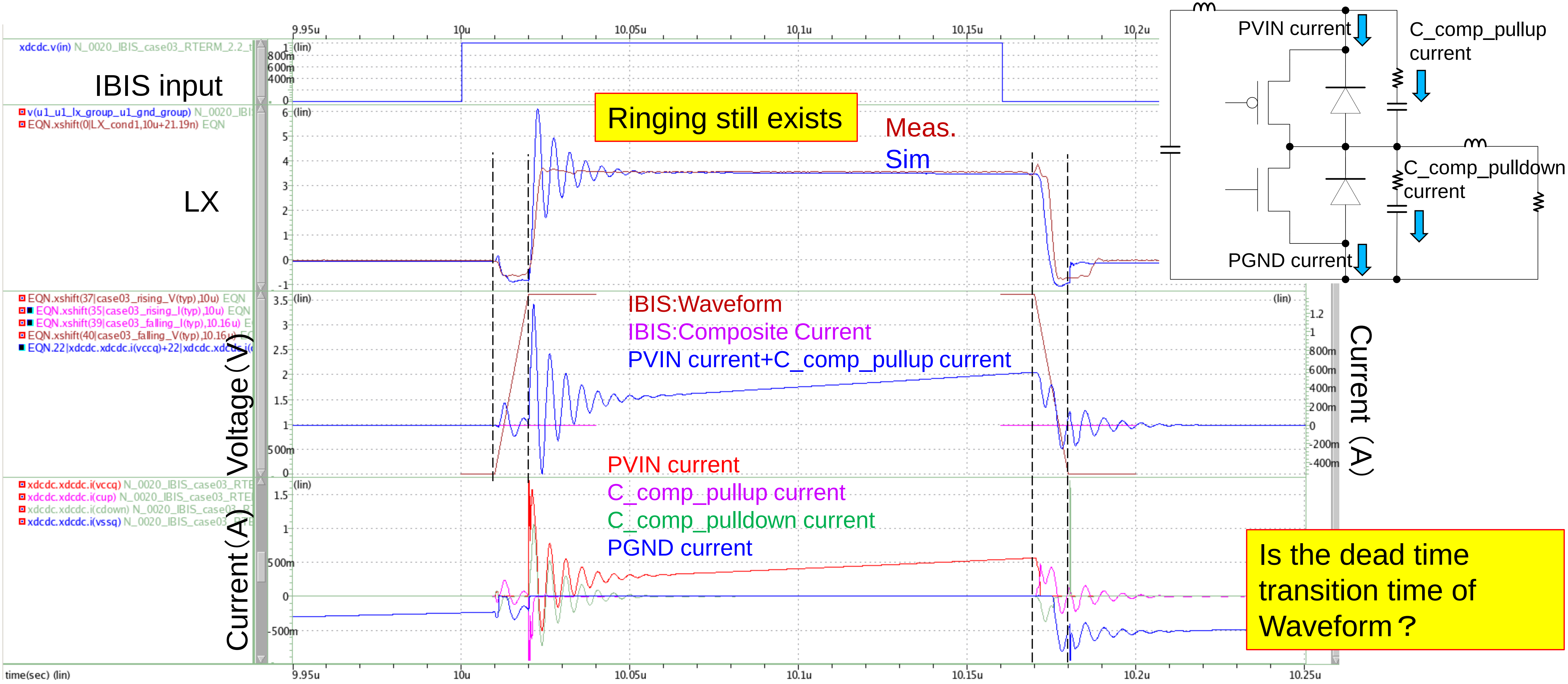
Make Ccomp external, Composite Current 0A, and Waveform simple rise/fall, respectively




```
[Rising Waveform]
R_fixture = 1000000
V_fixture = 0.000
V_fixture_min = 0.000
V_fixture_max = 0.000
| time V(typ) V(min) V(max)
|
0 0 0 0
10e-9 0 0 0
20e-9 3.6 3.2 4.0
40e-9 3.6 3.2 4.0
|
[Composite Current]
| time I(typ) I(min) I(max)
0 0 0 0
10e-9 0 0 0
20e-9 0 0 0
40e-9 0 0 0
[Rising Waveform]
R_fixture = 1000000
V_fixture = 3.600
V_fixture_min = 3.200
V_fixture_max = 4.000
| time V(typ) V(min) V(max)
|
0 0 0 0
10e-9 0 0 0
20e-9 3.6 3.2 4.0
40e-9 3.6 3.2 4.0
|
[Composite Current]
| time I(typ) I(min) I(max)
0 0 0 0
10e-9 0 0 0
20e-9 0 0 0
40e-9 0 0 0
```

```
[Falling Waveform]
R_fixture = 1000000
V_fixture = 3.6
V_fixture_min = 3.2
V_fixture_max = 4
| time V(typ) V(min) V(max)
|
0 3.6 3.2 4
10e-9 3.6 3.2 4
20e-9 0 0 0
40e-9 0 0 0
[Composite Current]
| time I(typ) I(min) I(max)
0 0 0 0
10e-9 0 0 0
20e-9 0 0 0
40e-9 0 0 0
|
[Falling Waveform]
R_fixture = 1000000
V_fixture = 0.000
V_fixture_min = 0.000
V_fixture_max = 0.000
| time V(typ) V(min) V(max)
|
0 3.6 3.2 4
10e-9 3.6 3.2 4
20e-9 0 0 0
40e-9 0 0 0
[Composite Current]
| time I(typ) I(min) I(max)
0 0 0 0
10e-9 0 0 0
20e-9 0 0 0
40e-9 0 0 0
|
```

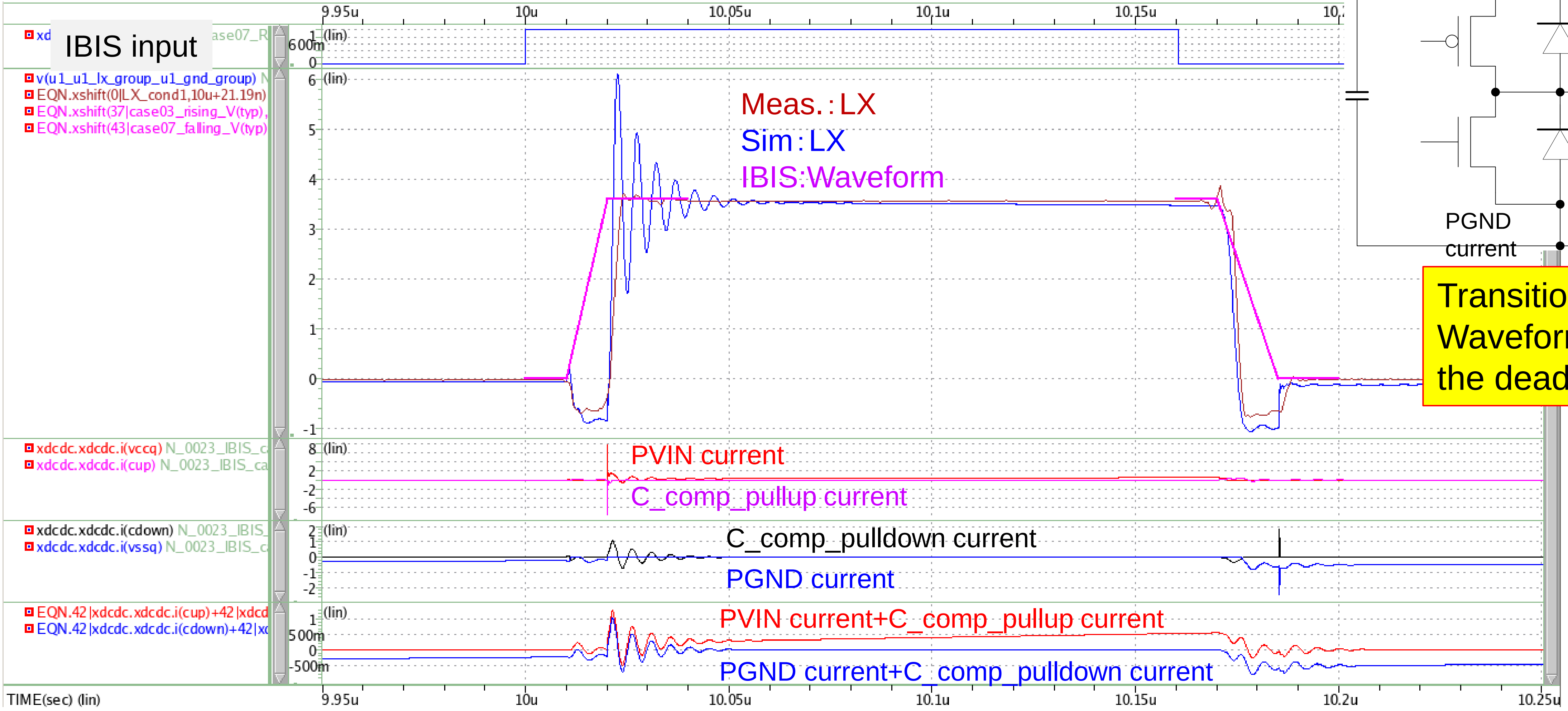
Resistive load: Dependence on Rising/Falling Waveform, Composite current

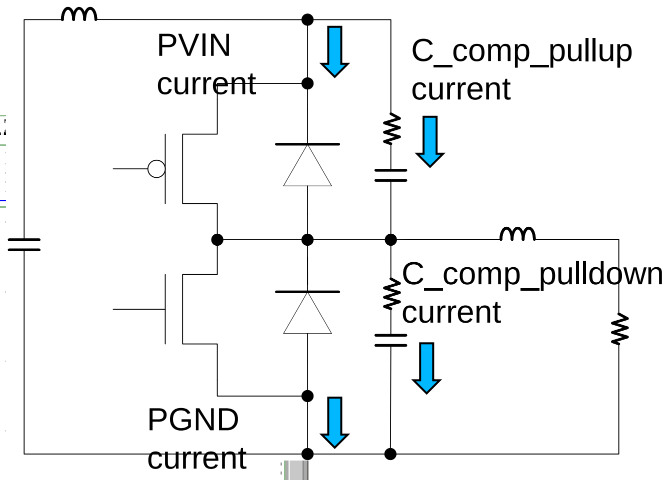


Is the dead time transition time of Waveform？

Confirm if the dead time is transition time of Waveform

Adjust transient time of Falling Waveform to the measurement





Transition time of Waveform becomes the dead time.

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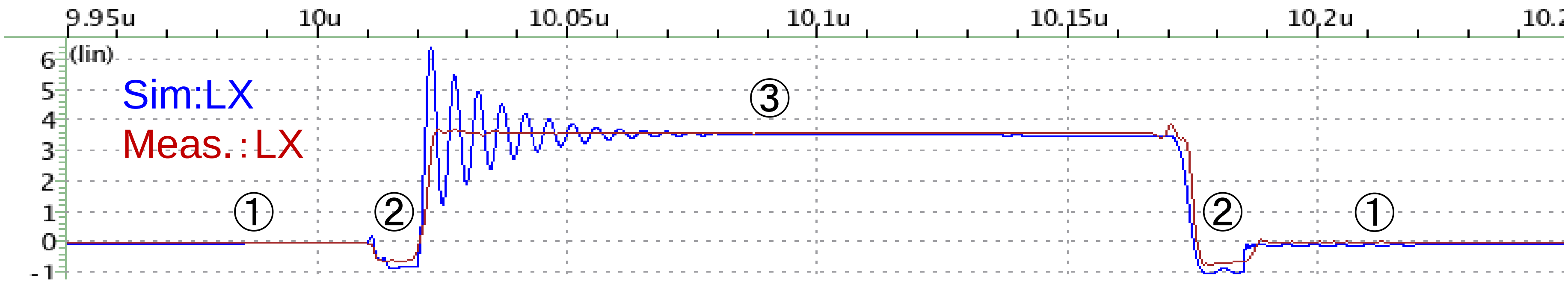
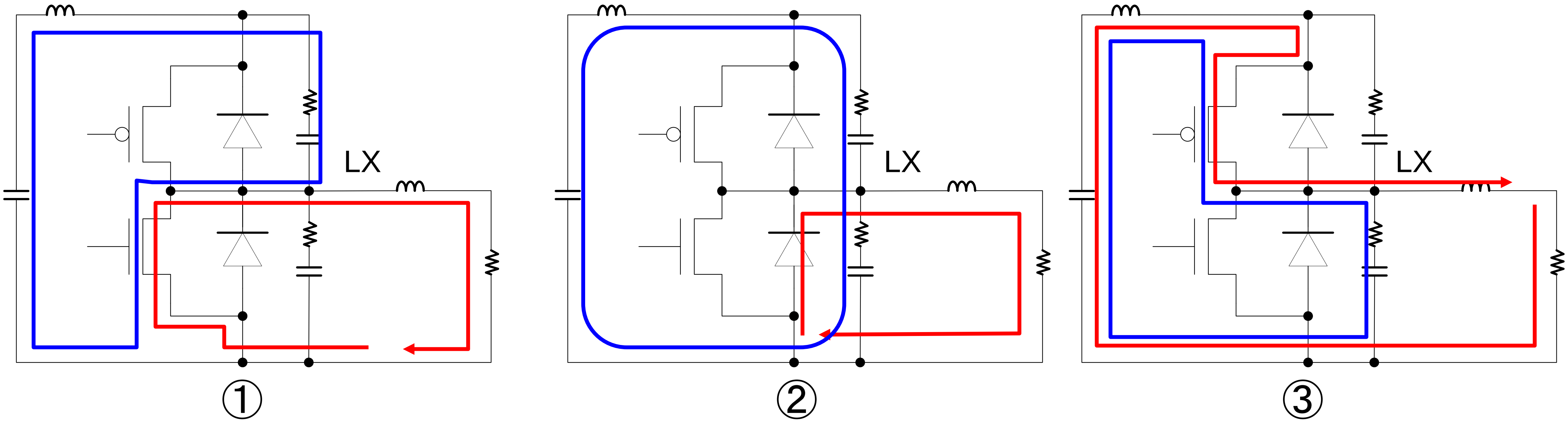
Discussion：Load current path and resonance current path

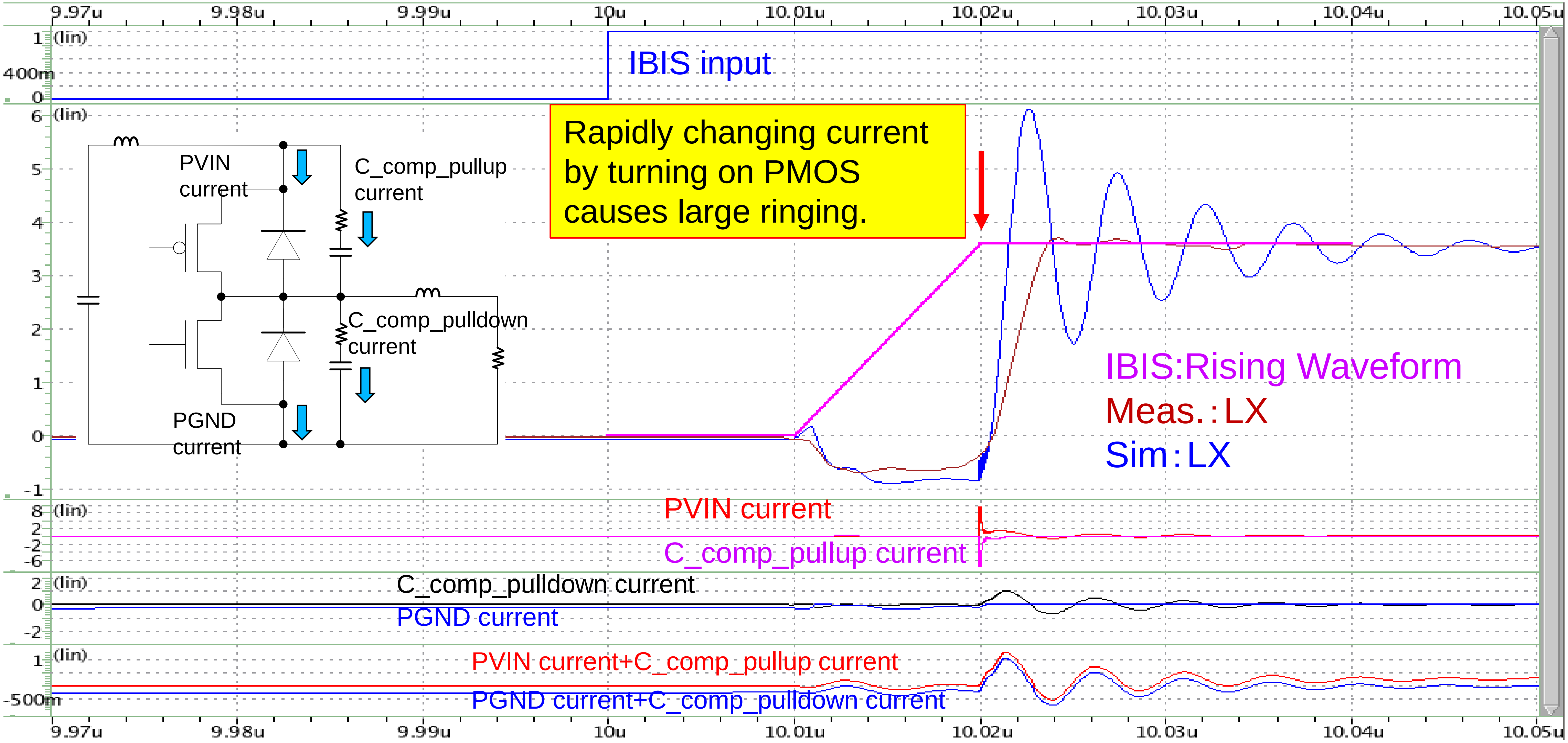


Resonance current path

Load current path



Discussion：Cause of the ringing



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Summary

- Trial to simulate CISPR25 for IBIS described DCDC
- Discrepancies from measurements in high frequency range

✓ Possible source of error in the simulation:

Large ringing induced by instantly switching MOS transistors

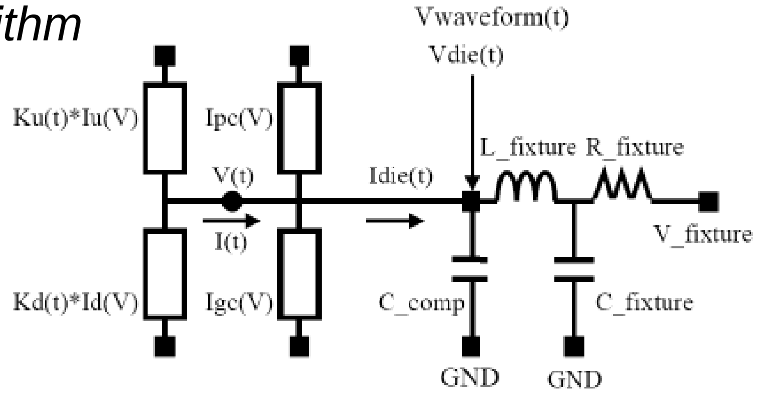
- Mitigating unrealistic transitions is considered to be a dominant solution.

Possible improvements

- Retrieve Waveform and Composite Current in IBIS by SPICE simulation adjusted the load conditions

cf.) https://ibis.org/summits/nov08a/chen.pdf

2EQ/2UK algorithm



$$0 = Ku(t) * Iu(V_{wfm1}(t)) + Ipc(V_{wfm1}(t)) - Kd(t) * Id(V_{wfm1}(t)) - Igc(V_{wfm1}(t)) - Idie(V_{wfm1}(t))$$
$$0 = Ku(t) * Iu(V_{wfm2}(t)) + Ipc(V_{wfm2}(t)) - Kd(t) * Id(V_{wfm2}(t)) - Igc(V_{wfm2}(t)) - Idie(V_{wfm2}(t))$$

- Obtain Rising/Falling Waveform and Composite Current directly from measurement