

Brief Review of PDN in IBIS

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Outline

- **Basic IBIS concepts**
- **PDN related keywords in IBIS**

- **Assume people familiar with basic IBIS content**
- **IBIS content is nearly all based on measured values (physical or SPICE simulation) and some data sheet information**
- **Simulation algorithms are not specified (with one exception)**
- **Much information already discussed during BIRD198.3 development and at JEITA 2019 workshop**



IBIS Element Classification

- [Component] (component centric) Pins
- Component [Package]*
- [Model]s* (I/O buffers including submodels)
- Information and specification content
 - Header information
 - (e.g., thresholds, Model_type, timing test load)
- Interconnect Model Set Syntax*

- * Also in SPICE models, but SPICE has availability, compatibility, speed issues



[Model] Elements

- Rails: [Voltage Range], [Pullup Reference], [Pulldown Reference], [POWER Clamp Reference], [GND Clamp Reference] and assumed GND if not overridden
- I-V tables: [Pullup], [Pulldown], [POWER Clamp], [GND Clamp]
- V-T: [Ramp], dV/dt_r , dV/dt_f
- V-T tables: [Rising Waveform], [Falling Waveform]
 - Under V_{fixture} , R_{fixture} , etc. loads
- Typ/min/max corners by PVT (process, voltage, temperature) – typ information always required



Required [Model] Subparameters

- **Model_type**
- **C_comps: typ/min/max ordered by magnitude**
 - **C_comp**
 - **And/or C_comp_pullup, C_comp_pulldown, C_comp_power_clamp, C_comp_gnd_clamp to specific rails**
- **Optional: [C Comp Corner]: typ/min/max by PVT**



21 Model_types (thru Ver. 7.0)

- **Model_type list**
 - I/O, I/O_open_drain, I/O_open_sink, I/O_open_source, I/O_ECL, I/O_diff
 - 3-state, 3-state_ECL, 3-state_diff
 - Output, Output_ECL, Output_diff
 - Open_drain, Open_sink, Open_source
 - Input, Input_ECL, Input_diff
 - Terminator
 - **Series (could be used for decoupling of rails)**
 - Series_switch



[Component] Section

Package Keywords

- [Package]
 - Subparameters R_pkg, L_pkg, C_pkg
 - Required and default
- Under [Pin], R_pin, L_pin, C_pin
 - Pin specific information overrides [Package]
- [Package Model] <name> links to advanced [Define Package Model] <name>
 - Coupled matrix format (could contain coupling to **POWER and GND rails**)
 - Coupled matrix format (could contain [Merged Pins] for **POWER and GND rails**)
 - Multi-stage uncoupled transmission line or discrete sections



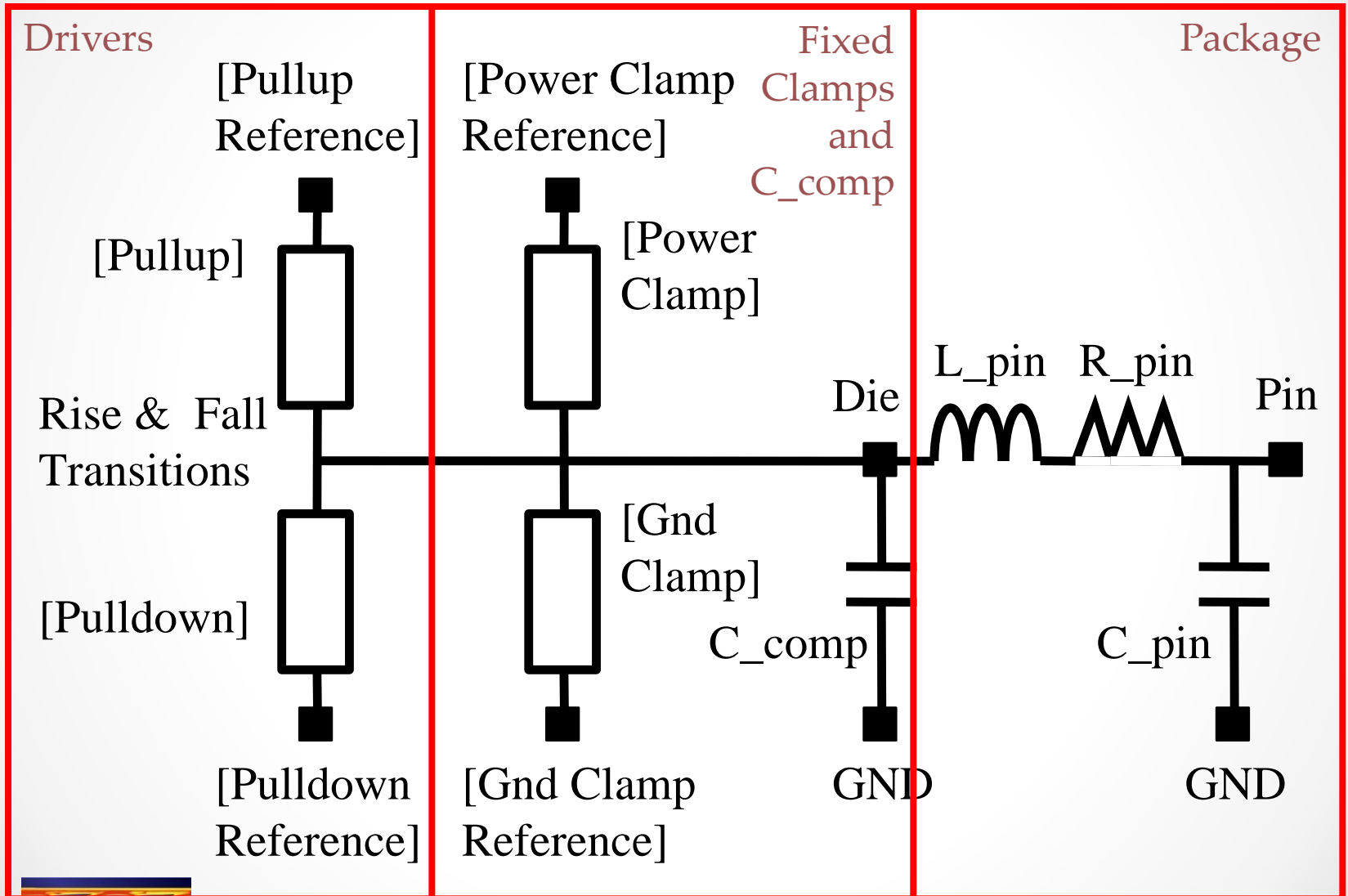
[Component] Section

Pin Keywords

- **[Pin]**
 - Required and gives pin to buffer mapping
 - Documents the pins used for rails
- **[Diff Pin]**
 - Differential buffers by single-ended construction and pin linkage
- **[Pin Mapping]** ← For PDN rail mapping to I/O buffers rail terminals using “bus_label” values
 - Maps POWER and GND “busses” to buffers for **SSN** analysis
- Plus other pin keywords not listed here

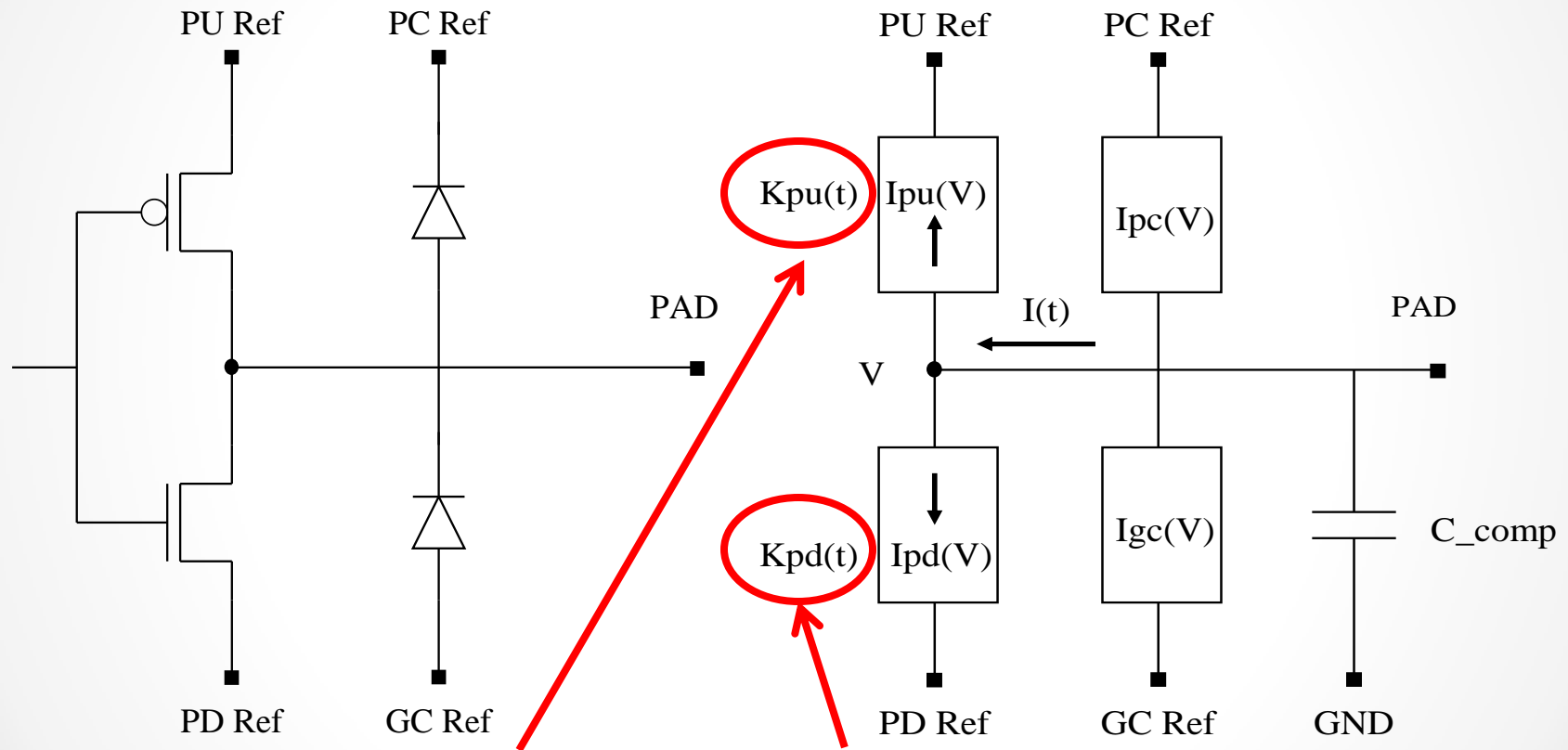


General IBIS V2.1 Buffer [Model]



Simulation: (unofficial) K-T Table

Multiplier Algorithm



$K_{pur}(t)$, $K_{puf}(t)$, $K_{pdr}(t)$, $K_{pdf}(t)$ from 2EQ/2UK (2-equations/2-unknowns) algorithm and different test loads



Gate Modulation (currents adjusted for Vgs changes) - Extraction

Assume [Voltage Range] is 1.8V (typ), 1.7V (min) and 1.95V (max).

The table voltage entries are relative to the typ/min/max of the corresponding reference voltage for each table.

[ISSO PD] | Relative to the [Pulldown Reference] voltage

Voltage	I (typ)	I (min)	I (max)
-1.8V	10.0m	7.0m	13.0m
.			
-0.5V	24.0m	18.0m	31.0m
-0.2V	27.0m	20.0m	37.0m
0.0V	25.0m	19.0m	34.0m
0.2V	18.0m	13.0m	26.0m
0.5V	10.0m	7.0m	16.0m
0.7V	5.0m	3.0m	9.0m
1.0V	1.0m	0.7m	3.0m
.			
1.8V	0.0m	0.0m	0.0m

[ISSO PU] | Relative to the [Pullup Reference] voltage)

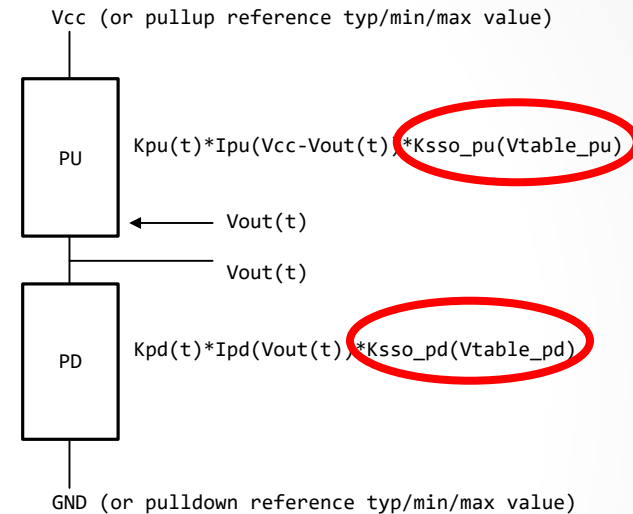
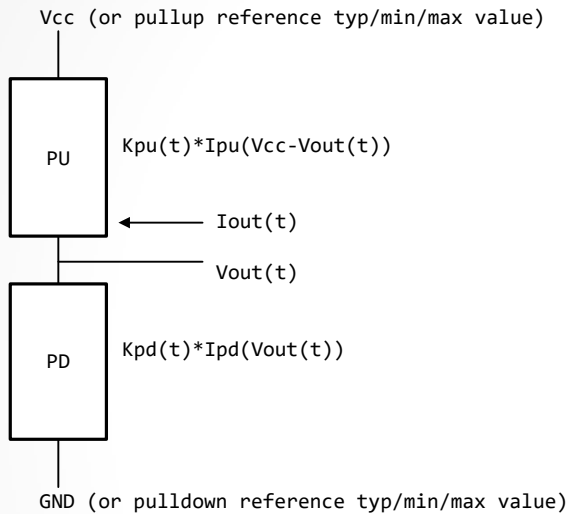
Voltage	I (typ)	I (min)	I (max)
-1.8V	-10.0m	-9.0m	-14.0m
.			
-0.6V	-28.0m	-19.0m	-40.0m
-0.4V	-31.0m	-22.0m	-43.0m
-0.2V	-29.0m	-21.0m	-40.0m
0.0V	-27.0m	-19.0m	-38.0m
0.2V	-21.0m	-14.0m	-31.0m
0.4V	-14.0m	-9.0m	-22.0m
.			
1.8V	0.0m	0.0m	0.0m

BIRD98.3 – Gate Modulation Effect (table format), A. Muranyi, A. Girardi, G. Bernardi, R. Izzi, B. Ross

**[ISSO PU]
[ISS) PD]**



Gate Modulation Simulation Model



$$K_{sso_pd}(V_{table_pd}) = I_{sso_pd}(V_{table_pd}) / I_{sso_pd}(0)$$

$$K_{sso_pu}(V_{table_pu}) = I_{sso_pu}(V_{table_pu}) / I_{sso_pu}(0)$$

$$I_{sso_pd}(0) = I_{pd}(V_{cc})$$

$$I_{sso_pu}(0) = I_{pu}(V_{cc})$$

Deriving modulation table factors for K-T table multipliers



Student Research Presented at EMC+SIPI 2020 Summit

- *Improving Power Supply Induced Jitter Simulation Accuracy for IBIS Model*, Yin Sun and Chulsoon Hwang, EMC Laboratory, Missouri University of Science and Technology
- <http://www.ibis.org/summits/aug20/sun.pdf>
- Link shows advanced proposal not in IBIS
- Accounts for pre-driver switching delays
- Further modification of Kpu and Kpd multipliers
- One slide from proposal shown next



New Behavior Model Proposal

- Modify $K_u(t)$, $K_d(t)$ as a function of **time averaged** power rail voltage $V_{cc}(t)$; introduce correction coefficient B and A as a function of **time**

$$K_u(t) = K_{u0}(t) + B_u(t) \cdot \left[\frac{\int_0^{T_{switch}} V_{cc}(t)}{T_{switch}} - V_{cc0} \right] + A_u(t) \left[\frac{\int_0^{T_{switch}} V_{cc}(t)}{T_{switch}} - V_{cc0} \right]^2$$

$$K_d(t) = K_{d0}(t) + B_d(t) \cdot \left[\frac{\int_0^{T_{switch}} V_{cc}(t)}{T_{switch}} - V_{cc0} \right] + A_d(t) \left[\frac{\int_0^{T_{switch}} V_{cc}(t)}{T_{switch}} - V_{cc0} \right]^2$$

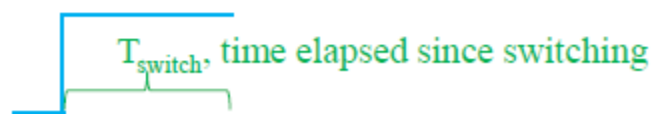
K_u , K_d under nominal V_{cc} (typical)

Linear fitting coefficient

Source:

Quadratic fitting coefficient

Averaged $V_{cc}(t)$ after the switching event happens;

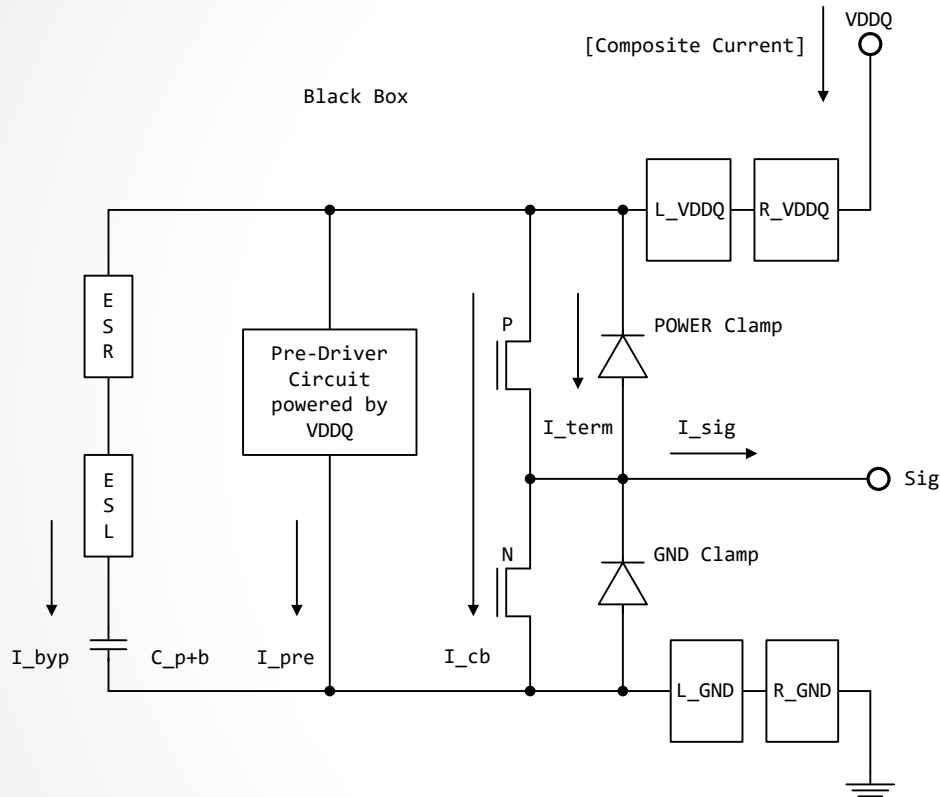


Input switching happens, time=0

Previous method on modification of K_u , K_d does not consider the time averaged effect;

Source: Behavioral modeling of jitter due to power supply noise for input/output buffers (US Patent 9842177B1)

[Composite Current]



BIRD95.6 – Power Integrity Analysis Using IBIS, S. Huq, V. Arumugham, Z. Yang, B. Ross

Buffer model output terminal currents adjusted for core currents for SSO analysis



[Composite Current] Under [Rising/Falling Waveforms]

[Rising Waveform]

R_fixture = 50.0

V_fixture = 0.0

| Rising Waveform table

[Composite Current]

Time	I (typ)	I (min)	I (max)
0	4.243E-05	NA	NA
4.00E-11	4.244E-05	NA	NA
8.00E-11	4.242E-05	NA	NA
...			
3.96E-09	2.012E-02	NA	NA
4.00E-09	2.012E-02	NA	NA

[Falling Waveform]

R_fixture = 50.0

V_fixture = 1.8

| Falling Waveform table

[Composite Current]

Time	I (typ)	I (min)	I (max)
0	4.302E-05	NA	NA
4.00E-11	4.299E-05	NA	NA
8.00E-11	4.304E-05	NA	NA
...			
3.96E-09	4.842E-05	NA	NA
4.00E-09	4.244E-05	NA	NA



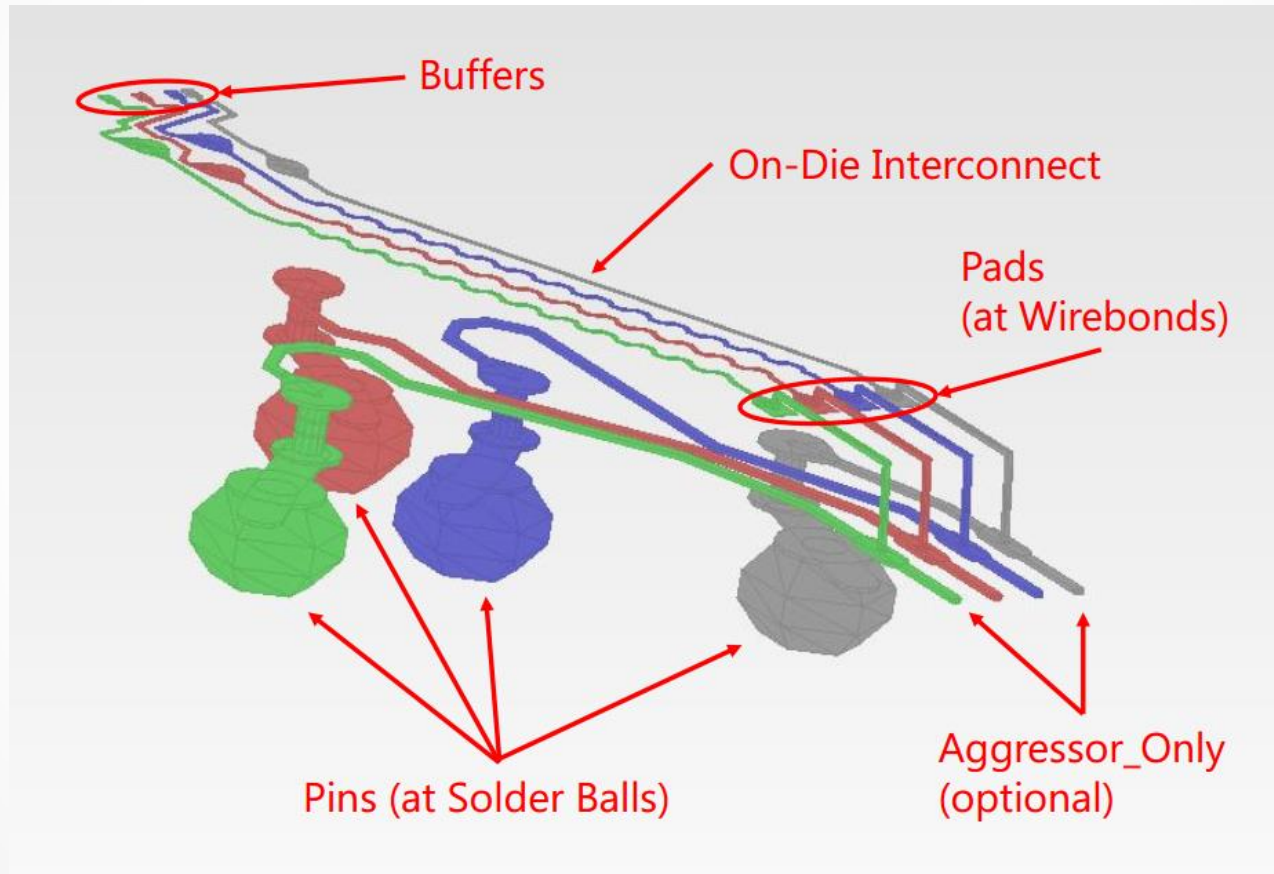
General [Interconnect Model]

- **BIRD189.7 – Interconnect Modeling Using IBIS-ISS and Touchstone, W. Katz, R. Biernacki, J. Butterfield, C. Clark, M. LaBonte, A. Muranyi, B. Ross, R. Wolff**
- **Documents buffer, die pad, and pin interfaces**
- **Electrical paths require IBIS-ISS or Touchstone**
- **Decoupling capacitors at any of the interfaces.**
- **Rail terminals can be reduced by signal_name or bus_label**
- **Uses [Pin Mapping] for rail mapping to I/O buffers**



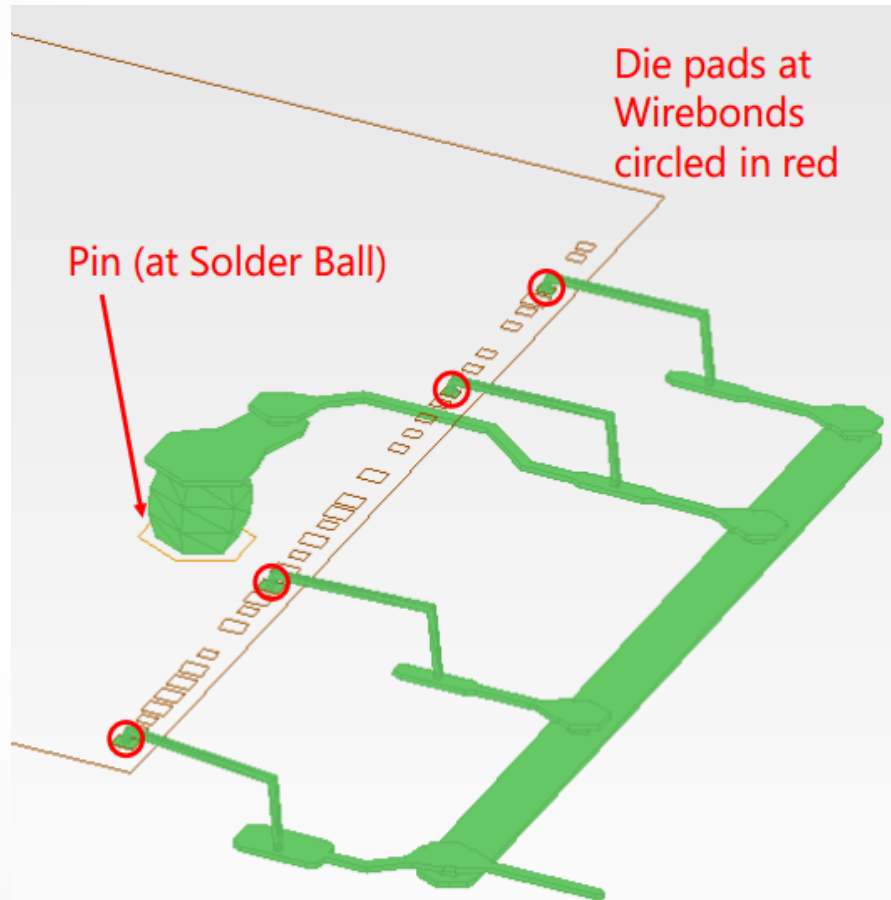
[Interconnect Model] (I/O)

Buffer, Die pad, Pin Interfaces



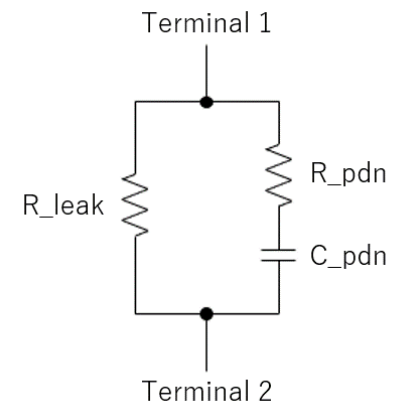
[Interconnect Model] (Rail)

Buffer, Die pad, Pin Interfaces



JEITA [PDN Model]

- BIRD 198.3 – Keyword Additions for On-Die PDN (Power Distribution Network) Modeling, K. Murata, M. Goto, K. Sakata, K. Yamada, K. Ichikawa, T. Toshiba, T. Hasegawa, K. Seko, T. Kanamoto, M. Ono
- Simple fixed topology [PDN Model] at die pad or pin interfaces and under [PDN Domain]
- [PDN Domain]s in parallel
- Terminals by Signal_name or Bus_label
- No IBIS-ISS or Touchstone files

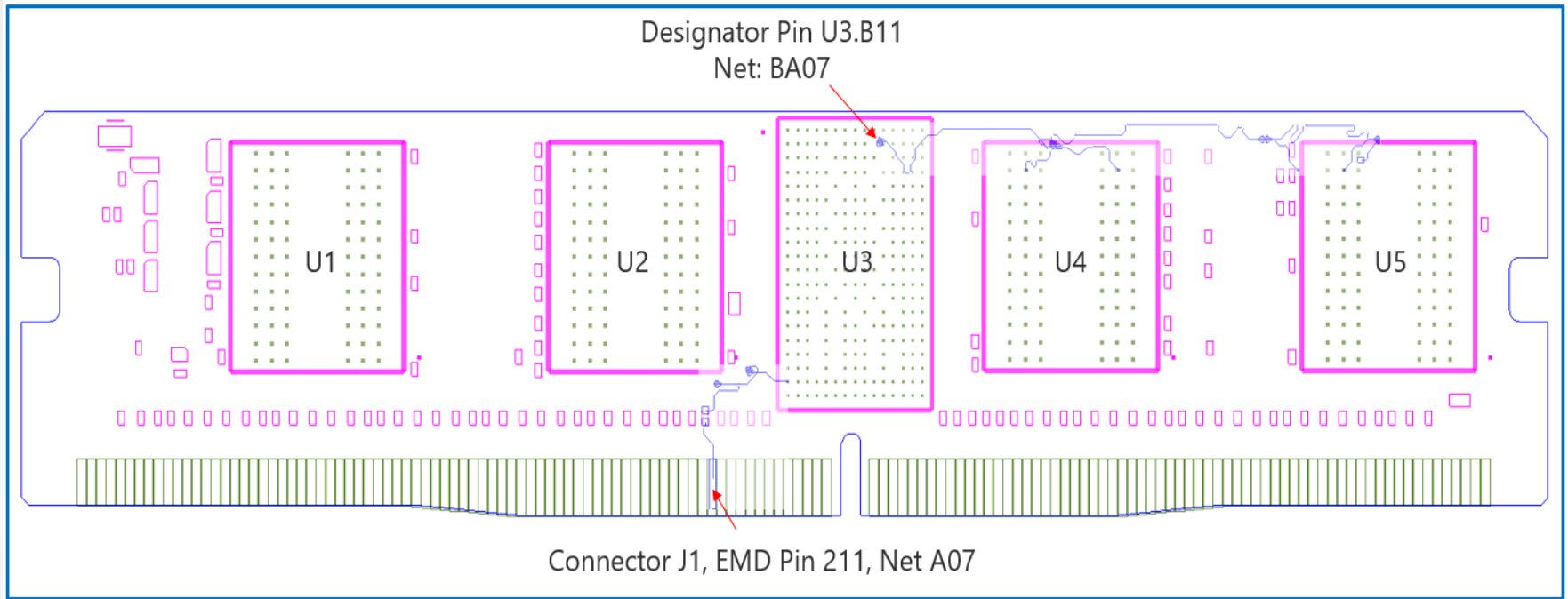


[Electrical Module Set]

- **BIRD202.x – Electrical Description of Modules, W. Katz**
- **IBIS-ISS or Touchstone electrical connections**
- **I/O pins: signal_name nets, pin_name terminals**
- **Rails: pin_name, bus_label or signal_name terminals**
- **Can be used for boards attached to (IBIS) [Components] or to (EMD) [Define Module]s**
- **For modules or stacked dies**
- **Under development for IBIS Version 7.1**



[Electrical Module]



Summary of PDN in IBIS

- Package models [Package] [Pin], [Package Model]
- [Pin Mapping] for mapping rails to I/O buffers
- [Define Package Model] for coupled paths including possible decoupling paths between rails
- Gate Modulation effects from [ISSO PU], [ISSO PD]
- [Composite Current] for output currents adjusted for buffer core currents
- JEITA [PDN Model] under [PDN Domain] for simple decoupling
- [Interconnect Model] with IBIS-ISS and Touchstone
- Electrical Module Description – module paths

