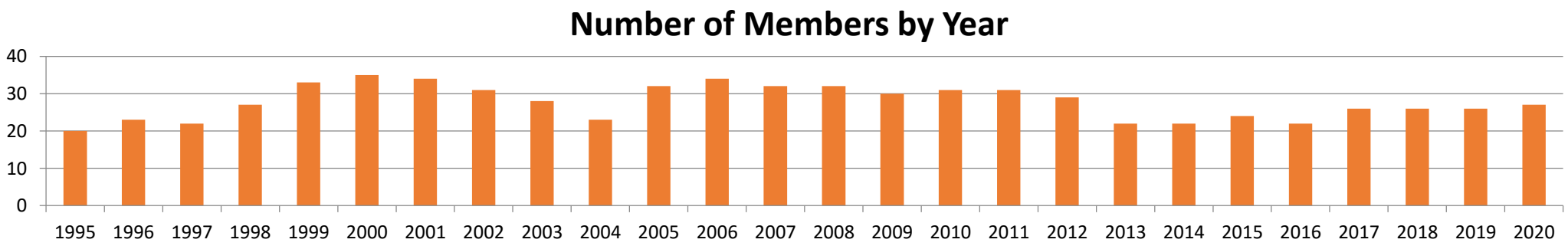
IBIS Chair's Report

Randy Wolff
Micron Technology
Chair, IBIS Open Forum

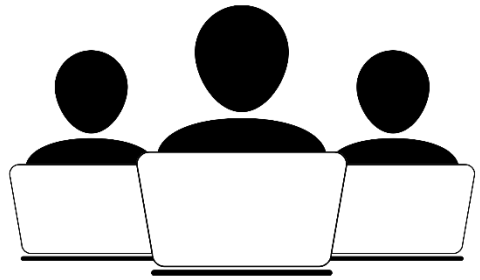
2020 Virtual Asian IBIS Summit – Japan
November 13, 2020

27 IBIS Members (Organization-based)



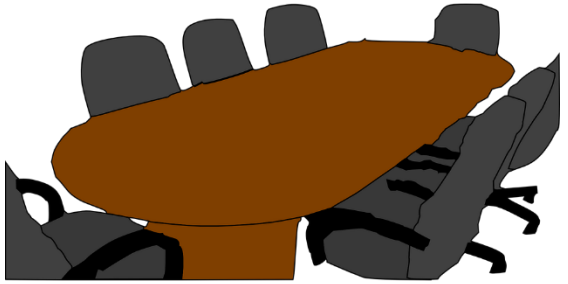
IBIS Officers 2020-2021

Chair:	*Randy Wolff, Micron Technology*
Vice-Chair:	*Lance Wang, Zuken USA*
Secretary:	*Curtis Clark, ANSYS*
Treasurer:	*Bob Ross, Teraspeed Labs*
Librarian:	*Zhiping Yang, Google**
Postmaster:	*Mike LaBonte, SiSoft (MathWorks)*
Webmaster:	*Steve Parker, Marvell*



* Temporary appointment with election in process to replace Anders Ekholm after resignation on October 6.

IBIS Meetings



- Weekly teleconferences
  - Quality task group (Tuesdays, 08:00 PT)
  - Advanced Technology Modeling (ATM) task group (Tuesdays, 12:00 PT)
  - Interconnect task group (Wednesdays, 08:00 PT)
  - Editorial task group (some Fridays, 08:00 PT)
- IBIS Open Forum teleconference every 3 weeks (Fridays, 08:00 PT)
- IBIS Summit meetings (USA and international)
  - DesignCon, IEEE SPI, Shanghai, Taipei, Tokyo (JEITA-organized)
  - IEEE EMC+SIPI (new for 2020)
- Participants: 368 in 2019

SAE ITC

- SAE Industry Technologies Consortia is the parent organization of the IBIS Open Forum
- IBIS is assisted by SAE employees José Godoy, Phyllis Gross, Laurie Strom
- SAE ITC provides financial, legal, and other services
- https://www.sae-itc.com/

Task Groups

- Interconnect Task Group
  - Chair: Michael Mirmak, Intel
  - https://ibis.org/interconn_wip/
  - Develop on-die/package/module/connector interconnect modeling BIRDs
- Advanced Technology Modeling Task Group
  - Chair: Arpad Muranyi, Mentor, A Siemens Business
  - https://ibis.org/atm_wip/
  - Develop most other technical BIRDs
- Quality Task Group
  - Chair: Mike LaBonte, SiSoft (MathWorks)
  - https://ibis.org/quality_wip/
  - Oversee IBISCHK parser testing and development
- Editorial Task Group
  - Chair: Michael Mirmak, Intel
  - https://ibis.org/editorial_wip/
  - Produce IBIS Specification documents

BIRD = Buffer Issue Resolution Document

IBIS Milestones

I/O Buffer Information Specification

- 1993-1994 **IBIS 1.0-2.1**:
  - Behavioral buffer model (fast simulation)
  - Component pin map (easy EDA import)
- 1997-1999 **IBIS 3.0-3.2**:
  - Package models
  - Electrical Board Description (EBD)
- 2002-2006 **IBIS 4.0-4.2**:
  - Receiver models
  - AMS languages
- 2007-2012 **IBIS 5.0-5.1**:
  - IBIS-AMI SerDes models
  - Power-aware models
- 2013-2015 **IBIS 6.0-6.1**:
  - PAM4 multi-level signaling
  - Power delivery package models
- 2019 **IBIS 7.0**:
  - Back-channel support
  - Interconnect modeling using IBIS-ISS and Touchstone
- 2020-2021 **IBIS 7.1 (in progress)**
  - DDRx IBIS-AMI support

Other Work

- 1995: **ANSI/EIA-656 (International standard)**
  - IBIS 2.1
- 1999: **ANSI/EIA-656-A (International standard)**
  - IBIS 3.2
- 2001: **IEC 62014-1 (International standard)**
  - IBIS 3.2
- 2003: **ICM 1.0**
  - Interconnect Model Specification
- 2006: **ANSI/EIA-656-B (International standard)**
  - IBIS 4.2
- 2009: **Touchstone 2.0**
  - Official Touchstone donated from Agilent/Keysight
- 2011: **IBIS-ISS 1.0**
  - Interconnect SPICE Subcircuit specification (subset of HSPICE)
- **IBISCHK**: IBIS file syntax parser
  - Current version 7.0.2
  - Source code available for purchase
  - Compiled executables available free of charge

Planning for IBIS Version 7.1

BIRDs approved for 7.1

BIRD ID	BIRD Title	Approval Date
195.1	Enabling [Rgnd] and [Rpower] Keywords for Input Models	August 31, 2018
197.7	New AMI Reserved Parameter DC_Offset	February 21, 2020
198.3	Keyword Additions for On-Die PDN (Power Distribution Network) Modeling	August 7, 2020
199	Fix Rx_Receiver_Sensitivity Inconsistencies	June 7, 2019
200	C_comp Model Using IBIS-ISS or Touchstone	September 27, 2019
201.1	Back-channel Statistical Optimization	July 17, 2020
203	Submodel Clarification	April 24, 2020
204	DQ_DQS GetWave Flow for Clock Forwarding Modeling	June 26, 2020
205	New AMI Reserved Parameter for Sampling Position in AMI_Init Flow	June 26, 2020
206	Clarification of text "transition time"	September 18, 2020
207	New AMI Reserved Parameters Component_Name and Signal_Name	October 9, 2020

BIRDs expected to be approved

BIRD ID	BIRD Title	Tentative Vote Date
202	Electrical Descriptions of Modules	December 2020
208	Clock-Data Pin Relationship Keyword	November 2020

What's Next for IBIS?

- IBIS has traditionally focused on I/O buffers and interconnect, for:
  - Solving signal integrity issues from channel loss, inter-symbol interference (ISI), and crosstalk
  - Generating waveforms or eye diagrams for timing or bit-error-rate analysis
- IBIS must continue to evolve to meet both the SI and PI demands of new signaling technologies
  - System-level perspective
    - Clock/data relationships, timing information, equalization training
  - Power Distribution Network (PDN) is a critical piece of overall system design
  - Potential for IBIS to enable improved modeling/analysis of PDN
    - Voltage regulator models
    - Chip power models

Submitting Your Idea – BIRD Process

- BIRD – Buffer Issue Resolution Document
  - Official method for submitting a proposed change to the IBIS specification
- BIRD template found on IBIS website
  - Standardizes method to describe your idea
- Submit BIRD to chair@ibis.org
- BIRDs discussed in Open Forum meetings
  - Eventual vote by members for approval
- Idea not ready for an official BIRD?
  - Join an IBIS Task Group meeting for technical discussion

BIRD Link on IBIS Website

Link to BIRDs webpage

BIRD Template Link on the BIRD Webpage

Buffer Issue Resolution Documents (BIRD)

To submit a BIRD to the IBIS Open Forum, please use the BIRD Template, Rev. 1.3.

ID#	Issue Title	Requester	Date Submitted	Date Accepted	Supporting Version
208	Clock-Data Pin Relationship Keyword	Michael Mirmak, Intel Corp.	October 6, 2020		
207	New AMI Reserved Parameters Component_Name and Signal_Name	Randy Wolff, Micron Technology	July 29, 2020	October 9, 2020	
206	Clarification of text "transition time"	Hansel Desmond Dsilva, Achronix Semiconductor; Walter Katz, Signal Integrity Software; Fangyi Rao, Keysight; Todd Bermensolo, Keysight; Arpad Muranyi, Mentor Graphics.	June 26, 2020	September 18, 2020	
205	New AMI Reserved Parameter for Sampling Position in AMI_Init Flow	Hansel Desmond Dsilva, Achronix Semiconductor; Walter Katz, Signal Integrity Software; Todd Bermensolo, Keysight; Fangyi Rao, Keysight; Arpad Muranyi; Mentor Graphics; Ambrish Varma, Cadence	May 14, 2020	June 26, 2020	
204	DQ_DQS GetWave Flow for Clock Forwarding Modeling	Walter Katz, The MathWorks Fangyi Rao, Keysight Wendem Beyene, Intel Ambrish Varma, Cadence	April 22, 2020	June 26, 2020	
203	Submodel Clarification	Randy Wolff, Micron Technology	March 10, 2020	April 24, 2020	
202	Electrical Descriptions of Modules	Walter Katz, Signal Integrity Software	January 22, 2020		
201.1	Back-channel Statistical Optimization	Walter Katz, Signal Integrity Software	January 7, 2020, June 2, 2020	July 17, 2020	
200	C_comp Model Using IBIS-ISS or Touchstone	Randy Wolff, Micron Technology, Inc. Walter Katz, Signal Integrity Software, Inc.	July 9, 2019	September 27, 2019	
199	Fix Rx_Receiver_Sensitivity Inconsistencies	Arpad Muranyi, Mentor a Siemens Business	March 19, 2019	June 7, 2019	
198.3	Keyword Additions for On-Die PDN (Power Distribution Network) Modeling	Kazuki Murata; Sony LSI Design Inc.; Miyoko Goto; Ricoh Co., Ltd.; Kazuyuki Sakata; Renesas Electronics Corporation; Kazunori Yamada; Renesas Electronics Corporation; Kouji Ichikawa; Denso Corporation; Atsushi Tomishima; Toshiba Electronic Devices & Storage Corporation; Takashi Hasegawa; Sony LSI Design Inc.; Koichi Seko, Panasonic Industrial Devices Systems and Technology Co., Ltd.; Toshiki Kanamoto; Hirosaki University Megumi Ono; Socionext Inc.	March 11, 2019, April 3, 2020, June 23, 2020, August 7, 2020	August 7, 2020	

[Thank You]

IBIS Open Forum:
Web: https://www.ibis.org
Email: info@ibis.org

We welcome participation by all IBIS model makers, EDA tool vendors, IBIS model users, and interested parties.