Comprehensive Multilingual Modeling of CPHY Trio
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Agenda

- Motivations
- Technical challenges
- Preferred modeling solution
- IBIS vs. SPICE circuit correlation
- Conclusions
Motivations

- In order to ensure complete CPHY link’s SI performance, SI simulations for entire system (Tx/Rx PHY + package + PCB) are mandatory from end user point of view
- Demand for a CPHY Trio modeling is high
- A universal CPHY modeling solution that would be applied in various EDA tool will be beneficial
- IBIS model is a great candidate for CPHY Tx trio modeling
  - Widely used in industry
  - Accepted by different EDA tools
  - Fairly simple test bench setup
- Goal: create IBIS buffer based solution for complete CPHY link SI simulation
Technical challenges

- CPHY possesses unique Trio signaling scheme (picture c and d) [1], which is not explicitly supported in latest IBIS specification
  - EDA tools are not mandated to be able to feed the CPHY 3-level data pattern to TX model
  - Model generator also needs to take care of 3-level data pattern generation

- CPHY Trio also transmit data according to a FSM (finite-state-machine) with specific mapping
  - Control logic required and capable of interfacing with D/A signals
  - Verilog-A is broadly accepted in the industry, and can be used to realize the state-transition described in FSM

- Transition timing on a single wire (A, B or C) shall also be carefully calibrated in the model
  - No “glitches” or “prolonged propagation” at transitions

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Preferred Model Solution

- The complete CPHY bundled solution includes
  - Three tri-state IBIS buffers per lane (A, B or C) capture three state-transition scenarios
    - 0.5V ↔ 0.75V
    - 0.5V ↔ 0.25V
    - 0.25V ↔ 0.75V
  - Verilog-A module to
    - Realize FSM on the right [2]
    - Control IBIS buffers Enable and Data
  - Input clock signal defines symbol rate (e.g. 3.5GSps)

Preferred Model Solution - Illustration

- Picture illustration of single lane of the trio (A, B or C)

CPHY Trio Bundled Model

Verilog-A Control

Data Stream 010101...

IBIS model array

0.5V ↔ 0.75V
0.25V ↔ 0.75V
0.25V ↔ 0.5V

A, B or C

Tx-line

Zload

IBIS model array
IBIS vs. SPICE Circuit Correlation

- Correlation Simulation Topology
- Transient waveform correlation (typical, slow, fast)
Correlation Simulation Topology

- Simulation symbol rate: 3.5GSps
- Transient waveform at Line A of the Trio is probed
Transient Waveform Correlation (Typical)

- IBIS (blue) vs. SPICE circuit (red)
- Package, PCB, Tx/Rx models all included
Transient Waveform Correlation (Slow)

- IBIS (blue) vs. SPICE circuit (red)
- Package, PCB, Tx/Rx models all included
Transient Waveform Correlation (Fast)

- IBIS (blue) vs. SPICE circuit (red)
- Package, PCB, Tx/Rx models all included
Conclusions

• Adopt a CPHY Trio bundle model consisting of tri-state IBIS buffers and Verilog-A control (right top picture)

• Solution is based on currently existing, widely applied common technologies (tri-state IBIS, Verilog-A)

• Use the CPHY Trio model to perform channelSignal Integrity verifications (right bottom picture)

• Proposed bundled solution achieved great correlation with SPICE simulation