Think Bigger.
Reach Further.

Celestica 112G SI Study for 800G Switch

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Agenda

- PCB Material Study
- 112G Via and Pad Structure Optimization
- 112G C2M, VSR and CR Channel Simulation
- Conclusion

Abbreviations:
C2M: Chip to Module
VSR: Very Short Reach interface
CR: Cable assembly Reach interface
HS: High Speed
SW: Switch
QDD: QSFP-DD : Quad Small Form Factor Double Density
DAC: Direct Attach Copper cable

PCB Material Study

PCB Material SI Correlation Method

Measurement results:

layer	design	measured
L21	0.63	0.63
Prepreg	5.71	5.63
L22	0.63	0.63
Core	5.98	5.91
L23	0.63	0.67
Layer	**Line width**	**spacing**
95ohm Design	6.5	8.5
Measured		
L22 2" trace	7.0	8.0
L22 5" trace	6.7	8.4
L22 10" trace	6.9	8.2

L22

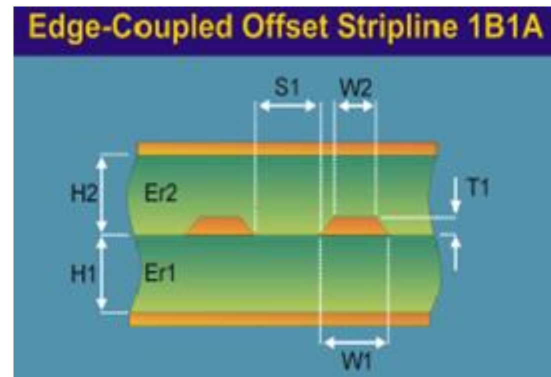
Impedance

Test layer	2 inches	5 inches	10 inches
L22	91.4	91.2	90.7
	91.1	91.4	91.0
	90.5	91.0	90.8
	90.3	90.2	90.3
	90.5	90.8	90.4
Min	90.3	90.2	90.3
Max	91.4	91.4	91.0
Avg	90.76	90.92	90.64

Insertion loss1

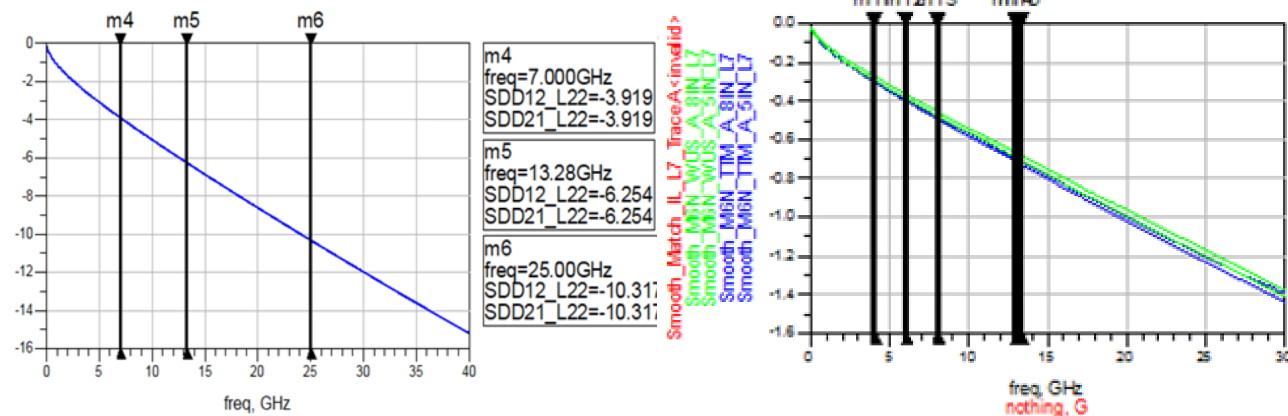
Test layer	5 inches vs 2 inches (dB / inches)		
	7GHz	13.28GHz	25GHz
L22	0.360	0.606	1.024
	0.415	0.663	1.089
	0.415	0.662	1.077
	0.375	0.619	1.032
	0.376	0.623	1.037
Min	0.360	0.606	1.024
Max	0.415	0.663	1.089
Avg	0.3882	0.6346	1.0518

Simulation correlation results:



LW/SP AVG	Impedance AVG
6.9/8.2	90.77

L21	0.63
PP	5.63
L22	0.63
Core	5.91
L23	0.67

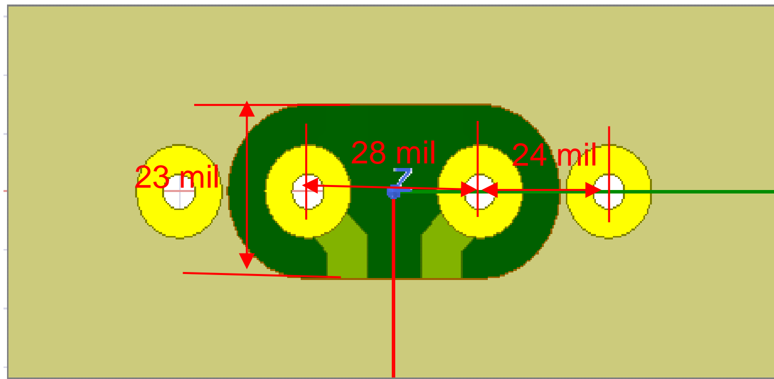


DK@10GHz	Stripline: Core/Prepreg for Fitting	Stripline Df@10GHz	Roughness
3.28	CORE:0.152mm core (2x1078) PP:2 x #1078 RC67%	0.0041	0.25um
3.28	CORE:0.152mm core (2x1078) PP:2 x #1078 RC67%	0.0041	0.25um

112G Via and Pad Structure Optimization

Via Structure Optimization

Via structure example:



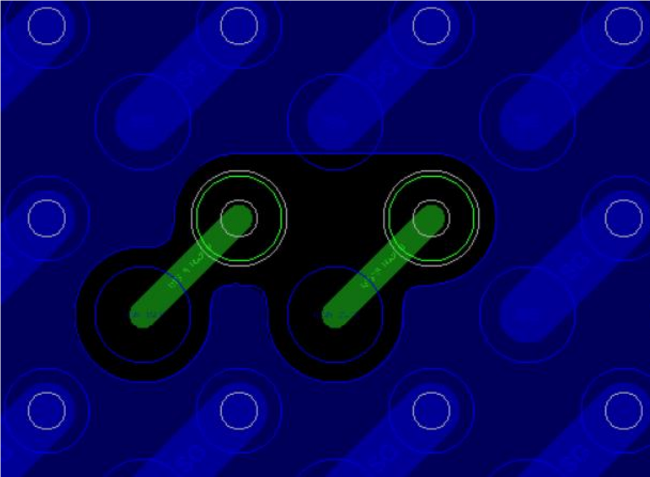
Anti-pad sweep example:

Fanout layer	Anti-Pad (mil)	Impedance (Rise time 12.5ps)	RL@26.56GHZ	IL@26.56GHZ
L03 to L18	23	Min:82.3 ; Max:100.7	-8.91dB	-0.93dB
	24	Min:85.68 ; Max:100.23	-9.16dB	-0.93dB
	25	Min:86.64 ; Max:100.78	-9.71dB	-0.89dB
	26	Min:86.47 ; Max:100.71	-9.89dB	-0.82dB
	27	Min:86.24 ; Max:100.99	-10.33dB	-0.80dB
	28	Min:86.39 ; Max:100.65	-10.53dB	-0.75dB
	29	Min:85.32 ; Max:100.58	-10.81dB	-0.73dB
	30	Min:86.41 ; Max:100.53	-11.11dB	-0.70dB
	31	Min:86.66 ; Max:100.88	-11.60dB	-0.67dB
	32	Min:86.77 ; Max:100.53	-11.62dB	-0.63dB

- The example via stub: 10mils. It based on current via stub tolerance 6+/-4mils. If PCB vendor could make the tolerance to 4+/-2mils. The max via stub will be 6mils. That would be helpful for 112G via SI performance.
- Via IL and RL will impact SI performance very much if we don't optimize the via structure thoroughly.
- Lower target impedance of the via may have better SI performance.

BGA area Pad/Via Structure Optimization

BGA area Pad/Via structure example:



Anti-pad sweep example:

Fanout layer	Anti-Pad (mil)	Impedance (Rise time 12.5ps)	RL@26.56GHZ	IL@26.56GHZ
L03 to L24	23	Min:83.1; Max:102.0	-10.74dB	-0.85dB
	24	Min:84.0; Max:96.2	-13.47dB	-0.67dB
	25	Min:83.6; Max:96.4	-13.52dB	-0.66dB
	26	Min:85.2; Max:96.7	-13.74dB	-0.64dB
	27	Min:85.6; Max:98.4	-13.80dB	-0.63dB
	28	Min:85.9; Max:96.9	-14.99dB	-0.59dB
	29	Min:85.6; Max:96.8	-14.67dB	-0.61dB
	30	Min:86.9; Max:97.1	-15.82dB	-0.58dB

- At BGA area, via to via and via to solder pad spacing has limitations. It’s not easy to change HS via to HS/GND via spacing to get a better via barrel impedance.
- In top layer, solder pad and via pad have very low impedance. How to optimize them is big problem.
- Use via in pad for all vias at the BGA area may have better SI performance.

112G C2M, VSR and CR Channel Simulation

802.3ck C2M Host Channel

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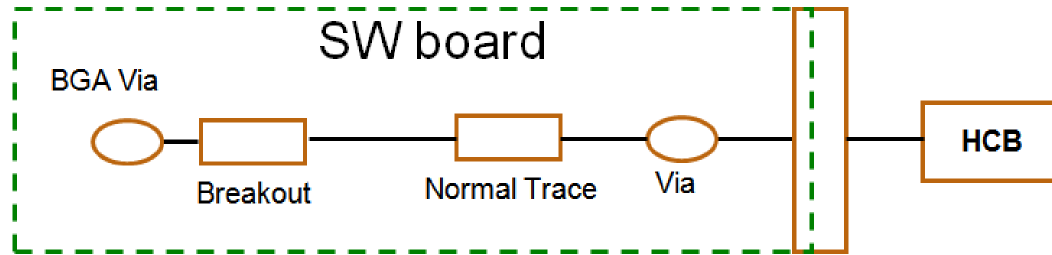


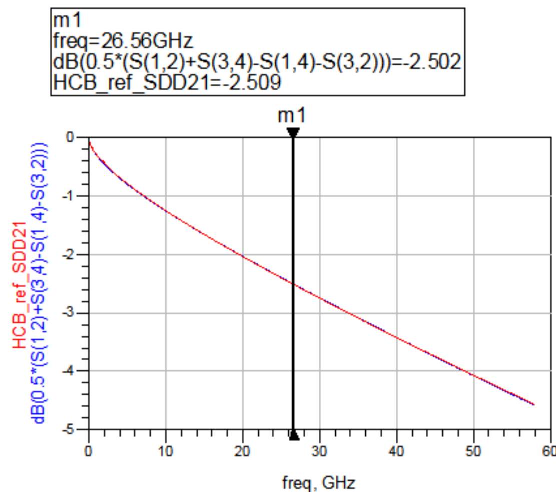
Host board PCB is 28 Layers, total 4.5mm thickness, Megtron-7 level material.

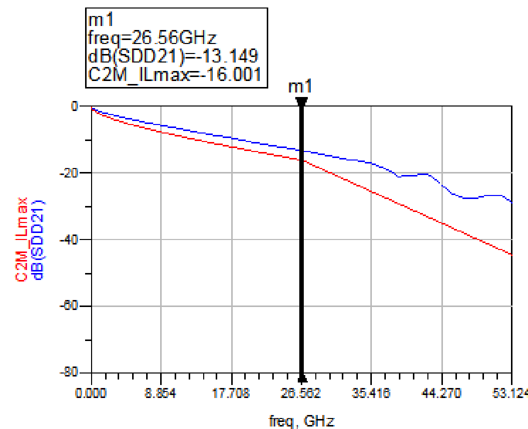
Host trace width/spacing is 7.8mil/12.5mil, total 10inches trace included 0.8inch neck-down(5.2mil/3mil).

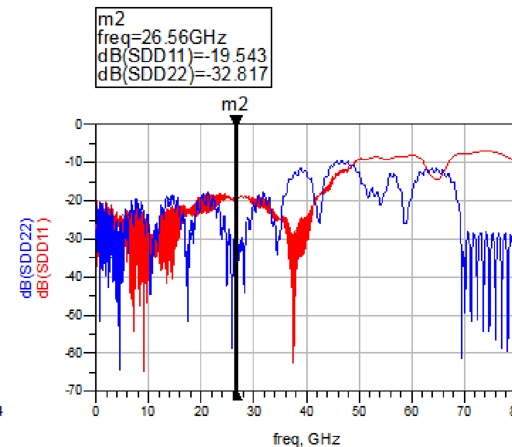
Vias stub modeled as 6mils, long via length, bandwidth up to 80GHz.

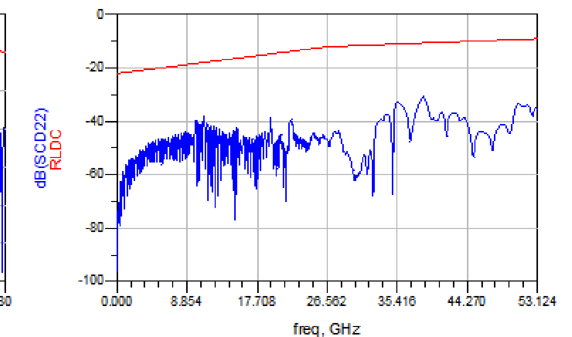
Referred to 802.3_3ck, C2M host channel insertion loss budget is 16dB@26.56GHz.

HCB (Host compliance board) modeled using simulation tools, about 2.5dB@26.56GHz.

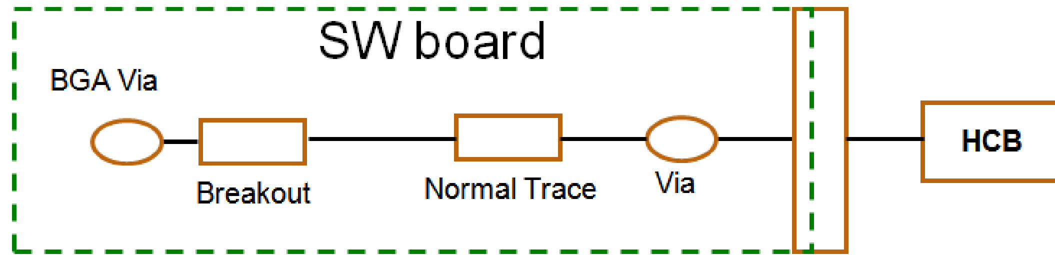








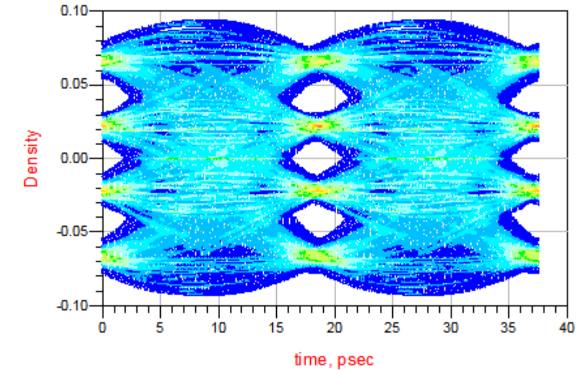
CEI-112G-VSR-PAM4 Host Channel



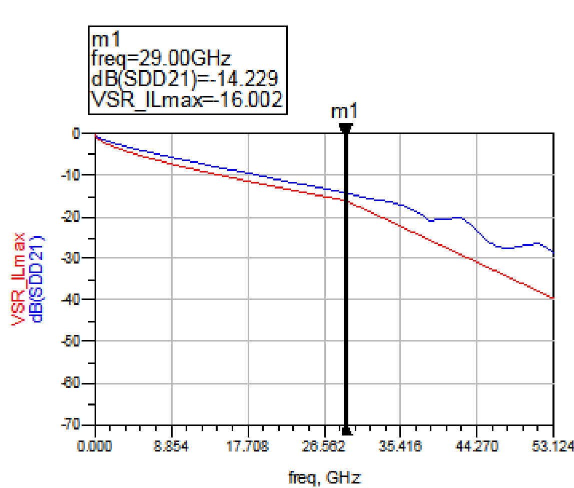
The same PCB related info as C2M channel. Total 10 inches PCB trace.

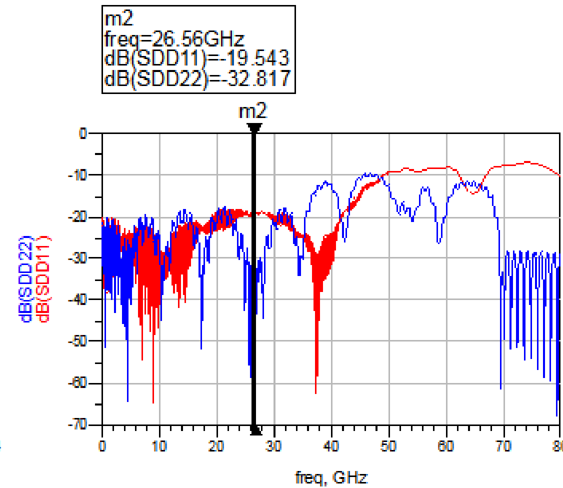
Referred to CEI-112G-VSR-PAM4 Draft, channel insertion loss budget is 16dB@29GHz.

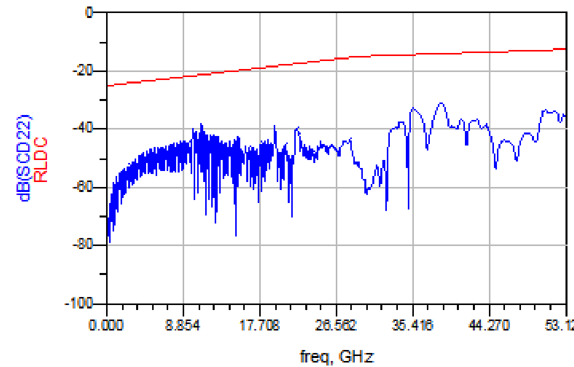
Eye diagram simulation used IBIS AMI model, RX side used CTLE, DFE not used.

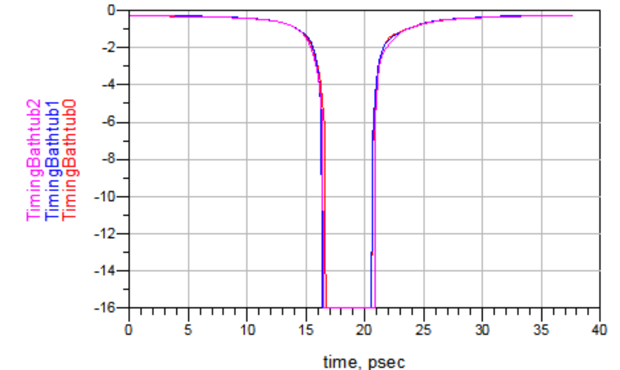


measurement	Summary
WidthAtBER0	4.612E-12
WidthAtBER1	4.424E-12
WidthAtBER2	4.894E-12
HeightAtBER0	0.023
HeightAtBER1	0.024
HeightAtBER2	0.023
Tmid	1.854E-11
Vlow	0.022
Vmid	0.023
Vupp	0.022
Hlow	4.047E-12
Hmid	4.424E-12
Hupp	4.424E-12
AVlow	0.044
AVmid	0.043
AVupp	0.044
CrossingLevel0	-0.039









802.3ck 100GBASE-CR Channel

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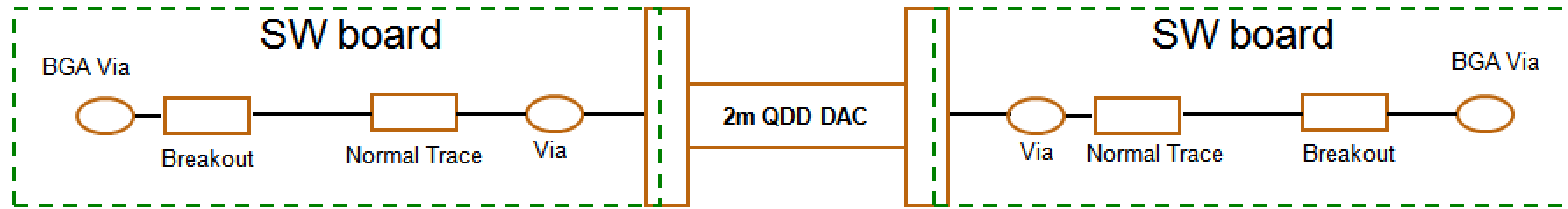
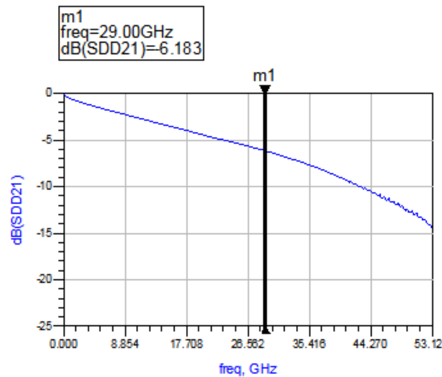


The same PCB related info as C2M channel. Total 5 inches PCB trace in one SW board.

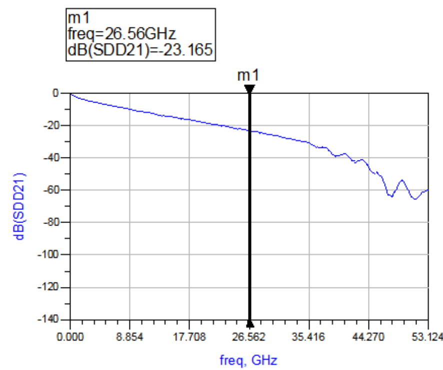
From BGA ball to DAC connector the IL spec is 6.875dB@26.56GHz.

Referred to 802.3_3ck, C2M host channel insertion loss budget is 28.5dB@26.56GHz.

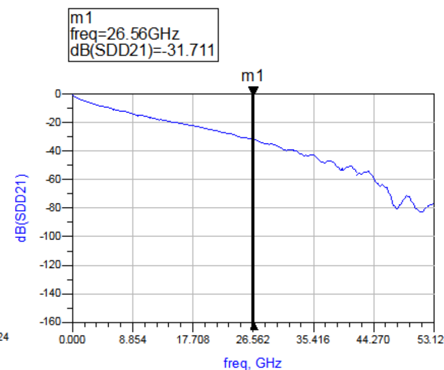
Eye diagram simulation used IBIS AMI model with switch PKG model.



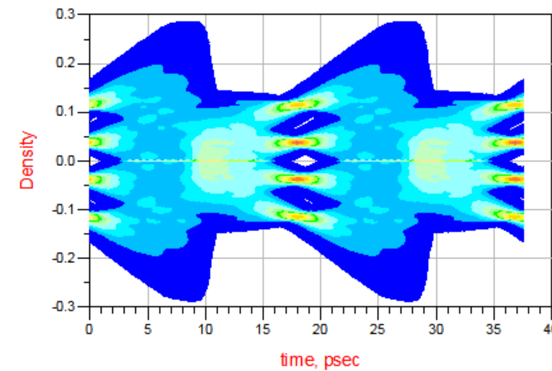
Pure one PCB loss

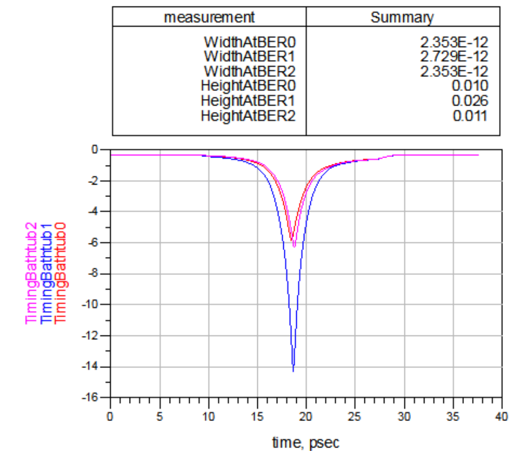


Without IC PKG



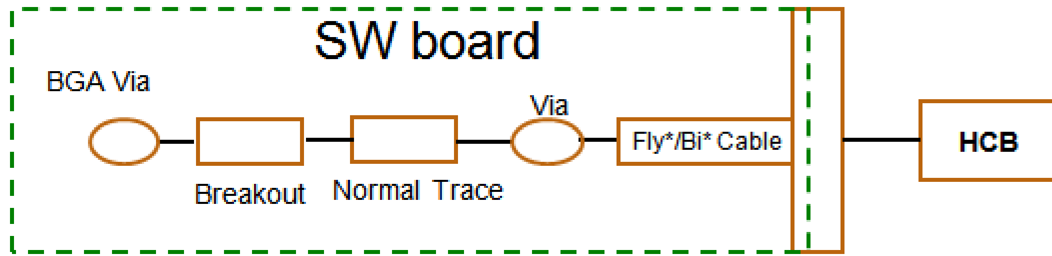
With IC PKG





measurement	Summary
WidthAtBER0	2.353E-12
WidthAtBER1	2.729E-12
WidthAtBER2	2.353E-12
HeightAtBER0	0.010
HeightAtBER1	0.026
HeightAtBER2	0.011

802.3ck C2M Host Channel With Fly*/Bi* Cable



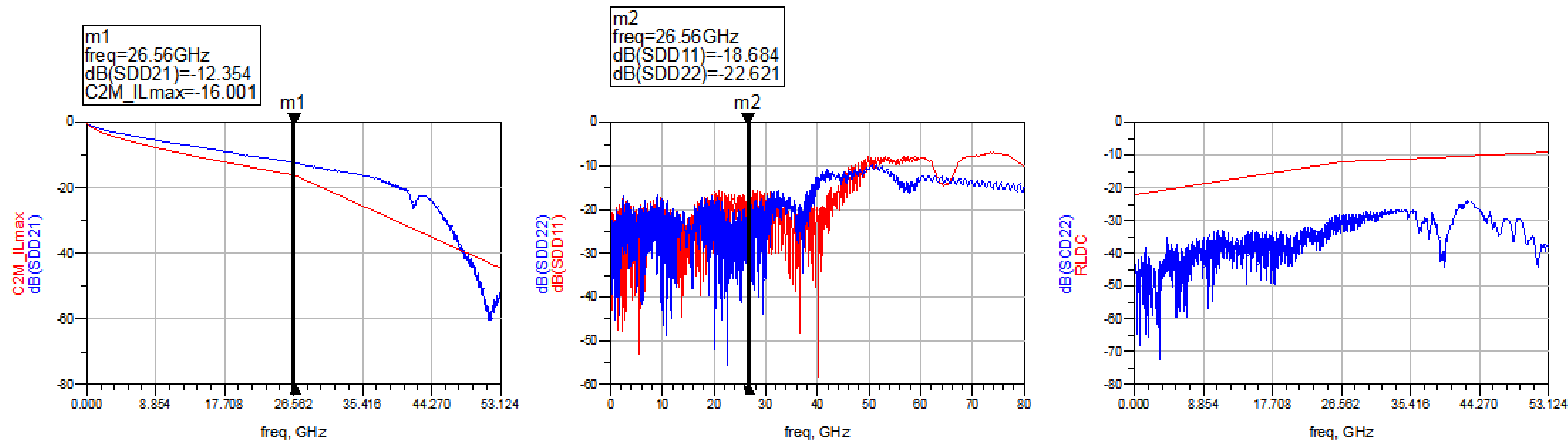
Host board PCB is 28 Layers, total 4.5mm thickness, M7 level material.

Host trace width/spacing is 7.8mil/12.5mil, total 5inches trace included 0.8inch neck-down(5.2mil/3mil).

Vias stub modeled as 6mils, long via length, bandwidth up to 80GHz.

Referred to 802.3_3ck, C2M host channel insertion loss budget is 16dB@26.56GHz.

HCB (Host compliance board) modeled using simulation tools, about 2.5dB@26.56GHz.



CEI-112G-VSR-PAM4 Host Channel With Fly*/Bi* Cable

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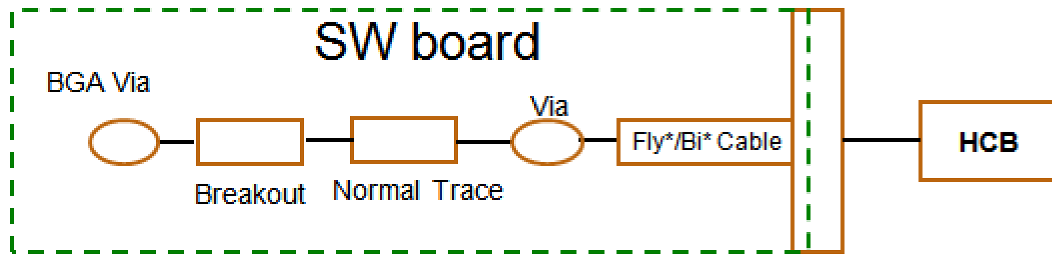
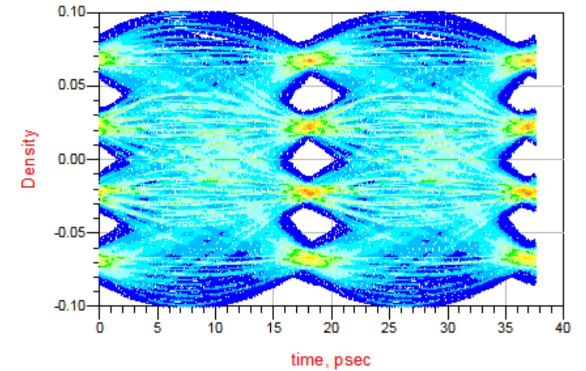


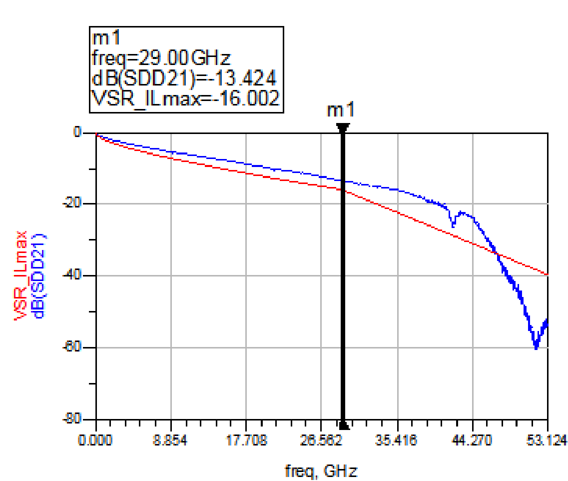


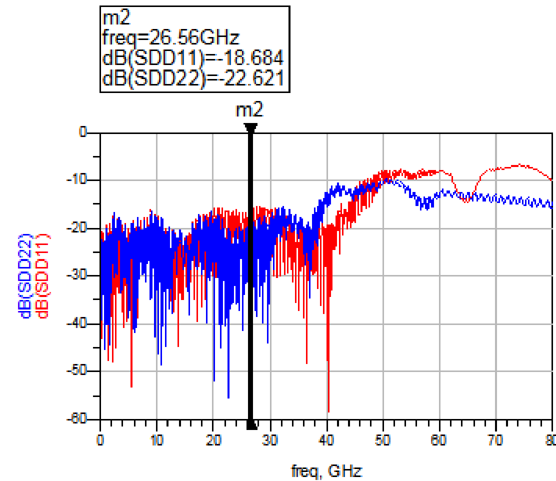
The same PCB related info as C2M channel. Total 5 inches PCB trace.

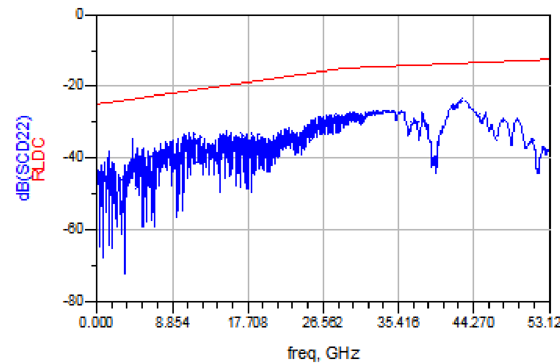
Referred to CEI-112G-VSR-PAM4 Draft, channel insertion loss budget is 16dB@29GHz.

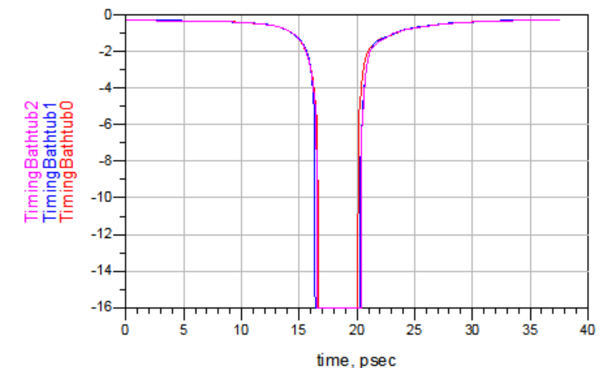
Eye diagram simulation used IBIS AMI model, RX side used CTLE, DFE not used.

measurement	Summary
WidthAtBER0	4.235E-12
WidthAtBER1	4.141E-12
WidthAtBER2	4.424E-12
HeightAtBER0	0.022
HeightAtBER1	0.025
HeightAtBER2	0.024
Tmid	1.835E-11
Vlow	0.021
Vmid	0.022
Vupp	0.022
Hlow	3.765E-12
Hmid	4.141E-12
Hupp	3.859E-12
AVlow	0.046
AVmid	0.045
AVupp	0.046
CrossingLevel0	-0.042

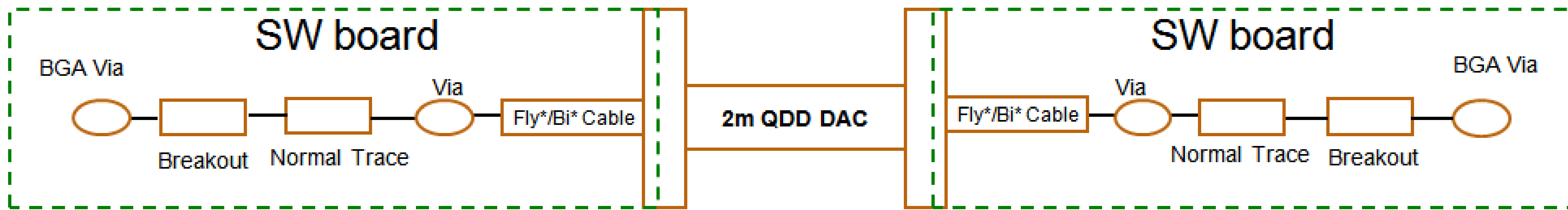








802.3ck 100GBASE-CR Channel With Fly*/Bi* Cable

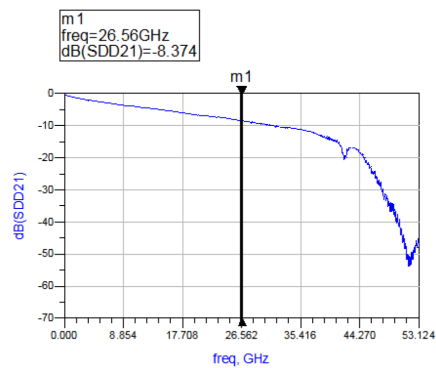


The same PCB related info as C2M channel. Total 3.5 inches PCB trace in one SW board.

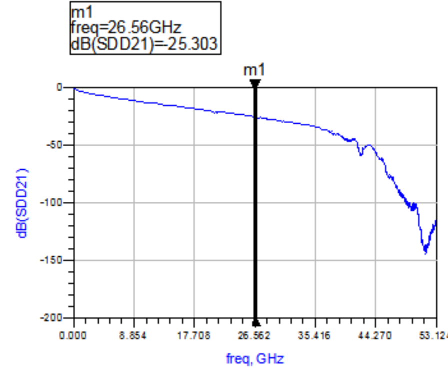
From BGA ball to DAC connector the IL spec is 6.875dB@26.56GHz. Connector spec is 1.6dB@26.56GHz.

Referred to 802.3_3ck, C2M host channel insertion loss budget is 28.5dB@26.56GHz.

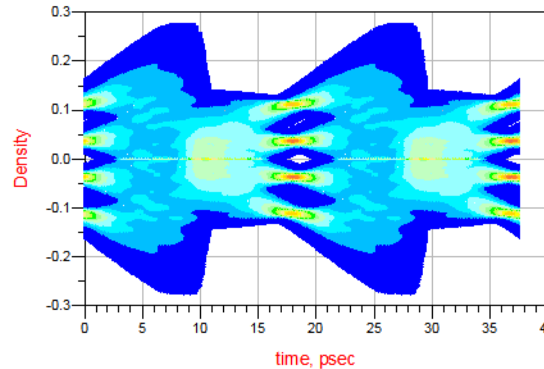
Eye diagram simulation used IBIS AMI model with switch PKG model.

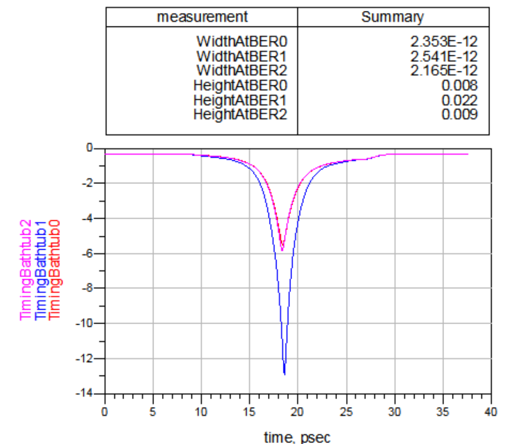


Without HCB spec
is 8.475dB@26.56GHz



Without IC PKG spec
Is 28.5dB@26.56GHz





measurement	Summary
WidthAtBER0	2.353E-12
WidthAtBER1	2.541E-12
WidthAtBER2	2.165E-12
HeightAtBER0	0.008
HeightAtBER1	0.022
HeightAtBER2	0.009

Conclusion

- **Celestica is preparing C2M, VSR and CR channel optimization for compliance and eye diagram simulation with IBIS-AMI model.**
- **Detailed via/pad structure optimization is needed. Or it will impact SI performance very much.**
- **Max 6 mils via stub is needed for 112G channel. Or it will impact IL and RL very much.**
- **M7 level PCB material still can be an option for 112G switch, but if you need improved SI performance, M8 level PCB material is needed. Especially for Fly*/Bi* cable application.**
- **In our simulation, the C2M and VSR Host channel trace length is 10inch, but CR host channel spec is strict. Only 5 inches can be used for CR channel in one SW board.**
- **We didn’t do crosstalk and COM(Channel Operating Margin) simulation this time. For PCB layout still under evaluation. Our goal is to control crosstalk in a very low level.**
- **Will continue to update the 112G simulation.**

Thank You