DDR5 AMI Modeling and Simulation

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Agenda

• DDR5 Introduction
• DDR5 Main Challenges
• DDR5 Simulation and Modeling Solutions
  • Channel Simulation
  • Why IBIS AMI?
  • DDR5 AMI Challenges & Solutions
DDR5 Introduction
### DDR5 Introduction

<table>
<thead>
<tr>
<th>Signal</th>
<th>MT/s (Mega Transfers Per second)</th>
<th>Generation</th>
<th>Characteristics</th>
<th>Specification</th>
<th>Introduction</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>DDR5</td>
<td>“Hyper Speed”</td>
<td></td>
<td>2019</td>
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<td></td>
<td></td>
<td></td>
<td>• Eye collapses</td>
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<td>• Impulse response</td>
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<td></td>
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<td></td>
<td>• BER Rj/Dj, Rn/Dn</td>
<td></td>
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<tr>
<td>3200 – 8400</td>
<td></td>
<td>DDR4</td>
<td>“Serial Speed”</td>
<td></td>
<td>2014</td>
</tr>
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<td></td>
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<td></td>
<td>• Rx Masks</td>
<td></td>
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<td></td>
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<td></td>
<td>• Bit error rates</td>
<td></td>
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</tr>
<tr>
<td>1600 – 3200</td>
<td></td>
<td>DDR/2/3</td>
<td>“High Speed Digital”</td>
<td></td>
<td>2002</td>
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<tr>
<td></td>
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<td></td>
<td>• Transmission lines</td>
<td></td>
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<td>• Ts / Th, Skew</td>
<td></td>
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<tr>
<td>200 – 1600</td>
<td></td>
<td>SDRAM</td>
<td>“Low Speed”</td>
<td></td>
<td>1961</td>
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<td></td>
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<td>• Fanout</td>
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<td></td>
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<td></td>
<td>• Capacitance</td>
<td></td>
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<td>33 – 133</td>
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</tbody>
</table>

**DDR5 AMI Modeling and Simulation**
## DDR4 Vs. DDR5

<table>
<thead>
<tr>
<th>Feature</th>
<th>DDR4</th>
<th>DDR5</th>
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</thead>
<tbody>
<tr>
<td>Data rates</td>
<td>1600-3200 MT/s</td>
<td>3200-8400 MT/s</td>
</tr>
<tr>
<td>$V_{DD}/V_{DDQ}/V_{PP}$</td>
<td>1.2/1.2/2.5</td>
<td>1.1/1.1/1.8</td>
</tr>
<tr>
<td>Internal $V_{REF}$</td>
<td>$V_{REFDQ}$</td>
<td>$V_{REFDQ}, V_{REFCA}, V_{REFCS}$</td>
</tr>
<tr>
<td>DQ receiver equalization</td>
<td>CTLE</td>
<td>DFE</td>
</tr>
<tr>
<td>Write leveling training modes</td>
<td>Yes</td>
<td>Improved</td>
</tr>
<tr>
<td>Loopback mode</td>
<td>None</td>
<td>Yes</td>
</tr>
</tbody>
</table>
DDR5 Main Challenges
**DDR5 Challenges - Jitter**

- Higher Data Rate $\Rightarrow$ Higher ISI
- ISI & RJ will decrease timing margin.
- Rx Eye Diagram/BER Contour need to be simulated/measured under low BER (1E-16)

### BER Contour at 1e-16 tells us the Real Margin

<table>
<thead>
<tr>
<th>Number of UI</th>
<th>BER</th>
<th>Eye Width</th>
<th>Eye Height</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.3e5</td>
<td>7.69e-6</td>
<td>352.72 ps</td>
<td>310.9 mv</td>
</tr>
<tr>
<td>2.80e6</td>
<td>3.57e-7</td>
<td>347.52 ps</td>
<td>288.3 mv</td>
</tr>
<tr>
<td>6.31e7</td>
<td>1.58e-8</td>
<td>339.70 ps</td>
<td>275.8 mv</td>
</tr>
<tr>
<td>1.10e8</td>
<td>9.13e-9</td>
<td>339.06 ps</td>
<td>271.1 mv</td>
</tr>
<tr>
<td>1e9</td>
<td>1e-9</td>
<td>336.45 ps</td>
<td>265.6 mv</td>
</tr>
</tbody>
</table>
**DDR5 Challenges - Jitter**

**BER Contour at 1e-16 tells us the Real Margin**

**No Jitter** –
Just ISI from Channel

No Jitter –
More ISI from Channel due to higher speed

Random Jitter
= 0.02 UI
Applied at Tx
(2%)

Jitter injected at Tx, and eye measured at the DRAM Solder-Ball (Rx Input)

47% Reduction in Timing Margin
(27ps less margin to mask)
The Importance of the Signal RETURN PATH

No Crosstalk, No Jitter – Just ISI from Channel

-23dB @2.4G Nyquist -17dB @4.8G Nyquist

Far-end/Near-end Crosstalk

Signal Return Path – through shared Ground Pin

PCB Trace Routing of Victim + Worst Aggressors

With Crosstalk
DDR5 Simulation and Modeling Solutions
1. Multiple Tx and Rx in one Simulation

2. Calculate Impulse Responses for both a Rising Edge and a Falling Edge

3. Simulator applies the correct impulse responses to the part of the waveform that is rising, or falling

4. Simulator passes DC Offset value to the AMI model

5. Simulator can pass both DQ & DQS waveform to AMI model

DDR5 Channel Simulation
Introducing IBIS AMI for DDR Signals

• EQ Necessary for TX: 3 Tap Pre-Emphasis (Feed Forward Equalization)

• EQ Necessary for RX: CTLE/VGA/DFE

• IBIS-AMI offers
  ➢ Portability – One IBIS-AMI mode can run on many EDA tools
  ➢ IP Protection – Digital signal processing behavior is concealed in model DLL/shared object
  ➢ Interoperability - IC Vendor A ↔ IC Vendor B (AMI defines a common interface between the vendor model and the EDA channel simulator)
  ➢ Non-linearity – As complex as the model vendor wishes the model to be
  ➢ Performance – Ultra low BER simulations in seconds not days over the traditional SPICE simulation

• AMI has been widely adopted by IC, system and EDA companies for SerDes signals but this is the first application to DDR single-ended signals.
What Do We Need for DDR5 AMI To Work?

Supporting Parallel, single-ended signals with external clocks

Input to DRAM

After Gain & 4 Tap DFE

1.1V

0.55V

Single-Ended Signal

Asymmetric Eye:
Rise Time ≠ Fall Time

Asymmetric Eye:
Crossing Points are shifted in the Equalized Eye

DFE Clocked by DQS:

- Correlated Jitter on DQ & DQS cancels out
- Uncorrelated Jitter on DQS is transferred to DQ
• Single-Ended (SE) signals
• Both differential and common modes

→ A new reserved parameter DC_Offset in BIRD197.7
• SE waveform at Rx DLL Input node = Rx GetWave input + DC_Offset
• DC_Offset value is a constant that is characterized and passed into Rx Init by EDA tool
• Rx GetWave input & output waveforms both center around 0V
DDR5 AMI Challenges & Solutions

Asymmetric Rise and Fall Edges in Single-Ended Signal

• Single-Ended (SE) signals
  • **Asymmetric** rise and fall edges
  • Simulation using symmetrical edges yields unrealistically symmetrical eye, resulting in inaccurate Vref determination and timing and voltage margin measurements.

→ EDA tool will capture asymmetrical rise and fall edges in waveform calculations.
• Higher data rate results higher ISI

→ 4-Tap DFE (Decision Feedback Equalizer)

### Mode Register Settings (per DQ)

<table>
<thead>
<tr>
<th></th>
<th>All values subject to change</th>
</tr>
</thead>
<tbody>
<tr>
<td>Variable Gain</td>
<td>-6dB to 6dB</td>
</tr>
<tr>
<td>VrefDQ</td>
<td>-3 to +3 Offset steps</td>
</tr>
<tr>
<td>DFE Tap 1</td>
<td>-200mV to 50mV</td>
</tr>
<tr>
<td>DFE Tap 2</td>
<td>-75mV to 75mV</td>
</tr>
<tr>
<td>DFE Tap 3</td>
<td>-60mV to 60mV</td>
</tr>
<tr>
<td>DFE Tap 4</td>
<td>-45mV to 45mV</td>
</tr>
</tbody>
</table>

**Variable Gain**

**Vref**

**Clk**
• No embedded CDR for DFE in DDR DQ Rx.

→ New parameter **Rx Use Clock Input** in BIRD204

• Output of DQS (DQS Rx AMI_GetWave)

![Diagram of DDR5 AMI Challenges & Solutions](image)
Appendix: Adaptive DFE

• The action of the DFE is to feed back a weighted sum of past decision to cancel the ISI they cause in the present signaling interval.
  \[ y_k = x_k + \sum_{i=1}^{N_{taps}} c_i \cdot slice(y_{k-i}) \]

• Feedback taps \( c_i \) is adapted with adaptive formula:
  \[ e = G \cdot y_k - slice(y_k) \]
  \[ c_i = c_{i-1} - \alpha \cdot e \cdot slice(y_{k-i}) \]

• Where
  • \( y_k \) is the DFE differential output voltage
  • \( x_k \) is the DFE differential input voltage
  • \( c_i \) is the DFE feedback coefficient
  • \( e \) is the error value between EQ output at clock and output of decision
  • \( slice(y_{k-i}) \) is the decision function output voltage, it may be BitVoltageAtChannelInput (e.g. ±0.5)
  • \( k \) is the sample index in UI
  • \( G \) is scaling factor
DDR5 AMI Challenges & Solution

High ISI & Clocking

- Controller DQ Rx Model Example
  - VGA, Gain compression, CTLE, adaptive DFE
  - DQS as clock with PI (Phase Interpolator)

- DRAM DQ Rx Model Example
  - VGA, Gain Compression, (CTLE), adaptive DFE
  - DQS as clock
**DDR5 AMI Challenges & Solution**

- Controller DQ Rx model can internally train the phase interpolator to adjust data-strobe skew for optimal DFE clocking

**DFE with PI followed DQS**

**Before Equalization**

**After Equalization**

- (with phase interpolator training)
- (without phase interpolator training)
Correlated jitters in DQ & DQS can be tracked in DQ Rx by clock forwarding.

Unmatched DQ & DQS Rx are allowed.

- DQ Rx package wo. DQ & DQS Tx SJ
- DQ Rx output wo. DQ & DQS Tx SJ
- DQ Rx package with DQ & DQS Tx SJ (0 DQS-to-DQ delay)
- DQ Rx output with DQ & DQS Tx SJ (0 DQS-to-DQ delay)
- DQ Rx package with DQ & DQS Tx SJ (5UI DQ-to-DQS delay)
- DQ Rx output with. DQ & DQS Tx SJ (5UI DQ-to-DQS delay)
Appendix: Others: TX Equalizer

Pre-shoot or De-emphasis

- Boost signal strength around high frequency range
- Can be constructed by a N-tap FIR filter

\[ y(n) = \sum_{k=0}^{N_F} b_k x(n - k) \]
CTLE (Continuous Time Linear Equalizer)

- CTLE is an amplifier with Analog Filter
- CTLE can be modeled by transfer function (Poles/Zeros)

\[
H(s) = A_{pre} \frac{(s - \omega_{z1})(s - \omega_{z2}) \ldots}{(s - \omega_{p1})(s - \omega_{p2})(s - \omega_{p3}) \ldots}
\]

Zeros in rad/s = \([\omega_{z1}, \omega_{z1}, \ldots]\)

Poles in rad/s = \([\omega_{p1}, \omega_{p2}, \omega_{p3}\ldots]\)

Pre-Factor: \(A_{pre}\)