Virtual Asian IBIS Summit (Tokyo)

DDR memory system simulation method

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KEI Systems
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OVERVIEW

• (LP)DDR Memory has 5 generations
• Every generation is x2 speed and lower Vdd from previous
• Higher speed makes it difficult to design PCB system
• New generation DDR implements new features to make PCB design easier
• New features require changes to simulation methods
(LP)DDR Speed/Vdd

- JEDEC

[Diagram showing the evolution of DDR memory technologies from DDR to LPDDR over time, with associated voltage and clock speed.]
# (LP)DDR Features on Generation

## JEDEC

<table>
<thead>
<tr>
<th>Item</th>
<th>DDR</th>
<th>LPDDR</th>
<th>DDR2</th>
<th>LPDDR2</th>
<th>DDR3</th>
<th>LPDDR3</th>
<th>DDR4</th>
<th>LPDDR4</th>
<th>DDR5</th>
<th>LPDDR5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transfer Speed(gBPS)</td>
<td>200〜400M</td>
<td>200〜400M</td>
<td>400〜800</td>
<td>400〜1066</td>
<td>800〜2066</td>
<td>800〜1600</td>
<td>1600〜3200</td>
<td>1600〜3200</td>
<td>3200〜6400</td>
<td>3200〜6400</td>
</tr>
<tr>
<td>Clock(Hz)</td>
<td>100〜200M</td>
<td>100〜200M</td>
<td>200〜400M</td>
<td>200〜533M</td>
<td>400〜1033</td>
<td>400〜800</td>
<td>800〜1600</td>
<td>800〜1600</td>
<td>1600〜3200</td>
<td>1600〜3200</td>
</tr>
<tr>
<td>Vdd/Vddq</td>
<td>2.5</td>
<td>1.8</td>
<td>1.8</td>
<td>1.2</td>
<td>1.5</td>
<td>1.2</td>
<td>1.2</td>
<td>1.1/0.6</td>
<td>1.1</td>
<td>1.05/0.5</td>
</tr>
<tr>
<td>Output Impedance</td>
<td>Full/Half</td>
<td>Full/Half</td>
<td>Full/Reduc</td>
<td>34/48/60/8</td>
<td>30/40</td>
<td>34/48</td>
<td>34/40</td>
<td>34/40</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>ODT Value</td>
<td>—</td>
<td>—</td>
<td>50/75/150/</td>
<td>—</td>
<td>20/30/40/6</td>
<td>34.3/40/6</td>
<td>34.4/40/6</td>
<td>640/48/60/8</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>ODT Pull</td>
<td>—</td>
<td>—</td>
<td>Vdd/2</td>
<td>—</td>
<td>Vdd/2</td>
<td>Vdd</td>
<td>Vdd</td>
<td>Vdd</td>
<td>Vdd</td>
<td></td>
</tr>
<tr>
<td>Training</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Equalizer/Empahys</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Strage</td>
<td>16Mb〜256Mb</td>
<td>64Mb〜2Gb</td>
<td>128Mb〜4Gb</td>
<td>64Mb〜32Gb</td>
<td>512Mb〜8Gb</td>
<td>1Gb〜32Gb</td>
<td>2Gb〜16Gb</td>
<td>4Gb〜32Gb</td>
<td>8Gb〜64Gb</td>
<td>4Gb〜32Gb</td>
</tr>
</tbody>
</table>
DDR vs. LPDDR

- **DDR**
  - Application: HPC, PC, Built-in System
  - High-end Performance: Speed, Memory Size
  - Connect multiple memories
  - BGA
    - DIMM/SIMM Module

- **LPDDR**
  - Application: Mobile device
  - Low Power First, next size then speed, memory size
  - Connect one or a few memories
    - POP (Package-on-Package), Flip Chip, BGA
DDR Technologies

- DDR
  - Lower Power
    - Green Energy
      - Data Center, Super Computer
  - LPDDR
    - Higher Speed, More Memory Size
      - High Performance Mobile Device
        - Smart Phone, Mobile Game, 5G
- DDR4/LPDDR4
- DDR5/LPDDR5
Basic Simulation Flow

- Schematic Design
- PCB Design Concept
- Pre-Layout Simulation
- Layout Design
- Post-Layout Simulation
- Manufacturing

PCB Design

- PCB Stack-up
- Temporary Placement
- Temporary Etch Length
- Layer Structure
- Design Rule
- Design Verification
- Sign off
DDR~DDR3

- Features for PCB Design
  - Multi-Driver Strength
  - Multi-Value ODT (DDR2)
  - Fly-by (DDR3)

- Considerations
  - Typical/Worst
  - Derating
Tolerance of IC Characteristics

- Drive: Slow - Fast
- Receiver: Slow - Fast

- IO Model
  - Fast/Typical/Slow
  - Driver: Output Impedance Ramp
  - Receiver: Threshold Voltage

- C Comp, Package L/C/R

- Vcc Voltage
  - Vtyp +/- 5~10%

- IC Temperature
Typ vs. Corner

- **Fast**

- **Typ**

- **Slow**

- **DDR4 2400**
  - Driver: DQ
  - Receiver: DQ

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**Ramp**

- $R_{load} = 50$

- $dV/dt_r$:
  - Typ: $4.1235E-01/6.4489E-11$
  - Min: $3.8046E-01/8.4106E-11$
  - Max: $4.4653E-01/5.2562E-11$

- $dV/dt_f$:
  - Typ: $4.5987E-01/6.2372E-11$
  - Min: $4.3947E-01/7.9203E-11$
  - Max: $4.6741E-01/4.9982E-11$

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**Falling Waveform**

- $V_{fixture} = 1.2V$
- $V_{fixture\_min} = 1.14V$
- $V_{fixture\_max} = 1.26V$
- $R_{fixture} = 50\Omega$
- $C_{fixture} = 0F$

<table>
<thead>
<tr>
<th>Time</th>
<th>V(typ)</th>
<th>V(min)</th>
<th>V(max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.00000000E+00</td>
<td>1.19999848E+00</td>
<td>1.13999700E+00</td>
<td>1.25999947E+00</td>
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<tr>
<td>5.00000000E-12</td>
<td>1.19999849E+00</td>
<td>1.13999700E+00</td>
<td>1.25999948E+00</td>
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<tr>
<td>1.00000000E-11</td>
<td>1.19999849E+00</td>
<td>1.13999700E+00</td>
<td>1.25999948E+00</td>
</tr>
</tbody>
</table>
Derating

- Timing Specification
  - Reference: Threshold Voltage
    - Timing differs based on Slew-Rate
  - Standard is the value of 1v/ns

Table 69 — Derating values DDR3-800/1066/1333/1600 tHs/tIH - ac/dc based

<table>
<thead>
<tr>
<th>CMD/ADD Slew Rate V/ns</th>
<th>0.4</th>
<th>0.5</th>
<th>0.6</th>
<th>0.7</th>
<th>0.8</th>
<th>0.9</th>
<th>1.0</th>
<th>1.5</th>
<th>2.0</th>
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<tbody>
<tr>
<td>4.0 V/ns</td>
<td>62</td>
<td>60</td>
<td>60</td>
<td>62</td>
<td>64</td>
<td>64</td>
<td>67</td>
<td>67</td>
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<tr>
<td>3.0 V/ns</td>
<td>60</td>
<td>62</td>
<td>64</td>
<td>67</td>
<td>70</td>
<td>71</td>
<td>67</td>
<td>67</td>
<td>67</td>
</tr>
<tr>
<td>2.0 V/ns</td>
<td>62</td>
<td>64</td>
<td>67</td>
<td>70</td>
<td>72</td>
<td>73</td>
<td>67</td>
<td>67</td>
<td>67</td>
</tr>
<tr>
<td>1.8 V/ns</td>
<td>62</td>
<td>62</td>
<td>64</td>
<td>67</td>
<td>70</td>
<td>72</td>
<td>67</td>
<td>67</td>
<td>67</td>
</tr>
<tr>
<td>1.6 V/ns</td>
<td>60</td>
<td>60</td>
<td>60</td>
<td>62</td>
<td>64</td>
<td>64</td>
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<tr>
<td>1.4 V/ns</td>
<td>60</td>
<td>60</td>
<td>62</td>
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<tr>
<td>1.2 V/ns</td>
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<td>60</td>
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<td>60</td>
</tr>
<tr>
<td>1.0 V/ns</td>
<td>60</td>
<td>60</td>
<td>60</td>
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<td>60</td>
<td>60</td>
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</tr>
</tbody>
</table>
DDR3 System Simulation

- IBIS Model
- Timing Simulation
  - Bus Simulation (Crosstalk)
  - 8 Bit Parallel Signals
  - PRBS
- Power Aware
- Eye Pattern
  - Derating
- Worst Case/Typical Case
  - Margin/Yield Rate
**New Features**

- DQ Vref Training/ZQ calibration
- Support Eye Mask
  - No more Derating

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**Diagram**

- **Controller**
  - Ron: 34/40
  - Write
  - Read

- **ODT/Driver Vref**
  - Set

- **DDR**
  - Ron: 34/40
  - ODT: 34/40/48/60/120/240/OFF

- **MPR**

**Flowchart**

- Return Data
- Same Data
- Different Data

**Convention of Values**

- Same
- Different

**Center of Convention**
DDR4/LPDDR4 System Simulation

- IBIS Model
  - Timing Simulation
    - Bus Simulation (Crosstalk)
      - 8 Bit Parallel Signals
    - PRBS
  - Power Aware
  - Eye Mask
    - No More Derating
  - Best Case Analysis
    - Any One Case is Good, Real Should be Better
- IBIS–AMI (Idea)
  - Auto Model Selector
  - Crosstalk Analysis, SSN Analysis
• New Features
  • Analog Driver/Receiver
    • Emphasis
    • Equalizer
      • Feature of PCI Express/High Speed Serial
  • Separate Clock/DQ Write/DQ Read
    • CMD/Address is Slower than DQ
DDR5 Simulation

- IBIS–AMI
  - Emphasis, Equalization: IBIS Model Supports Driver/Receiver
  - Crosstalk Analysis?
  - SSN Effect?
Reference

  S.Maeda, 2016 Asian IBIS Summit Tokyo