A further study on the application of IBIS to CISPR25 based EMI analysis of DCDC converter
~Resolving unexpected ringing in the waveform~

Kazuyuki Sakata, Renesas Electronics Corp.
Koji Ichikawa, DENSO CORP.
Miyoko Goto, Ricoh Corp.
Toshiki Kanamoto, Hirosaki University
Agenda

- Motivation and objective
- Impedance modeling of DCDC converters
- Measurement settings and results
- Simulation results and comparison with measurement
- Study on the discrepancy from the measurement
  - From IBIS model to Spice macro model
  - Improving the Spice macro model
- Summary
- Remaining issues and plans
Motivation and objective

Most power device models are provided as Spice models dedicated to specific circuit simulators
→ Can not freely choose a circuit simulator
   Potential limitation by expression of each circuit simulator
If the power device model can be represented with IBIS
→ Can freely choose a circuit simulator
   Can improve usability by gaining regularity
Furthermore, if the IBIS model can be derived from measurement
→ Modeling made easier

JEITA IBIS-TG studies IBIS modeling of a power device DCDC converter, targeting to EMI simulation (CISPR25 conducted noise simulation)

In this presentation, we discuss error caused in the IBIS based DCDC noise simulation compared to the measurement, reported at 2019 Asian IBIS Summit (TOKYO, JAPAN)
Agenda

- Motivation and objective
- Impedance modeling of DCDC converters
- Measurement settings and results
- Simulation results and comparison with measurement
- Study on the discrepancy from the measurement
  - From IBIS model to Spice macro model
  - Improving the Spice macro model
- Summary
- Remaining issues and plans
DCDC converter impedance measurement

DCDC converter: RICOH RP510L004N-TR-A

IO Pins for impedance measurement

<table>
<thead>
<tr>
<th>Pin (S-G)</th>
<th>No. (S-G)</th>
<th>Pitch (mm)</th>
<th>Bias voltage (V)</th>
<th>Freq. (Hz) ※</th>
</tr>
</thead>
<tbody>
<tr>
<td>PVIN-PGND</td>
<td>PIN2-PIN10</td>
<td>2.65mm ±0.3mm</td>
<td>0, 0.3, 0.6, 1, 2, 3, 3.6, 4, 5, 5.5</td>
<td>1k-3G</td>
</tr>
<tr>
<td>PVIN-LX</td>
<td>PIN2-PIN11</td>
<td>2.6mm ±0.3mm</td>
<td>0, 0.3, 0.6, 1, 2, 3, 3.6, 4, 5, 5.5</td>
<td>1k-3G</td>
</tr>
<tr>
<td>LX-PGND</td>
<td>PIN11-PIN10</td>
<td>0.5mm ±0.1mm</td>
<td>0, 0.3, 0.6, 1, 2, 3, 3.6, 4, 5, 5.5</td>
<td>1k-3G</td>
</tr>
</tbody>
</table>

※Frequency depends on equipment

Equipment used in this report: HP4291A

Impedance measurement and equivalent circuit

<table>
<thead>
<tr>
<th></th>
<th>$L$ (nH)</th>
<th>$C$ (pF)</th>
<th>$R$ (Ω)</th>
<th>$R_{\text{leak}}$ (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PVIN-PGND</td>
<td>0.19</td>
<td>186</td>
<td>0.66</td>
<td>1.87e7</td>
</tr>
<tr>
<td>PVIN-LX</td>
<td>0.38</td>
<td>319</td>
<td>0.24</td>
<td>9339</td>
</tr>
<tr>
<td>LX-PGND</td>
<td>0.59</td>
<td>232</td>
<td>0.29</td>
<td>56.12</td>
</tr>
</tbody>
</table>

**PVIN-LX impedance (HighSide)**

**LX-PGND impedance (LowSide)**

**Series cap. 134pF**

$186pF - 134pF = 52pF$
Capacitance description in IBIS format

Specify the measured caps as C_comp_pullup, C_comp_pulldown in the IBIS format.

|Model| bbb |
|Model_type| I/O |
Polarity | Non-Inverting |
Vinl | = .72000000 |
Vinh | = 2.88000000 |
Vmeas | = 1.80000000 |
C_comp | 5.53197e-10 | 4.65065e-10 | 7.07186e-10 | CDL |
C_comp_pullup | 319e-12 | NA | NA | Measurement |
C_comp_pulldown | 232e-12 | NA | NA | Measurement |

In case that large discrepancy appear in the total capacitance, need to regenerate IBIS model adding supplemental capacitance to the Spice netlist.
Agenda

• Motivation and objective
• Impedance modeling of DCDC converters
• Measurement settings and results
• Simulation results and comparison with measurement
• Study on the discrepancy from the measurement
  • From IBIS model to Spice macro model
  • Improving the Spice macro model
• Summary
• Remaining issues and plans
Measurement circuit construction

Vout load
① Open
② 2.2Ω
Measurement environment and results

Power supply (3.6V)

LISN

Substrate

Styrofoam: t=50mm

LISN

15cm wire

Cu plate

Stabilized power supply, LISN GND connect to Cu plate

Measurement equipment inside shield

Power supply as LISN* (PVIN)

Meas. port

*LISN: Line Impedance Stabilization Network

Open load 2.2Ω load

Off (noise floor)
Measured LX waveform

Dead time appears in LX waveform with resistive load

Open load
2.2Ω load
Printed circuit board model

Modeling printed circuit board by electromagnetic analysis

Reference for power supply port is Cu plate located 5cm below
Agenda

- Motivation and objective
- Impedance modeling of DCDC converters
- Measurement settings and results
- Simulation results and comparison with measurement
- Study on the discrepancy from the measurement
  - From IBIS model to Spice macro model
  - Improving the Spice macro model
- Summary
- Remaining issues and plans
Simulation results: Open

Large ringing appears in the simulation results unlike measurements.

IBIS input
LX (DCDC converter output)
LISN power supply
Resonance current

Sim: PVIN current
Sim: CIN current

Meas.
Sim
Simulation results: Resistive load

Large ringing appears in the simulation results unlike measurements, as well.

Dead time is reappeared in the simulation.

Ringing caused by resonance current path through PVIN, PGND, CIN.

Sim: PVIN current
Sim: CIN current

Meas.
Sim
CISPR25 (Voltage) PVIN Noise: Open load

The simulation is up to 30db larger than the measured
Even Spice simulation show some ringing waveform
After trying to eliminate the ringing, consider the JISSO modeling.

※With pre-layout Spice netlist
Agenda

• Motivation and objective
• Impedance modeling of DCDC converters
• Measurement settings and results
• Simulation results and comparison with measurement
• Study on the discrepancy from the measurement
  • From IBIS model to Spice macro model
  • Improving the Spice macro model
• Summary
• Remaining issues and plans
From IBIS model to Spice macro-model

IBIS analysis by a circuit simulator is a black box approach. Not suitable for cause analysis.
Macro modeling replacing IV tables in IBIS with G element in Spice. Then, white box analysis.

Confirming current in each element, considering the deadtime.
A simple implementation

To simplify, only PVIN inductance is converted from S-parameter

Only inductance (0.9nH) is included in the circuit to analyze.

From EM field solver
CIN loop inductance: 0.88nH
CAVIN loop inductance: 2.17nH
Estimating deadtime from measurement (LX voltage)

Open load

2.2Ω load

9.5ns

13ns
Simulation result of Spice macro model (Simplified)

LX voltage
Open load

LX voltage
2.2Ω load

Ringing due to current concentration during switching

Fluctuations in the actual measurement due to prebuffer operation.

Measurement
Sim
HighSideMOS IN
LowLideMOS IN

Input TR/TF=1ns
Discussion according to macro model (Open load)

During deadtime, HighSide body diode dominated characteristic

HighSideMOS char.

During deadtime, LowSide body diode dominated characteristic

LowSide MOS char.

① Mainly via paras. cap.

② Mainly via paras. cap.

③ Mainly via paras. cap.

④ Mainly via paras. cap.

LX voltage
Open load

Inductance current

Current flow in IC

Current flow out from IC

Measured
Sim
HighSideMOS入力
LowSideMOS入力
Discussion according to macro model (2.2Ω load)

During deadtime, HighSide body diode dominated characteristic

HighSideMOS char.

During deadtime, LowSide body diode dominated characteristic

LowSide MOS char.

LX voltage
Open load

Inductance current

Current flow out from IC

Meas.
Sim
HighSideMOS IN
LowSideMOS IN

⑤

⑥

⑦

⑧

Copyright© JEITA SD-TC All Rights Reserved 2016-2021
Agenda

• Motivation and objective
• Impedance modeling of DCDC converters
• Measurement settings and results
• Simulation results and comparison with measurement
• Study on the discrepancy from the measurement
  • From IBIS model to Spice macro model
  • Improving the Spice macro model
• Summary
• Remaining issues and plans
Modified Spice macro model

The actual drivers were divided into

- HighSide: Small ・ Medium ・ Large transistors
- LowSide: Medium ・ Large transistors

Modified Spice macro model assuming

HighSide: 10%,30%,60%
LowSide: 40%,60%

RCs inserted considering post-layout

Considering post-layout situation distributes the operating timing, and then mitigates the unexpected current.

Modified Spice macro model

Divided G-element by drivability, Inserted parasitic RCs
Modified Spice macro model results (Simplified)

Resolved the unexpected ringing

LX voltage
Open load

LX voltage
2.2Ω load

Meas.
Sim
HighSide IN
LowSide IN
Modified Spice macro model results (S-parameter)

Resolved the unexpected ringing

LX voltage
Open load

LX voltage
2.2Ω load

Meas.
Sim
HighSide IN
LowSide IN

ringing with IBIS
Agenda

• Motivation and objective
• Impedance modeling of DCDC converters
• Measurement settings and results
• Simulation results and comparison with measurement
• Study on the discrepancy from the measurement
  • From IBIS model to Spice macro model
  • Improving the Spice macro model
• Summary
• Remaining issues and plans
Summary

• Considering driver subdivisions as well as post-layout timing and slew rate is indispensable to re-create the actual waveform.

• In our experiment, adopting the actual driver subdivisions with the parasitic RC network has mitigated the previously reported unexpected current concentration and ringing in the waveform.
Remaining issue:
Organized extraction and modeling methods of the red dotted line surrounded part.
Macro-modeling of the pre-buffer resolves the issue, however tradeoff between effectiveness and confidentiality of the driver configuration.

Future work:
CISPR25 EMI analysis utilizing the modified macro model.