Using [Driver Schedule] for PAM4 Testing

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Agenda

- Other Approaches
- [Driver Schedule] Models
- One Full Test Cycle Schedule
- Simulation Results
- PAM4 Eye Diagram
- C_comp Issues
- Conclusions

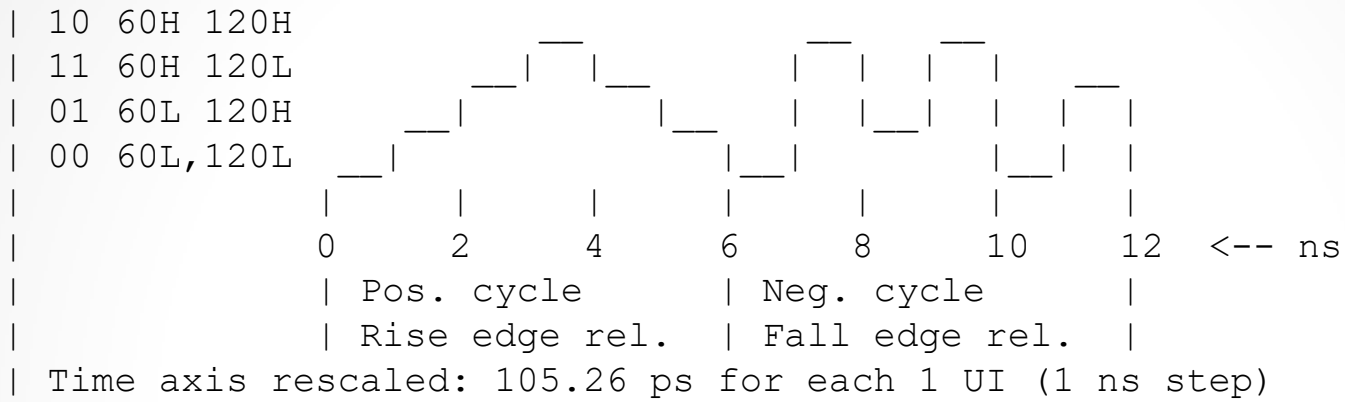
Other Approaches

- IBIS-AMI" "Modeling and Simulation of Single-ended PAM4 Signals in Memory Interfaces" (this meeting)
  - Fangyi Rao:
  - https://www.ibis.org/summits/nov21b/rao.pdf
  - Can program Tx GetWave stimulus
- Multi-lingual: "GDDR6X IBIS Modeling"
  - Randy Wolff, Arpad Muranyi: https://ibis.org/summits/aug21a/wolff2.pdf
  - Extracted K-T waveforms from MatLab script for 24 combinations
  - Implemented buffers using K-T tables and Verilog-A code
  - Switches in and out the buffers of interest based on a driving sequence

[Driver **Schedule**] Models

- Main (top-level) - very weak buffer (1 MΩ I-V tables) with minimal impact and [Driver Schedule]
  - Provides edge sequencing for scheduled models
  - Provides C_comp (more work is needed here)
- Parallel scheduled buffers (produce 40Ω driving impedance)
  - od60, os60 (60Ω Open-drain, Open-source structures)
  - od120, os120 (120Ω Open-drain, Open-source structures)
- Open-* structures can be set to a High-Z state to avoid interacting with each other

One Full Test Cycle Schedule



[Driver Schedule]

os120	105.26ps	421.04ps	210.52ps	105.26ps
os120	210.52ps	526.30ps	210.52ps	105.26ps
os120	315.78ps	631.56ps	421.04ps	105.26ps
os120	NA	NA	421.04ps	315.78ps
os60	NA	NA	631.56ps	526.30ps
od120	105.26ps	421.04ps	631.56ps	105.26ps
od120	210.52ps	526.30ps	631.56ps	105.26ps
od120	315.78ps	631.56ps	631.56ps	105.26ps
od60	NA	NA	210.52ps	315.78ps
od60	NA	NA	421.04ps	526.30ps
od120	NA	NA	421.04ps	631.56ps

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Driver Schedule Combinations

delay values can be defined:

1) Rise_on_dly with Fall_on_dly
2) Rise_off_dly with Fall_off_dly
3) Rise_on_dly with Rise_off_dly
4) Fall_on_dly with Fall_off_dly
5) All four delays defined

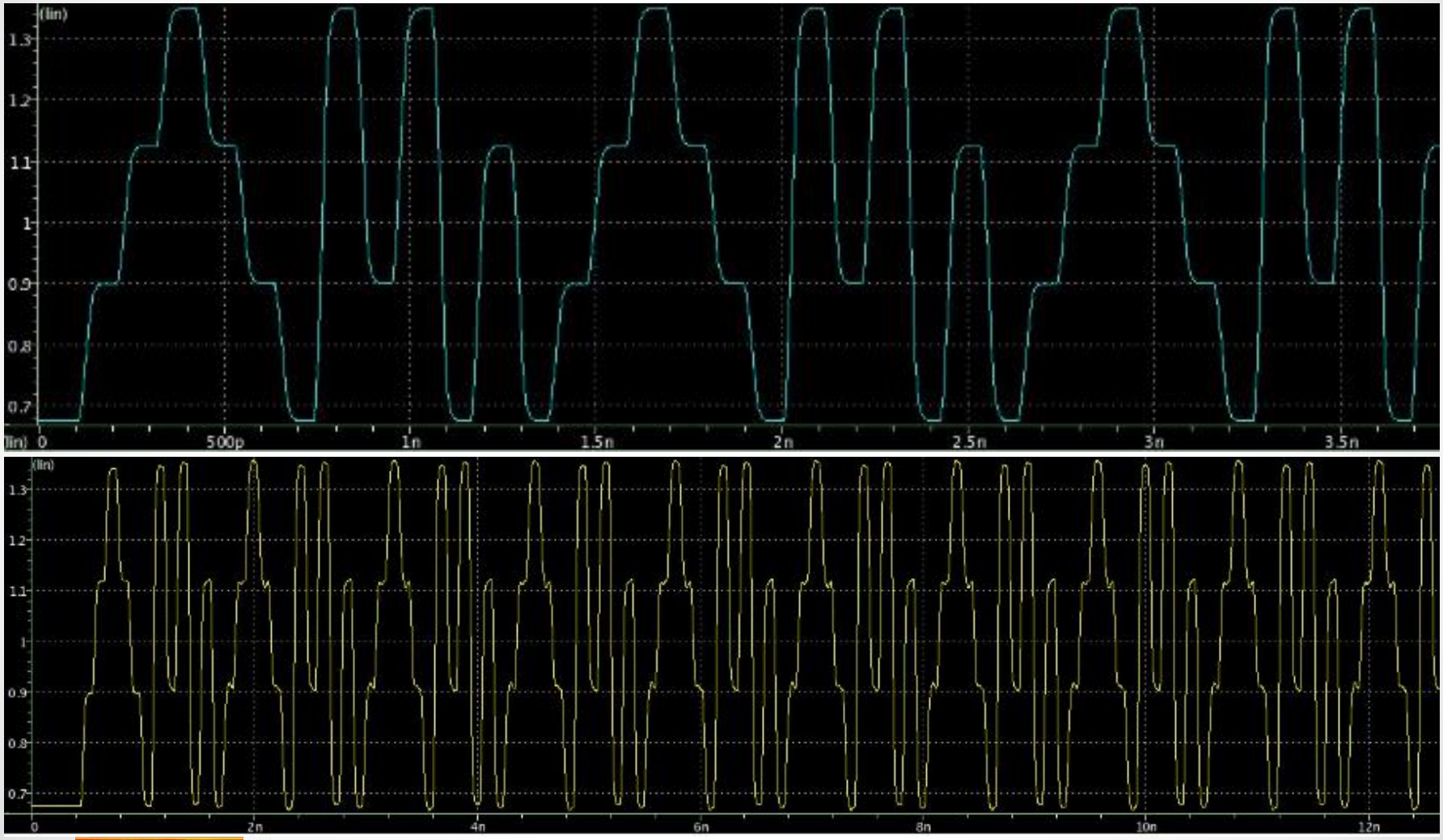
Table 1 – Scheduled Model Initial State

Table Numerical Delay Entries				[Model] Initial State	
Rise_on	**Rise_off**	**Fall_on**	**Fall_off**	**Low**	**High**
r	NA	f	NA	Low	High
NA	r	NA	f	High	Low
r1	r2	NA	NA	Low	Low
r2	r1	NA	NA	High	High
NA	NA	f1	f2	High	High
NA	NA	f2	f1	Low	Low
r1	r2	f2	f1	Low	Low
r2	r1	f1	f2	High	High

Test Load

- C_comp = 400 fF at top-level buffer
- Ideal lossless transmission line Z0 = 50Ω, Td = 333 ps
- TLine termination = 40Ω to 1.35 V
- Simple mismatch created for eye diagram

Simulation Results



Top: Buffer output with C_comp = 400 fF and 40Ω to1.35 V at output
Bottom: At Rx terminator

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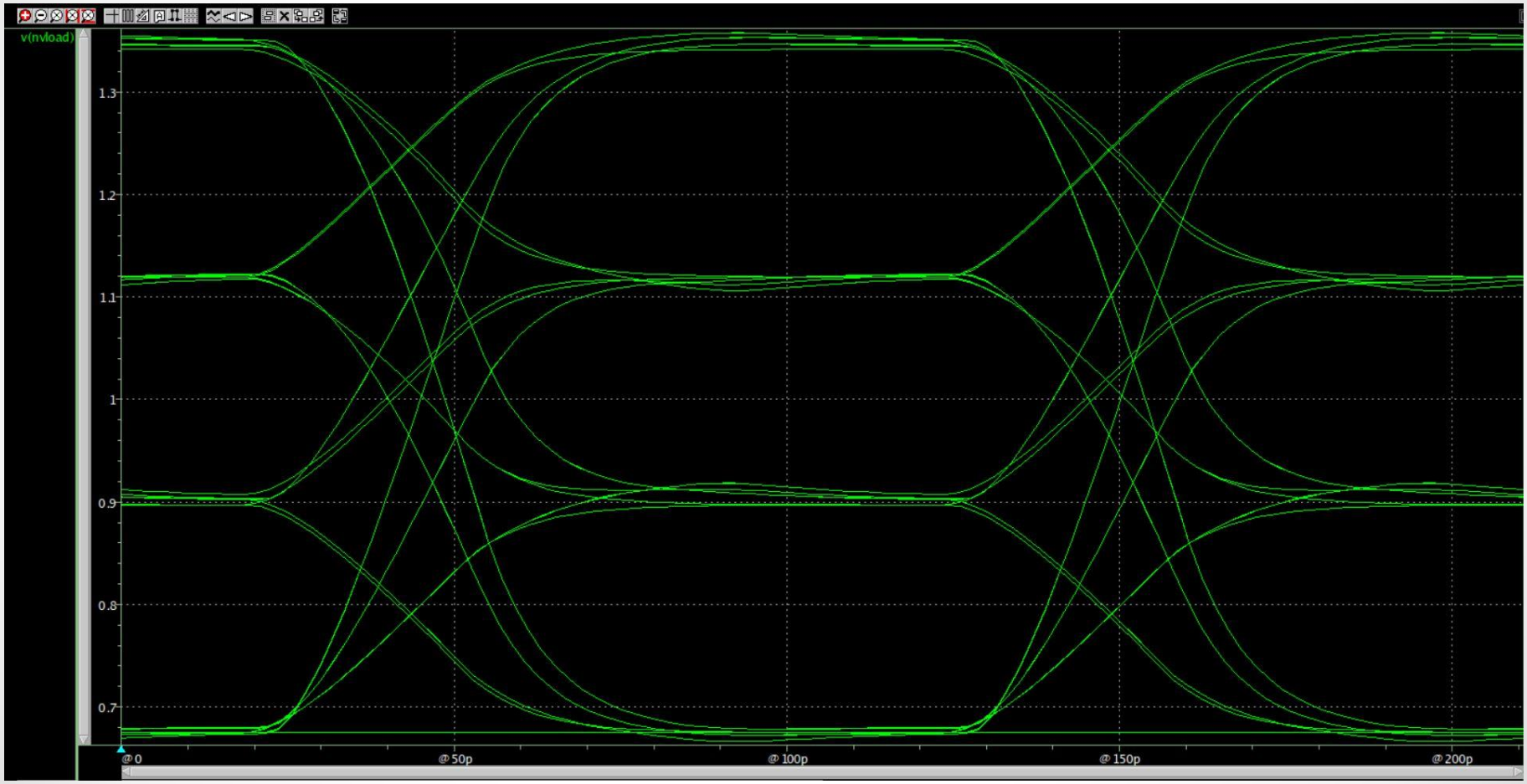
PAM4 Eye Diagram



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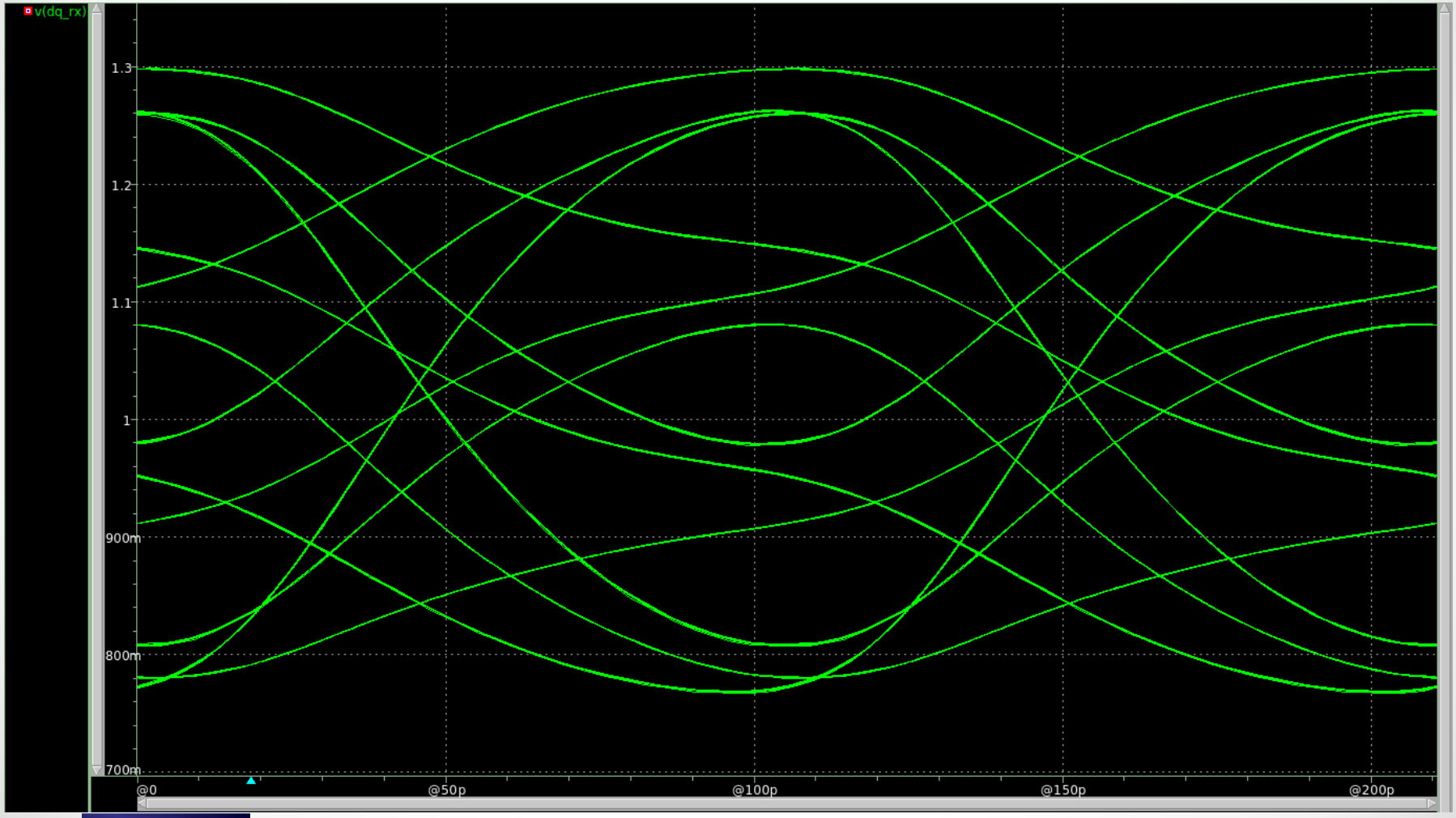
PAM4 Eye for GDDR6X Channel



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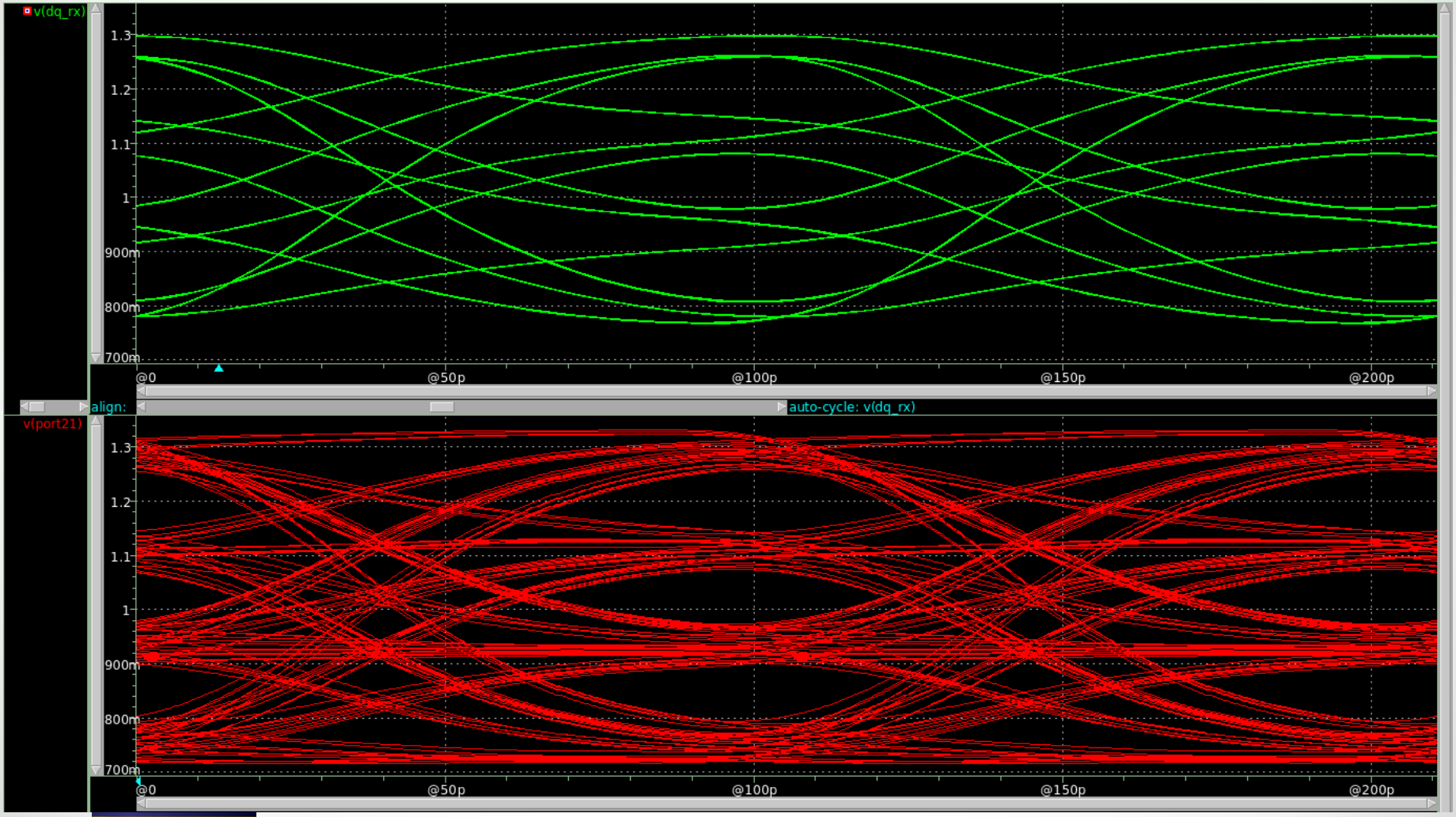
Thanks to Randy Wolff, Micron Technology

Comparison with IBIS-AMI



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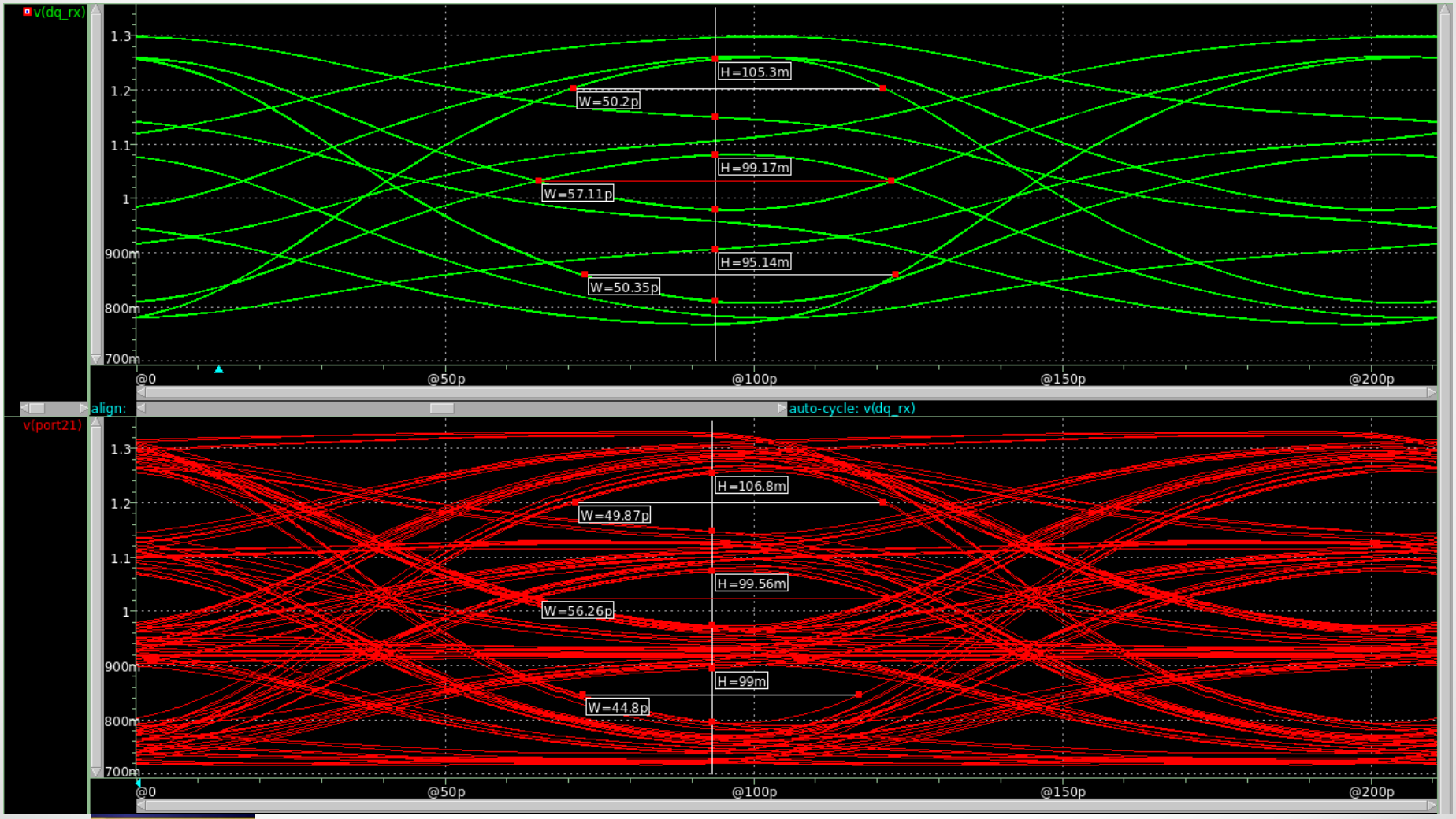
Measurement Comparisons



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C_comp Issues

- To be investigated; only a top-level C_comp is used per the IBIS Specification
- Possible scheduled model improvements
  - Compensate partially with C_fixture (some EDA tools may not be fully support this)
  - Time axis rescaling
  - Waveform peaking or some other method
- Some related past Summit references
  - http://www.ibis.org/summits/feb06/ross1.pdf
  - http://www.ibis.org/summits/sep07a/chen.pdf
  - http://www.ibis.org/summits/feb09/ross.pdf

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Conclusions

- [Driver Schedule] can be used for PAM4 test patterns
  - For all rising and falling transitions (00, 01, 11, 10)
  - Scheduling not easy, but script might be possible for generating random sequences
- Idealized buffers used, but could be generalized
  - Different rising and falling waveform shapes, speeds,
  - Non-linear I-V tables
- Good approximation by combining the od60, os60, od120, and os120 buffers
- Approach uses internal IBIS model processing algorithms
- More investigations are planned