[PSIJ Sensitivity] in IBIS

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Presenter

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Kinger drives CPU+ dGPU better together strategy in mobile platforms and leads strategic PI design tool evolution in Client Computing Group.
Kinger was awarded Ph. D by Shanghai Jiao Tong University in 2001, and MBA degree by W.P. Carey business school in ASU in 2008.
Kinger works in signal & power integrity domains for 20+ years.
Kinger holds 12 granted patents, and published 30+ papers.

Agenda

- Background
- HSIO architecture: Serial & Parallel
- Status Quo, for jitter analysis
- New system jitter analysis methodology
- [PSIJ Sensitivity] in IBIS
- [PSIJ Sensitivity] application
- Next Steps

Background

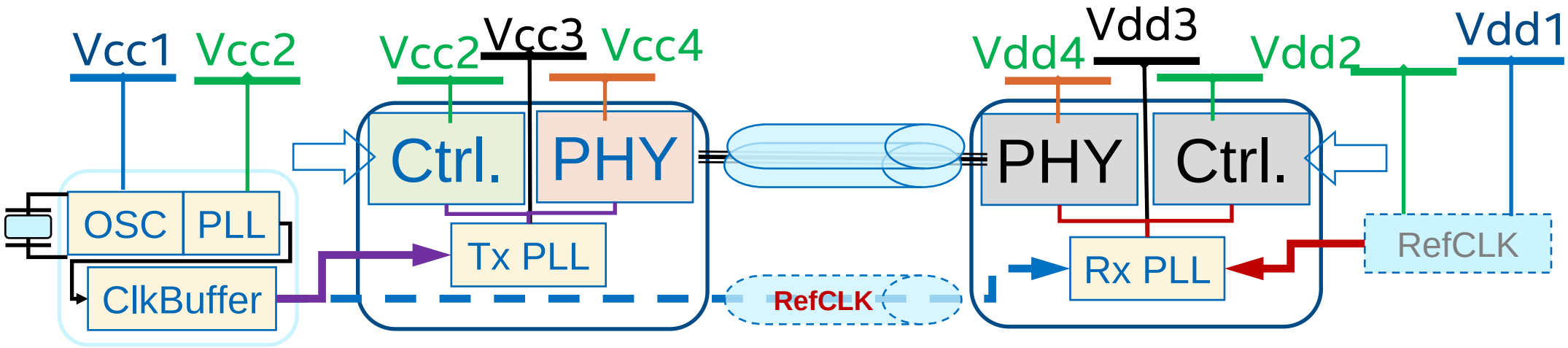
- Data speed-up => Less UI, less jitter budget
  - PCIe Gen3/4/5/6
  - LP(G)/DDR3/4/5/6
  - USB3/3.1/3.2/4, DP &THB

- Silicon Disaggregation => more complicated jitter implication
  - EMIB (Embedded Multi-die Interconnect Bridge), Foveros (Die to Die Stacking), and WoW (Wafer-on-Wafer)
  - Differentiated architecture

- Process evolution => lower operation voltage, less voltage margin
  - 22/14/10/7/6/5/4/3nm & 20A/18A

HSIO Architecture Example: Serial or Parallel

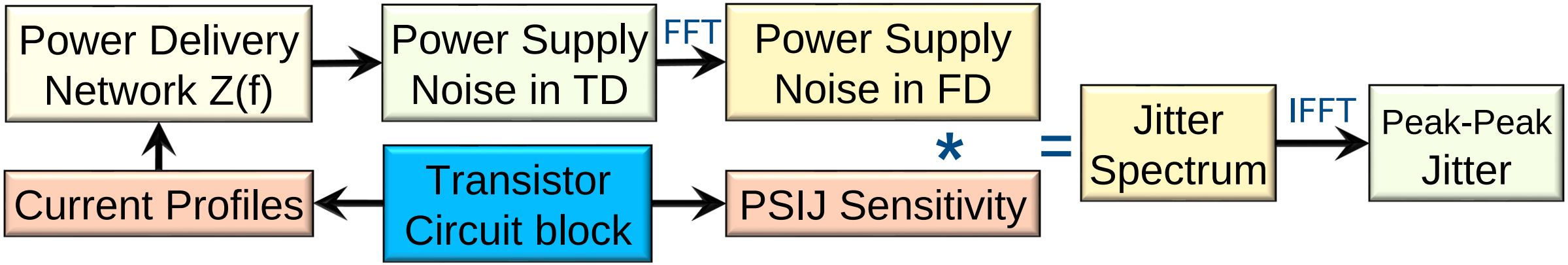
- HSIO Tx/Rx PHY with EQ, and CDR in Rx PHY
- HSIO jitter, from Data and Clock, common or independent RefCLK
- HSIO jitter, from SI & PI, of multiple power supplies' PDNs
- HSIO jitter, of Dj and Rj, in pp or rms



Status Quo, of Jitter Analysis

- SI & PI totally decoupled Sim, $Tj = Tj_{-SI} + Tj_{-PI}(+Tj_{-PM} + Tj_{-ctrl1} + \ldots)$
  - Over-design with direct superposition of the worst SI & PI cases in TD
    - PSIJ heavily frequency-dependent to each circuit block cascaded in the path
    - Jitter contribution from the other circuitry might not be included
    - Jitter contribution significantly different upon different process technology, even for same IP
- SI-PI Co-Sim, $Tj = Tj_{-Eye}(+Tj_{-PM} + Tj_{-ctrl1} + \ldots)$
  - Xtor model based, SI&PI co-sim,
    - very time-consuming, almost impossible to include all circuitry
  - Power-aware IBIS-AMI based sim
    - More efficient, but less accuracy
    - Jitter contribution from the other circuitry not included
  - PM noise needs lab verification

Jitter Analysis with PSIJ Sensitivity



- Tj = Dj + Rj
- Rj, unbounded, Gaussian distribution, characterized in rms upon BER
- Dj, comes from SI channel & PI noise

- $Dj_{-PI} = \sum_{i=1}^{N} IFFT[PSIJ_i * FFT(Vnoise_i)]$
- Dj_{-SI} from SI simulation, assuming ideal power supplies
- System total Dj, Dj=Dj-SI+Dj-PI

https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=4387157

PSIJ Sensitivity Derivation

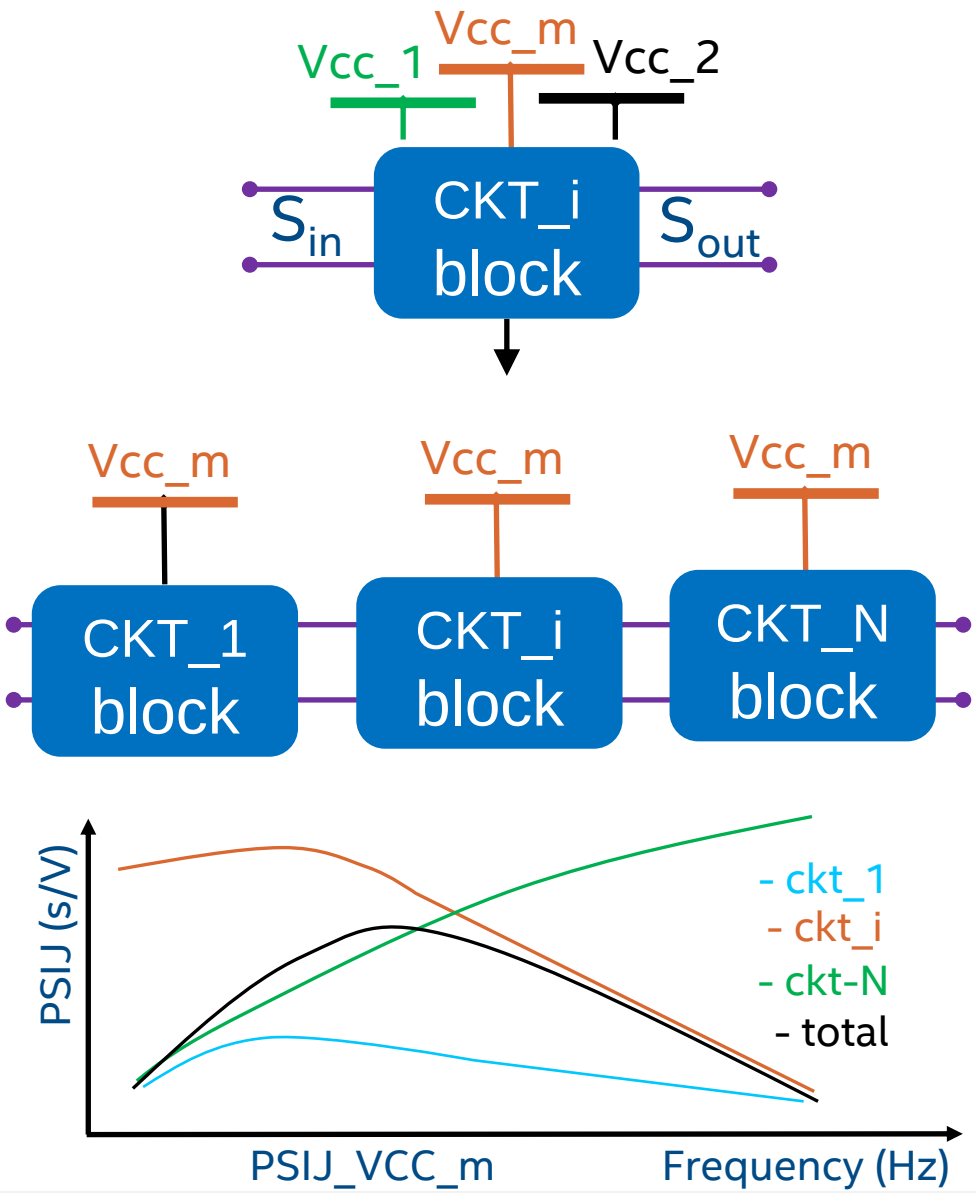
- Set up VCC_m= Vtyp+A*sin(f),
  - A=(Vmax-Vmin)/2,
  - Keep all other power supplies at their own Vtyp
- Observe jitter impact, while sweeping f, to get PSIJ_VCC_m_ckt_i

PSIJ_VCC_m= $\prod_{i=1}^{N} PSIJ\_VCC\_m\_ckt_i$ *or*

= $\sum_{i=1}^{N} PSIJ\_VCC\_m\_ckt_i$ *or*

= mix of $\prod_{i=A}^{B} X$ and $\sum_{j=C}^{D} Y$

- In equations, discrete {A, B, C, D} ={1, 2, …, N}, and
- X, Y could be any combinations of $PSIJ\_VCC\_m\_ckt_{i/j}$



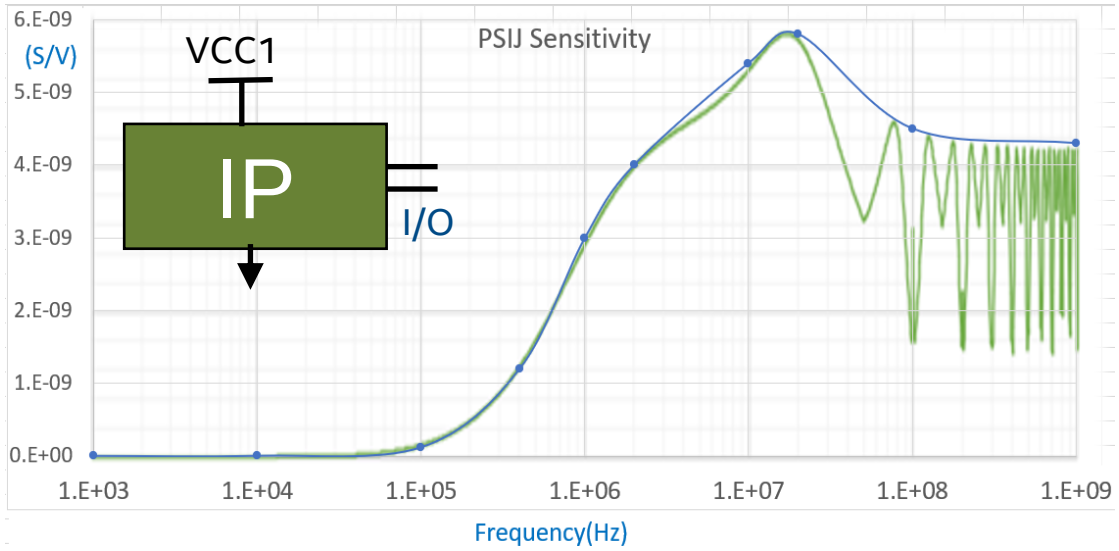
Proposal of [PSIJ Sensitivity] in IBIS

Keyword: [PSIJ Sensitivity]

Required: No. It is optional, unless [PSIJ Sensitivity] is defined for at least one power supply rail in an IO interface.

Description: This keyword describes the Power Supply Induced Jitter (PSIJ) sensitivity in PWL (Piece Wise Linear) format in the frequency domain for a power rail.

Usage Rules: PSIJ Sensitivity in PWL format, for each power rail listed in [Voltage List], to evaluate the jitter impact to all the circuit blocks from its power supplies' noise respectively.



Example:

```
[PSIJ Sensitivity Group] PCIe_Gen4
[PSIJ Sensitivity]  VCC2
| frequency(Hz)          sensitivity (s/V)
0                        1.00E-12
1.0E+03                  1.00E-12
1.0E+04                  2.00E-12
1.0E+05                  1.20E-10
4.0E+05                  1.20E-09
1.0E+06                  3.00E-09
2.0E+06                  4.00E-09
1.0E+07                  5.40E-09
2.0E+07                  5.80E-09
1.0E+08                  4.50E-09
1.0E+09                  4.30E-09
[End PSIJ Sensitivity] VCC2
| …
[PSIJ Sensitivity Group] PCIe_Gen4
```

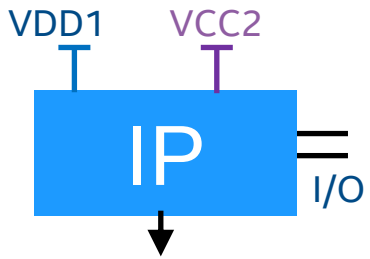
```
[Voltage List]
|V(name)     V(typ)     V(min)     V(max)
VCC1         1.000      0.900      1.100
VSS          0.000      0.000      0.000
[End Voltage List]
```

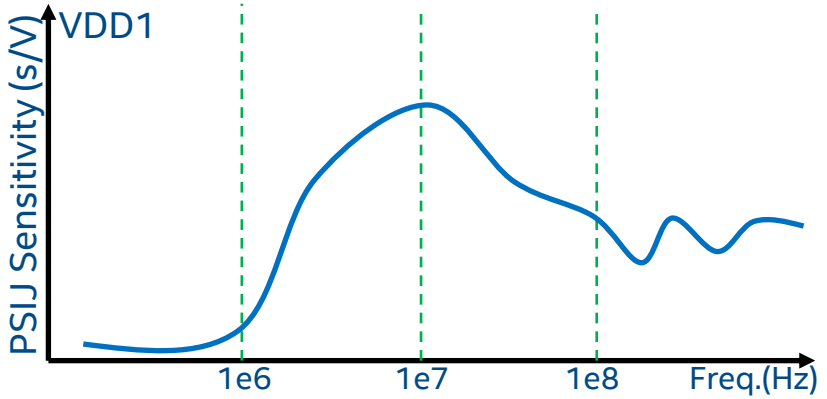
Examples of [PSIJ Sensitivity] in IBIS

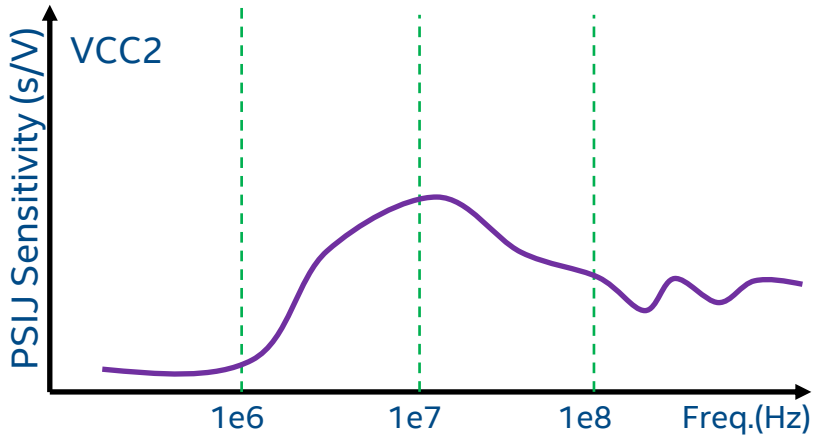
```
[PSIJ Sensitivity Group] DisplayPort
[PSIJ Sensitivity]  VDD1
| frequency(Hz)     sensitivity (s/V)
0                   1.0e-9
10,000              1.0e-9
100,000             1.1e-9
1,000,000           2.2e-9
10,000,000          7.8e-9
100,000,000         4.0e-9
1,000,000,000       3.9e-9
[End PSIJ Sensitivity] VDD1

[PSIJ Sensitivity]  VCC2
| frequency(Hz)     sensitivity (s/V)
0                   2.0p
10,000              2.0p
100,000             2.7n
1,000,000           3.0n
10,000,000          4.9n
100,000,000         4.1n
1,000,000,000        3.8n
[End PSIJ Sensitivity] VCC2
[PSIJ Sensitivity Group] DisplayPort

[Voltage List]
|V(name)     V(typ)     V(min)     V(max)
VDD1         1.800      1.710      1.890
VCC2         0.600      0.540      0.660
VSS          0.000      0.000      0.000
[End Voltage List]
```

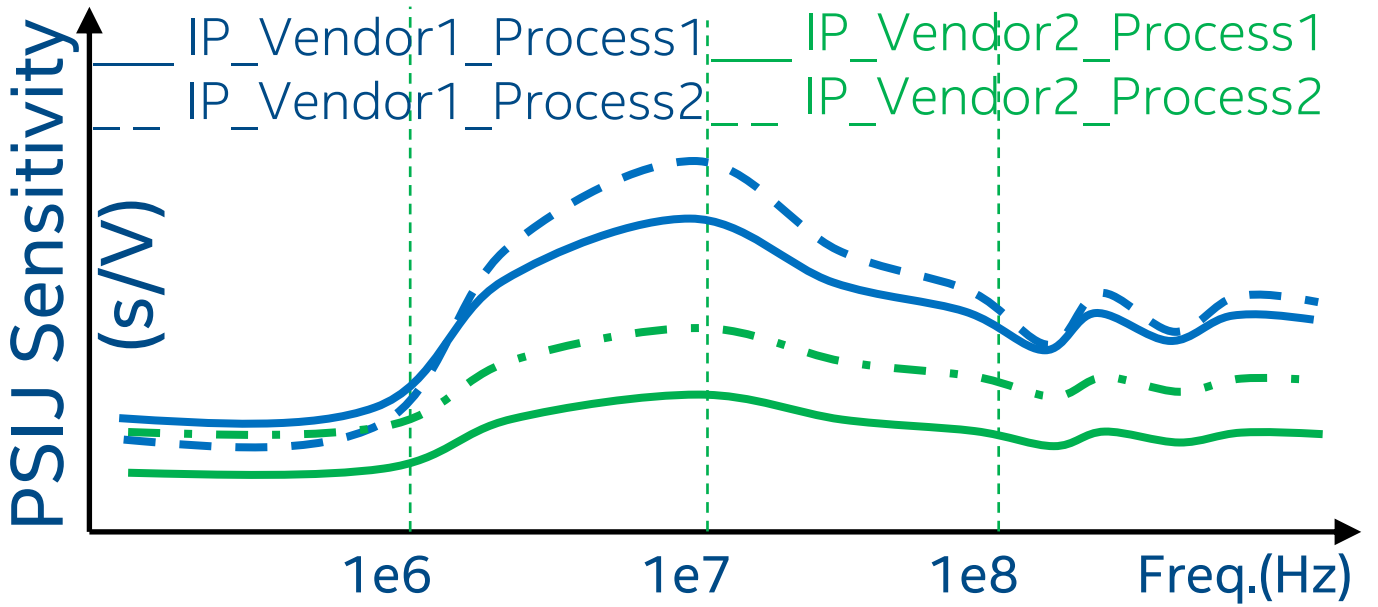






Quick IP Selection, based upon [PSIJ Sensitivity]

- Same IP is better:
  - from vendor2 than
  - from vendor1
- Same IP is better:
  - upon process1 than
  - upon process2
- Same IP is the best
  - from vendor2 and
  - upon process1.



Next Steps

- Submit IBIS BIRD to include [PSIJ Sensitivity] in IBIS.
- Call for EDA vendors to support [PSIJ Sensitivity] in IBIS
- Call for chip vendors to support [PSIJ Sensitivity] in IBIS
- Call for platform designers to support [PSIJ Sensitivity] in IBIS

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