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Using IBIS-AMI for DDR5 applications

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Outline

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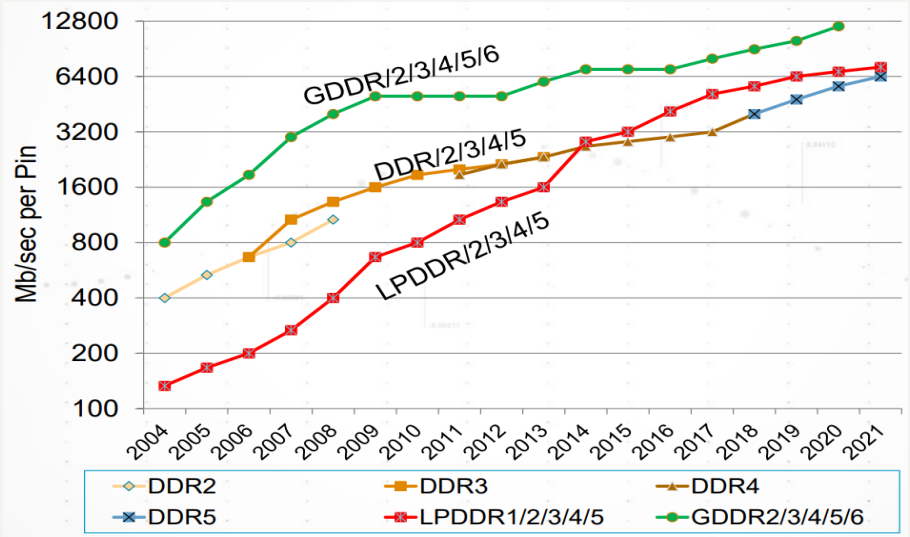
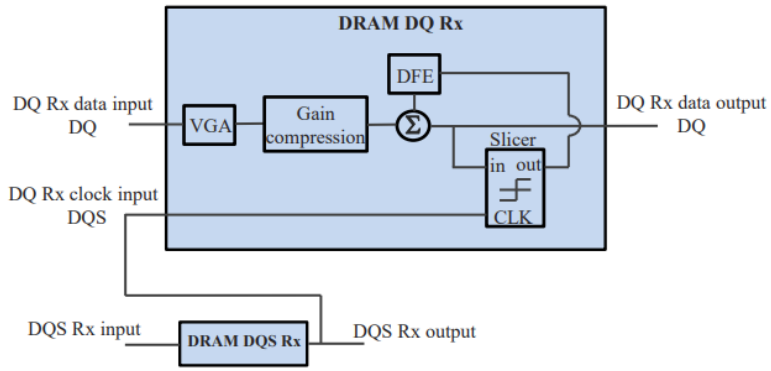
  - II: AMI Reserved Parameter: DC_offset
  - III: IBIS 7.1 standard mentions clock jitter based DDR5
  - IV: Significant SSN analysis
- Summary

Background: Challenges in IBIS-AMI Analysis of DDR5

JEDEC DDR Generations				
	DDR5	DDR4	DDR3	LPDDR5
Max Die Density	64 Gbit	16 Gbit	4 Gbit	32 Gbit
Max UDIMM Size	128 GB	32 GB	8 GB	N/A
Max Data Rate	6.4 Gbps	3.2 Gbps	1.6 Gbps	6.4Gbps
Channels	2	1	1	1
Width (Non-ECC)	64-bits (2x32)	64-bits	64-bits	16-bits
Banks (Per Group)	4	4	8	16
Bank Groups	8/4	4/2	1	4
Burst Length	BL16	BL8	BL8	BL16
Voltage (Vdd)	1.1v	1.2v	1.5v	1.05v
Vddq	1.1v	1.2v	1.5v	0.5v





- ✓ Faster Speed (3200MT/s to 6400MT/s)
- ✓ Equalizer (FIR,CTLE and DFE) requirement for DDR5,LPDDR5 and GDDR6.
- ✓ Asymmetric raise and fall edges in single-end signals
- ✓ Clock forwarding and jitter tracking in both controller and DRAM side
- ✓ With the development of new technologies such as 3D-IC and equalization, the SI/PI problem tends to become more complex and the design difficulty increases

AMI simulation tools needs to be extended

Basic IBIS

- No support DDR5 with Equalization

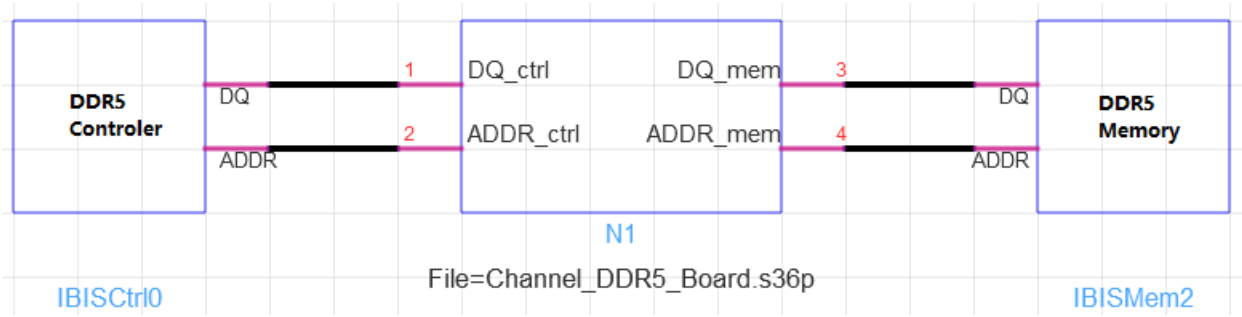
IBIS-AMI

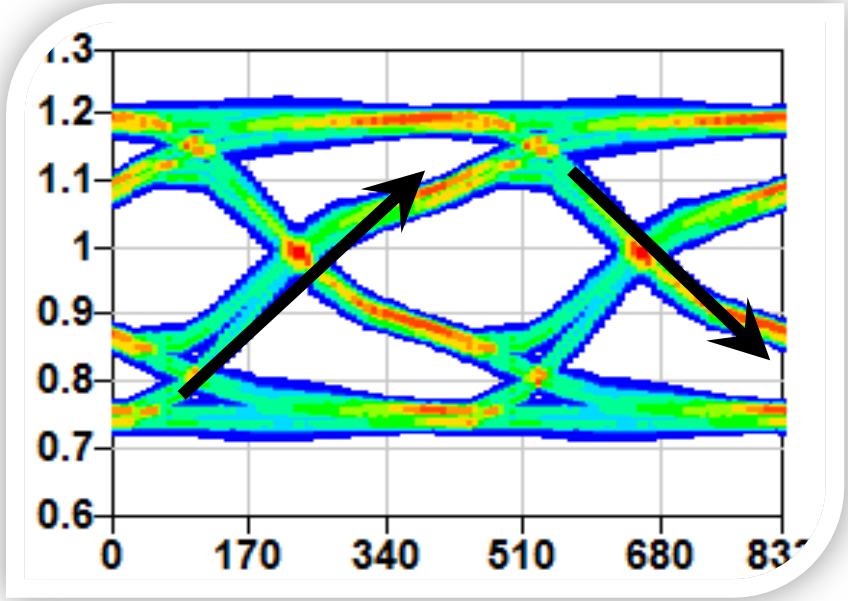
- Support Equalization
- Don’t support PDN effects
- Only support Differential Signal
- Only for point to point
- Don’t support external clock

New IBIS-AMI for DDR5 need

- Equalizer (FIR,CTLE and DFE) requirement for DDR5,LPDDR5 and GDDR6.
- Asymmetric raise and fall edges in single-end signals
- GetWave clock input for forwarded clocking
- IBIS-AMI standard needs to be extended to support DC offset in single-ended signaling.

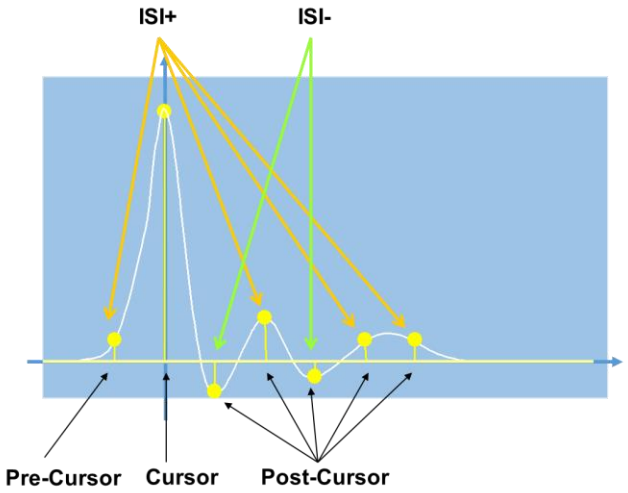
DER in bit-by-bit is a more accurate way to simulate asymmetrical signal edges

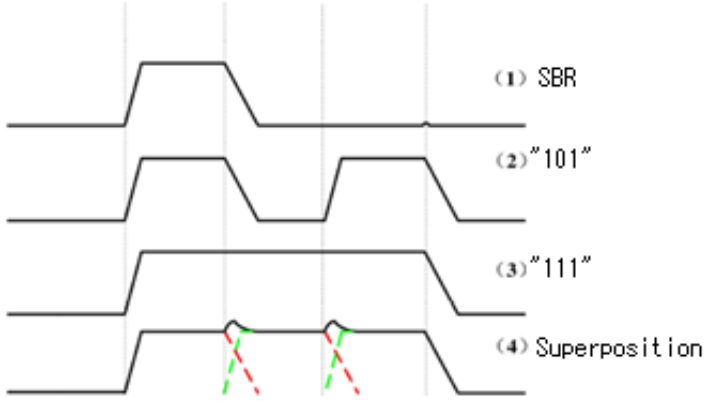


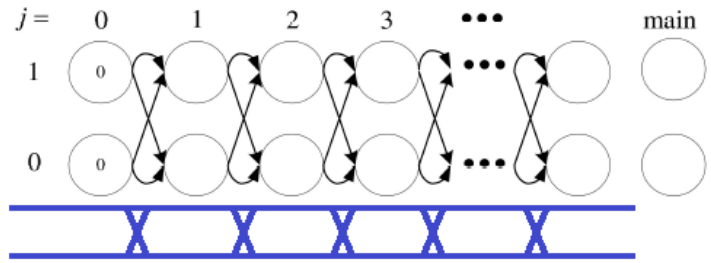


- Rise Time ≠ Fall Time
- Worst Cross and voltage level of voltage and timing
- In SerDes channels, the rising edge and falling edge of differential signal are symmetrical, so only a single step response is needed for channel simulation
- For a single ended signal, there are two step responses, rise and fall, need to be obtained simultaneously.
- At the same time, the simulator needs to use the corresponding step response to calculate when the signal rises and falls

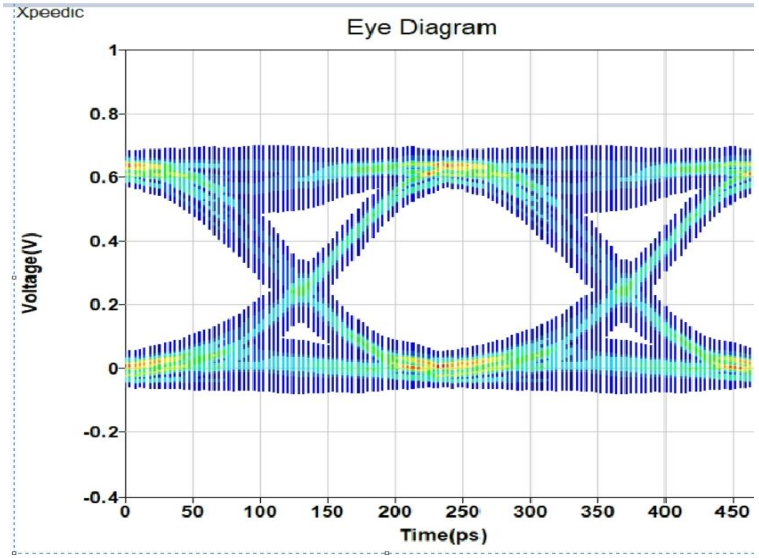
DER to deal with Asymmetric rise and fall edges





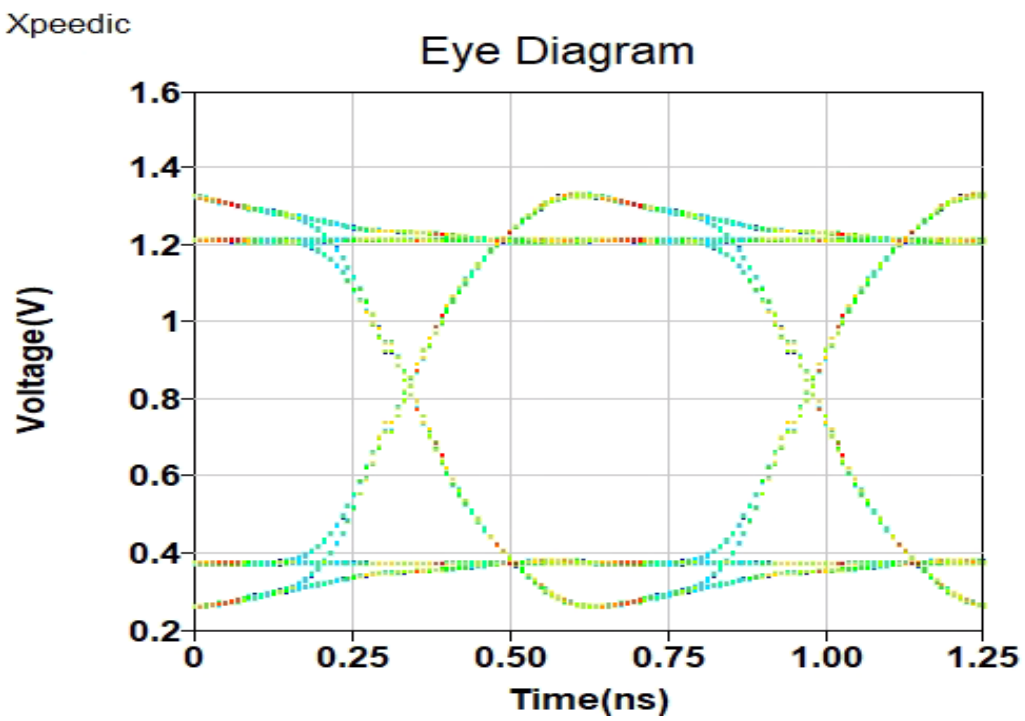


- SBR
- DER

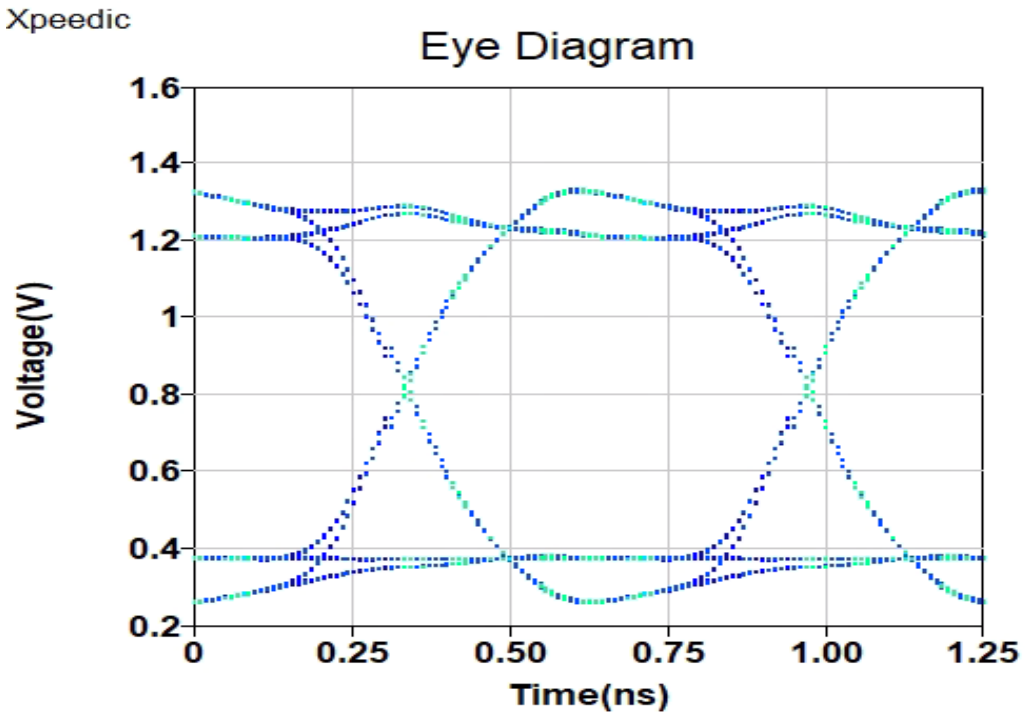


- The rise and fall step responses need to be obtained.
- DER algorithms are developed to capture the difference between rise and fall waveforms

PDA method Result Comparison



SBR



DER

- DER algorithms are developed to capture the difference between rise and fall waveforms

AMI Reserved Parameter: DC_offset

- Resolved in BIRD197.7 with the introduction of a new reserved parameter: DC_Offset
  - DC offset is an offsetting of a signal from zero

Parameter: **DC_Offset**

Required: No, and illegal before AMI_Version 7.1

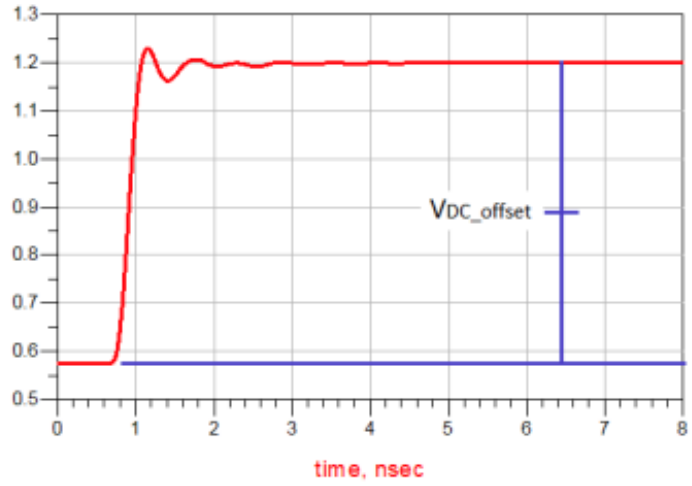
Direction: Rx

Descriptors:

Usage:	In
Type:	Float
Format:	Value
Default:	<numeric_literal>
Description:	<string>

Definition: The input value of DC Offset is the mean value of the steady state high and low voltages of the analog channel step response at the Rx pad.

Usage Rules: If the impulse response was generated by differentiating the analog channel step response, then the input value of DC Offset should be the same as the average of the step response initial and final voltages.



AMI Reserved Parameter: DC_offset

- New reserved parameter: DC_Offset in BIRD197.7
- How to remove DC Offset:
  - 1, Get the step response curve of each channel by Transient simulation;
  - 2, Extract high and low level signal in step response curve (V_high, V_low);
  - 3, V_dc_offset=(V_high + V_low)/2;

:;

Parameter: **DC_Offset**

Required: No, and illegal before AMI_Version 7.1

Direction: Rx

Descriptors:

Usage:	In
Type:	Float
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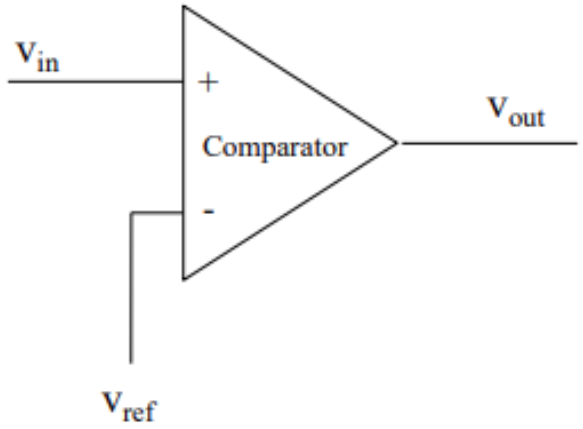
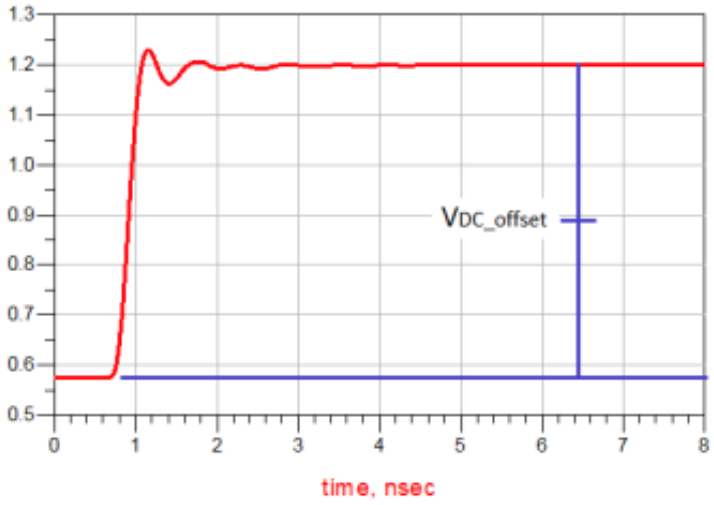
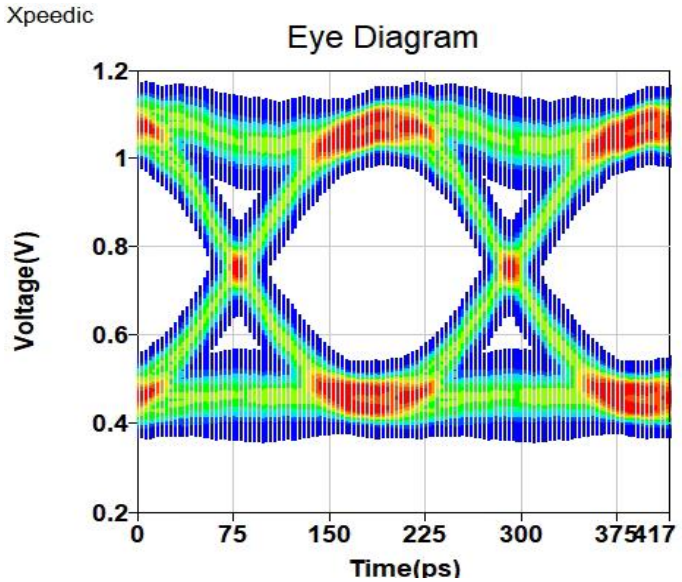
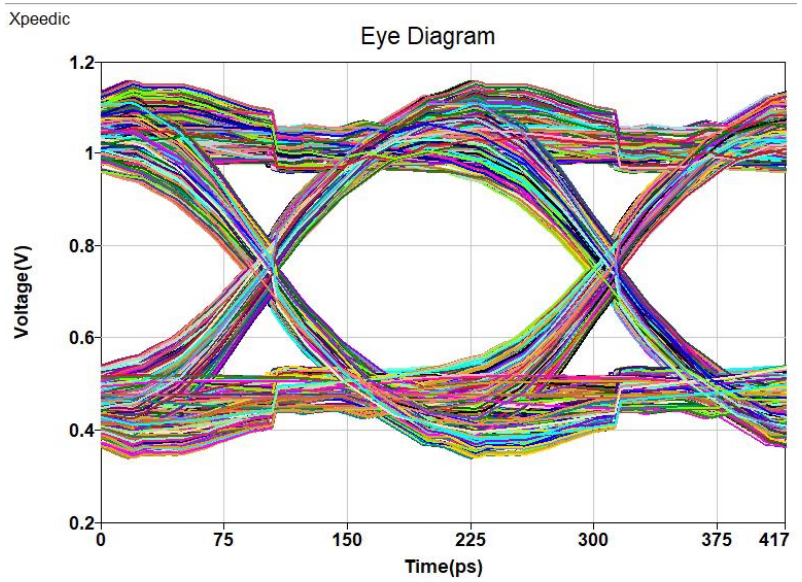




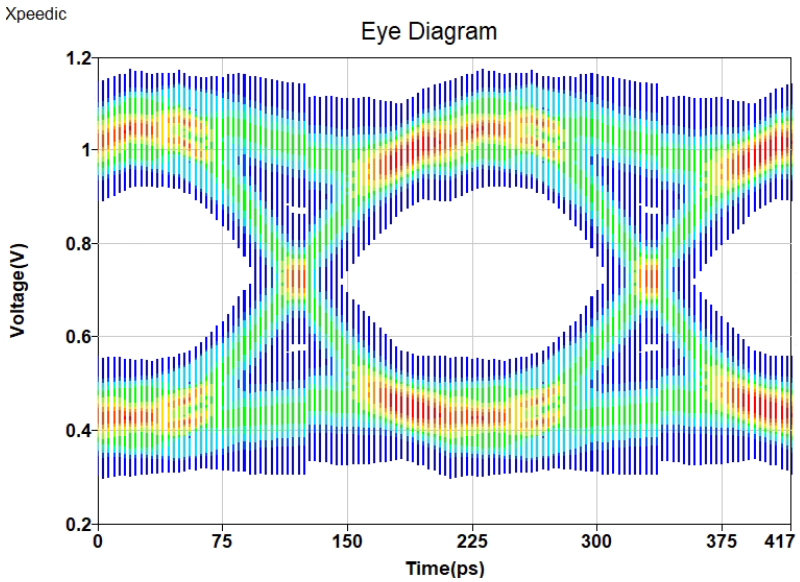
Eye Diagram with DC_offset



Eye Diagram without EQ



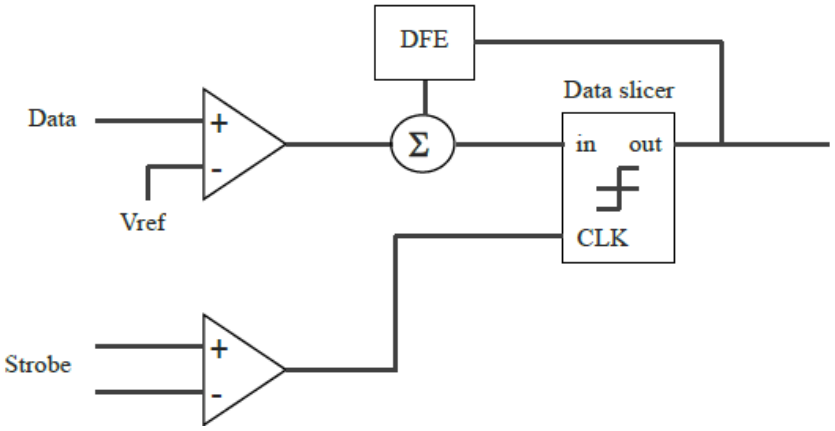
Stateye Diagram with EQ



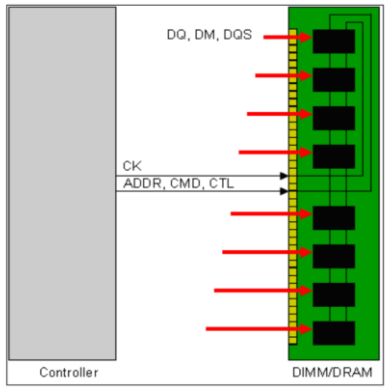
Stateye Diagram with EQ

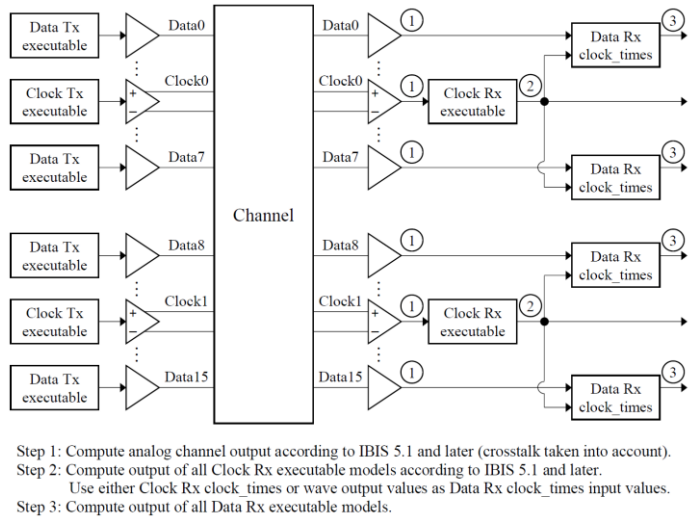
- Need to add DC_offset when to do Statistical eye simulation and bit-by-bit simulation;

IBIS 7.1 standard mentions clock jitter based DDR5



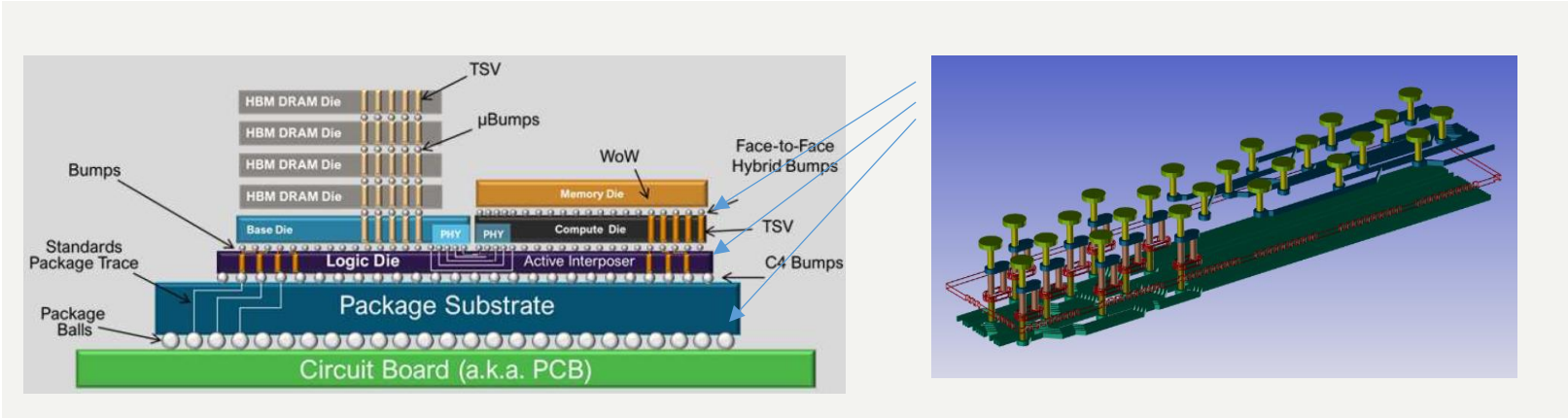
- Controller Delays DQ signals internally
- DQ & DQS signals are sent “Level” with the Addr/CLK

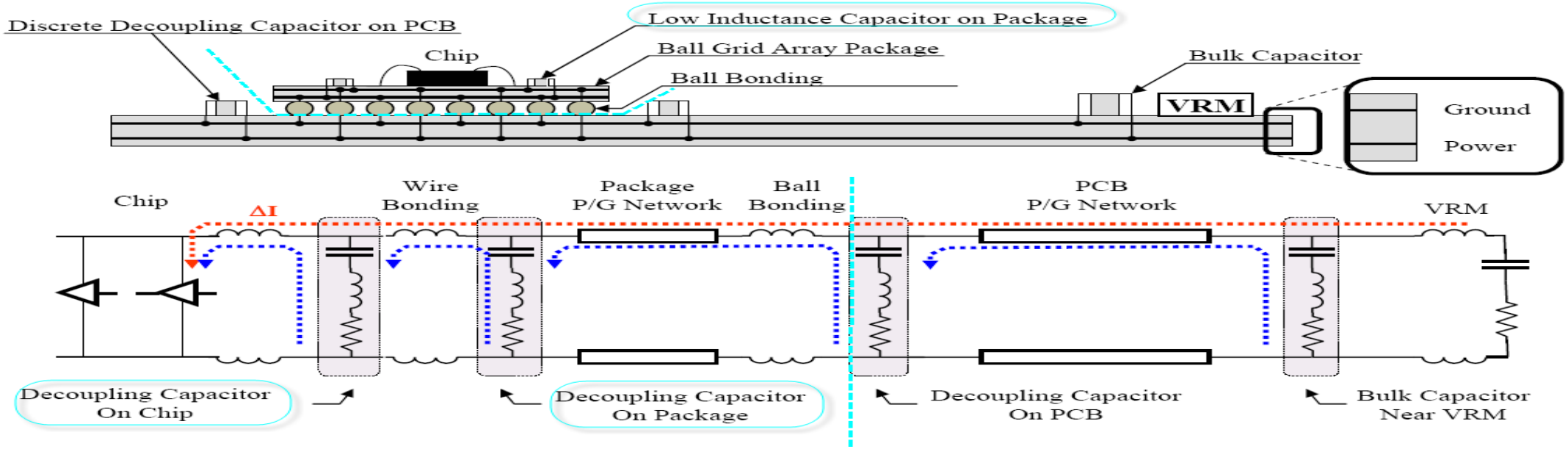




- SERDES signal usually recovers the clock signal from the signal itself through the clock and data recovery (CDR).
- DQ signal is triggered by DQS signal
- The clock input is the DQS Rx output
- Data DFE and sampling are clocked by DQS

Significant SSN analysis



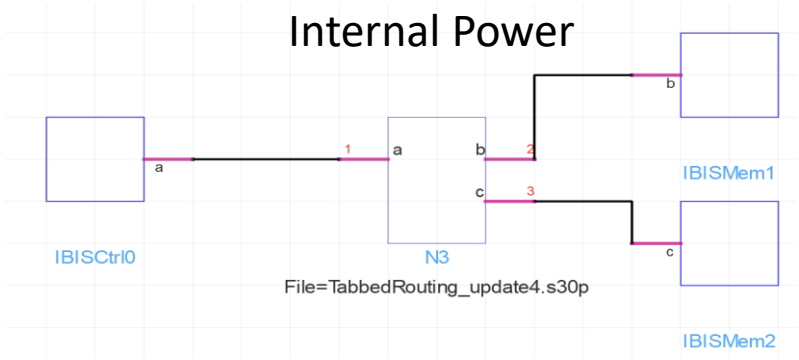


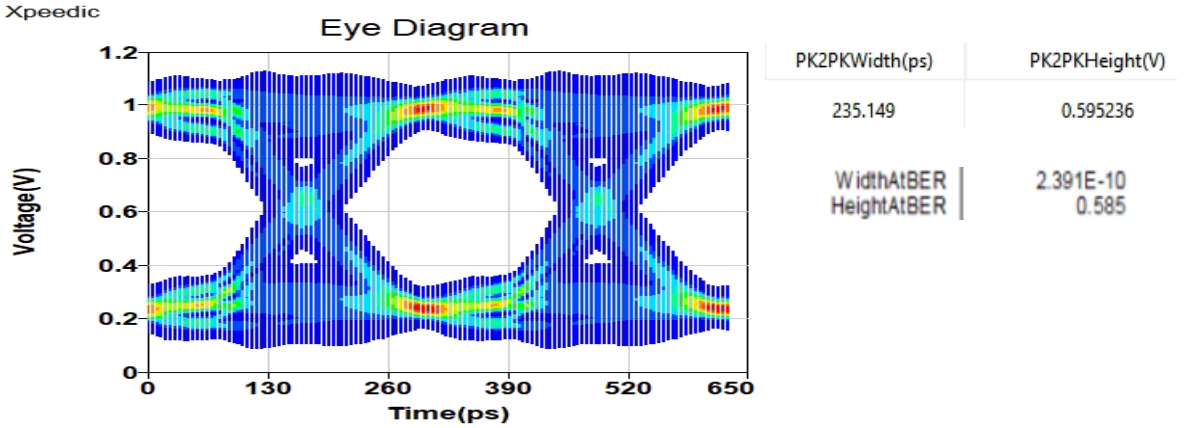
Eye-diagram Analysis with power noise

- Load Noise
  - Caused by Current Change by chips
  - Frequency Band: Under KHz
- Regulator Noise (Ripple Noise)
  - From power circuit Regulator LPF
  - Frequency Band: Under KHz
- Switching Noise
  - Coupled with VRM Phase Signal
  - Frequency Band: Several Hundred MHz
- White Noise:
  - From Resonance, Reflection, Radiation, Measurement equip
  - Frequency Band: Several Hundred MHz-GHz

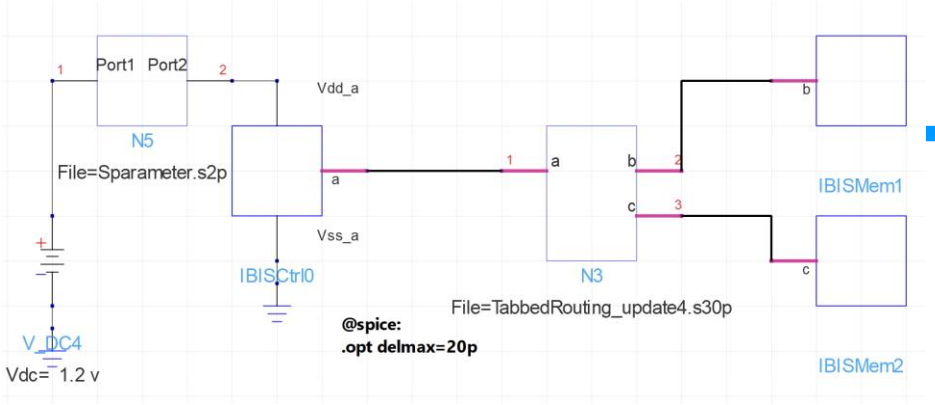
SSN: IBIS simulation result with external PDN effect

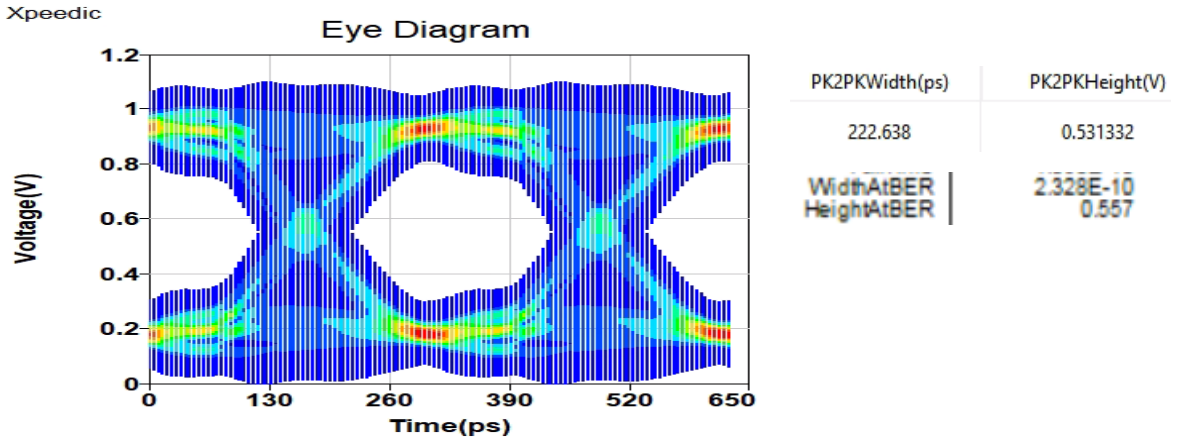
Internal Power





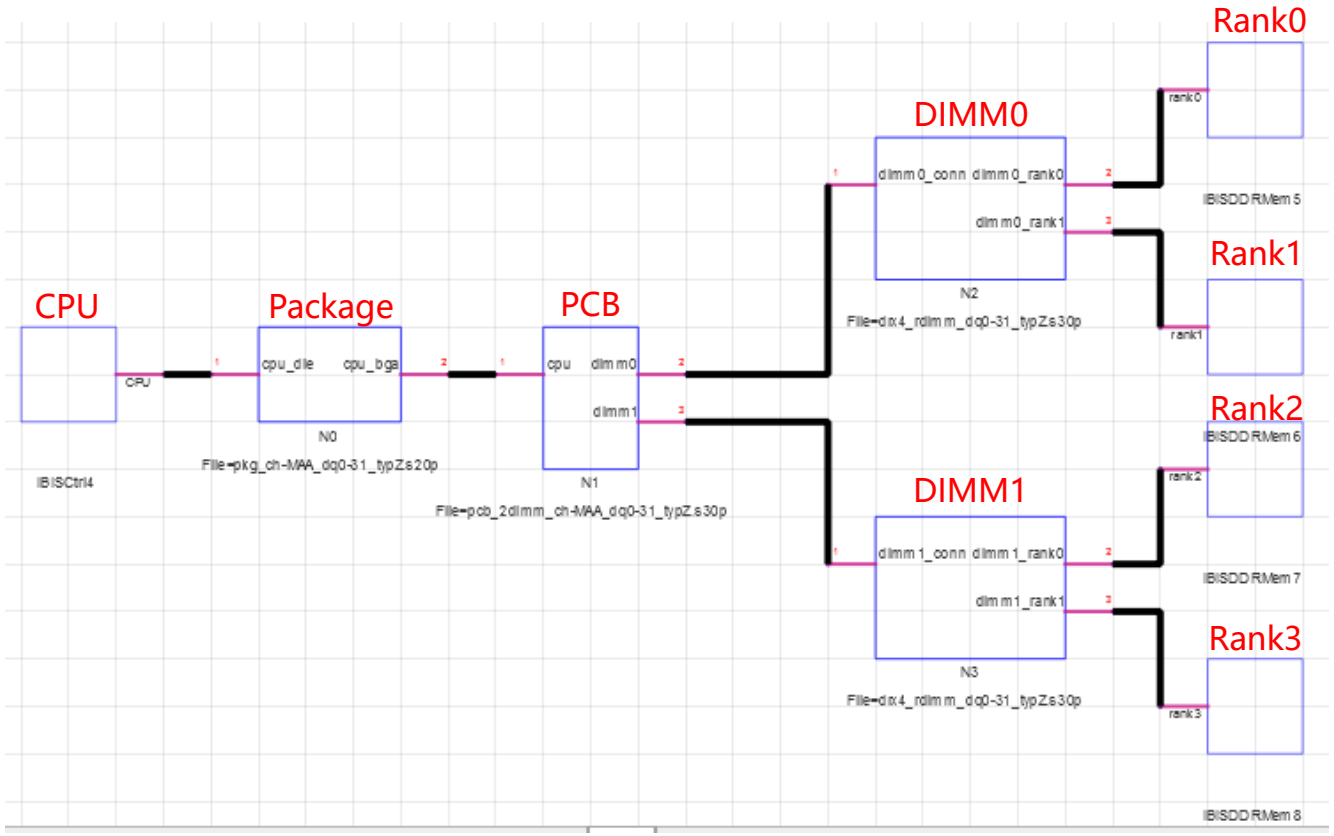
External Non-ideal Power





Eye Width : -13ps
Eye Height : -8mV

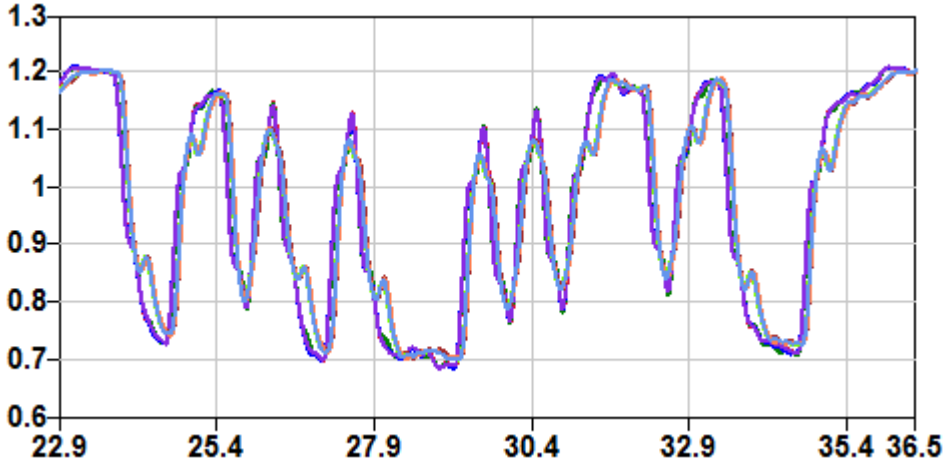
DDR5 simulation result

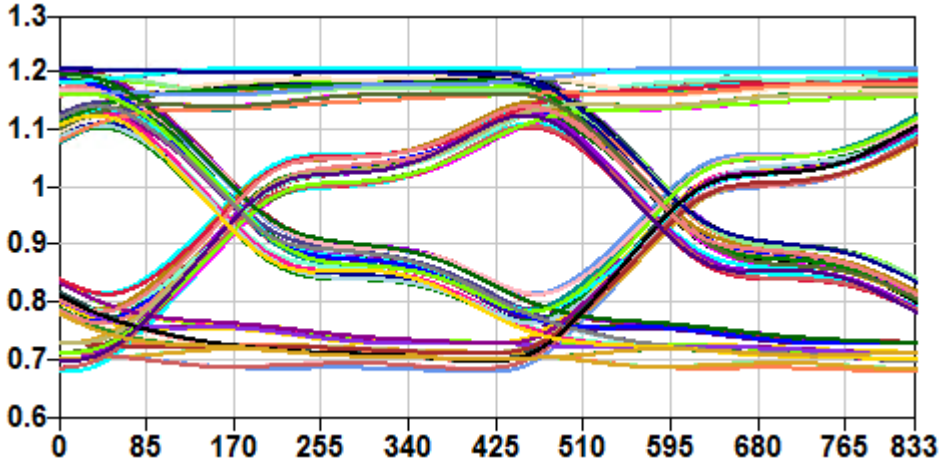


- Include S-parameter of CPU package;
- Include S-parameter of PCB transmission line (2-Slot);
- Include S-parameter of DIMM;
- Write signal: Rank ODT48 and Rank ODT240;
- Read signal: CPU ODT48, Rank ODT240;

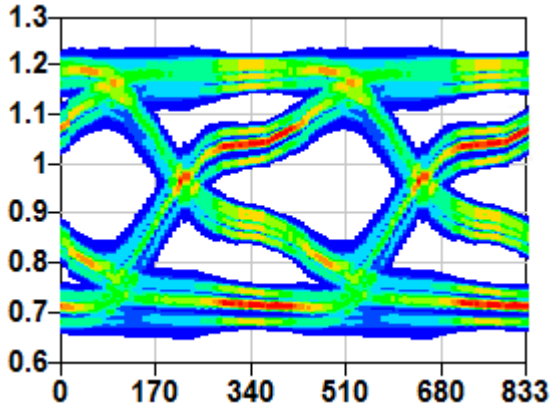
DDR5 simulation result

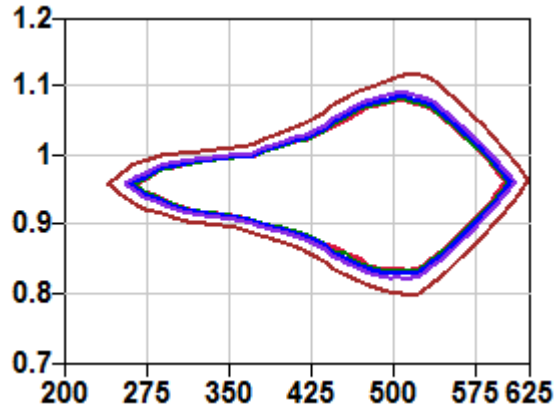
Bit-by-bit





Stateye





Stat Eye Summary

Name	Width(ps)	Height(V)
ibisddrmem8_...	332.022	0.243013
ibisddrmem8_...	328.67	0.241945
ibisddrmem8_...	320.977	0.236149
ibisddrmem8_...	329.574	0.24244
ibisddrmem8_...	292.916	0.149968
ibisddrmem8_...	284.25	0.152847
ibisddrmem8_...	284.89	0.16389
ibisddrmem8_...	284.709	0.159179

OK

Summary

- DER algorithms are developed to capture the difference between rise and fall waveforms
- Remove and restore DC Offset to solver DQ with EQ/DFE
- To enable modeling of clock forwarding, Rx AMI_GetWave API is extended to take both data and clock input waveforms
- Analyze DDR signal quality using SSN simulation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