Bandwidth Analysis of 224 Gb/s Serial Links

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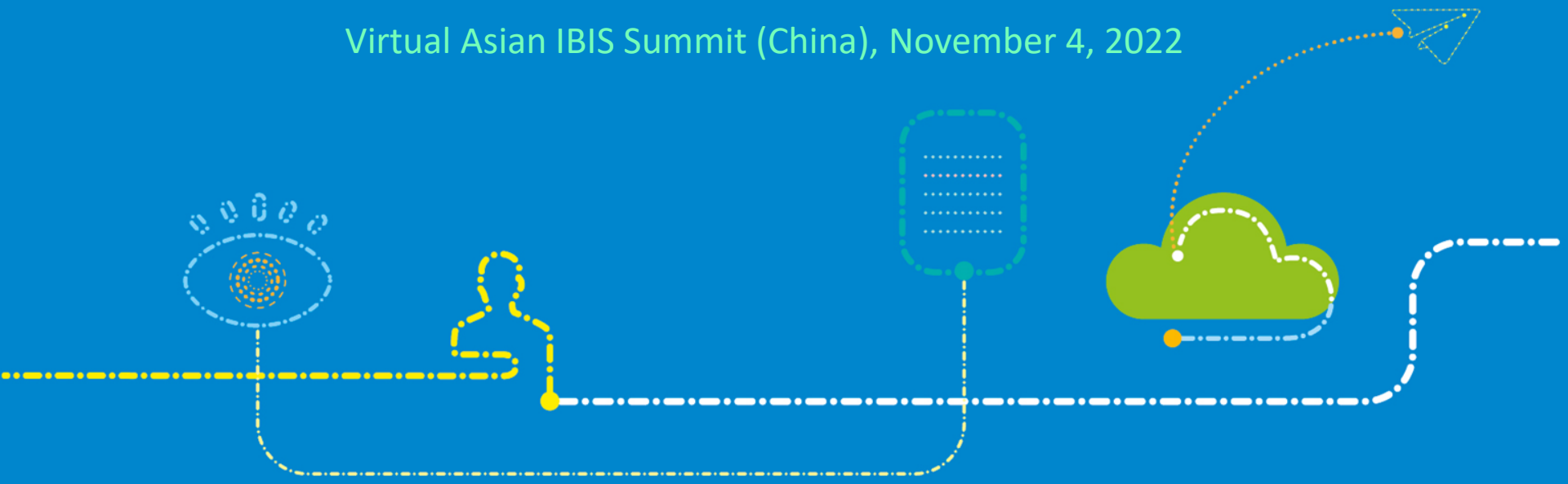
Virtual Asian IBIS Summit (China), November 4, 2022



Outline

- Overview
- Analysis Method
- Simulation on 224 Gb/s per Lane
- Summary

Increasing Bandwidth is Challenging

- Bandwith of system components increases with data rate, keeping increasing bandwidth is very challenging in next generation high-speed serial interconnection.

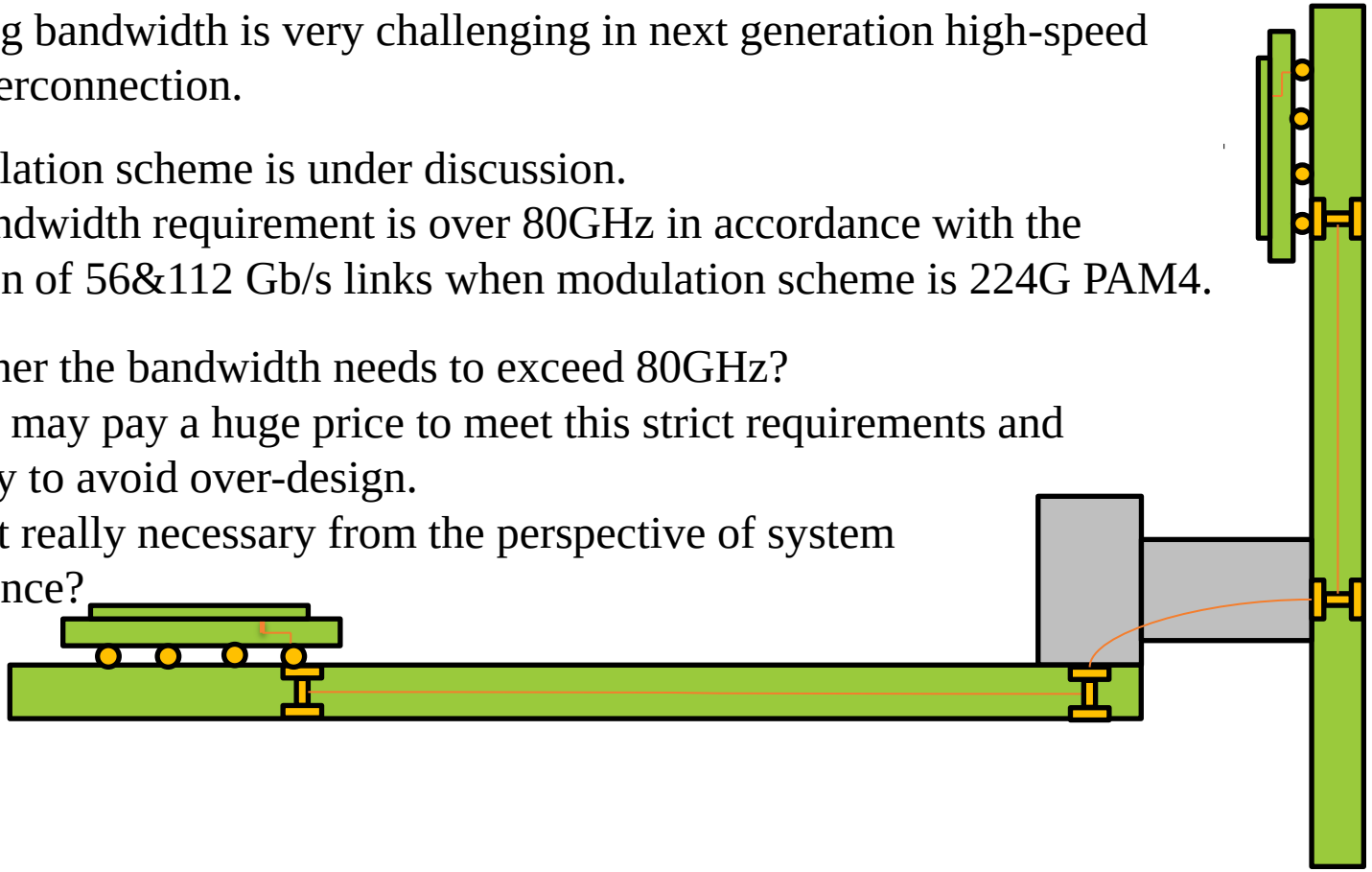
- Modulation scheme is under discussion.

  -Bandwidth requirement is over 80GHz in accordance with the evaluation of 56&112 Gb/s links when modulation scheme is 224G PAM4.

- Whether the bandwidth needs to exceed 80GHz?

  -We may pay a huge price to meet this strict requirements and should try to avoid over-design.

  -Is it really necessary from the perspective of system performance?



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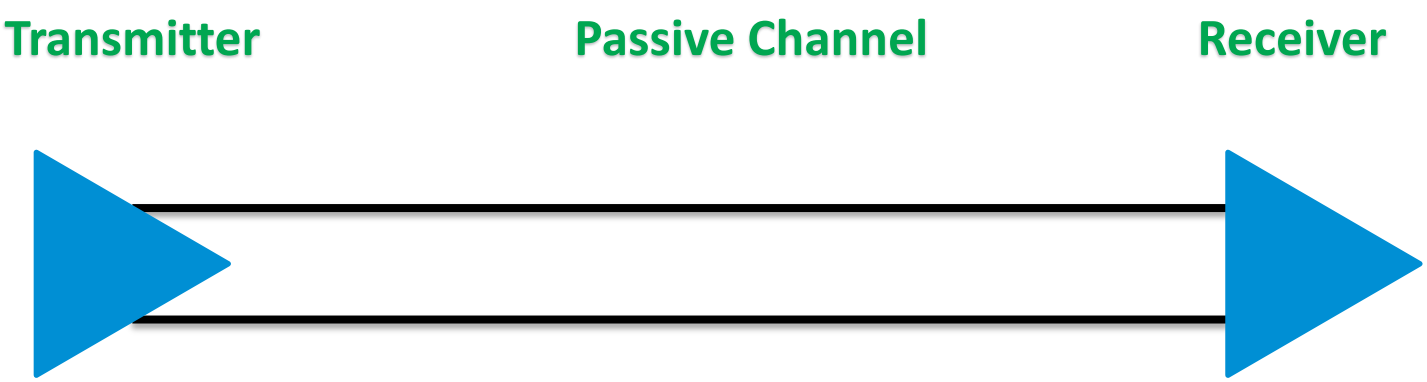
Whole Analog Channel Matters

- The performance of whole system is related with analog channel (passive channel, analog parts of transmitter and receiver), designer should pay attention to these parts at the same time.



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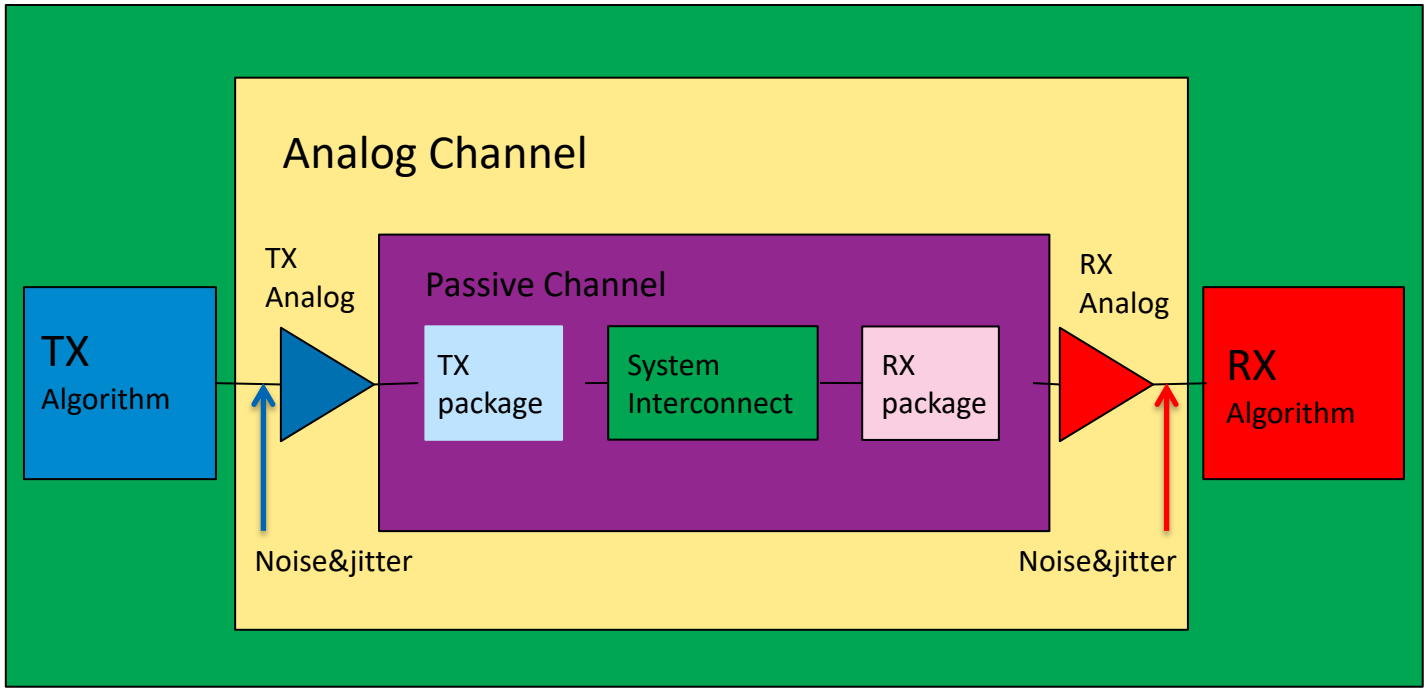
Self-built Model

- Analog channel
  -Passive channel and TX&RX analog
- Algorithmic model
  -TX &RX algorithm, noise&jitter



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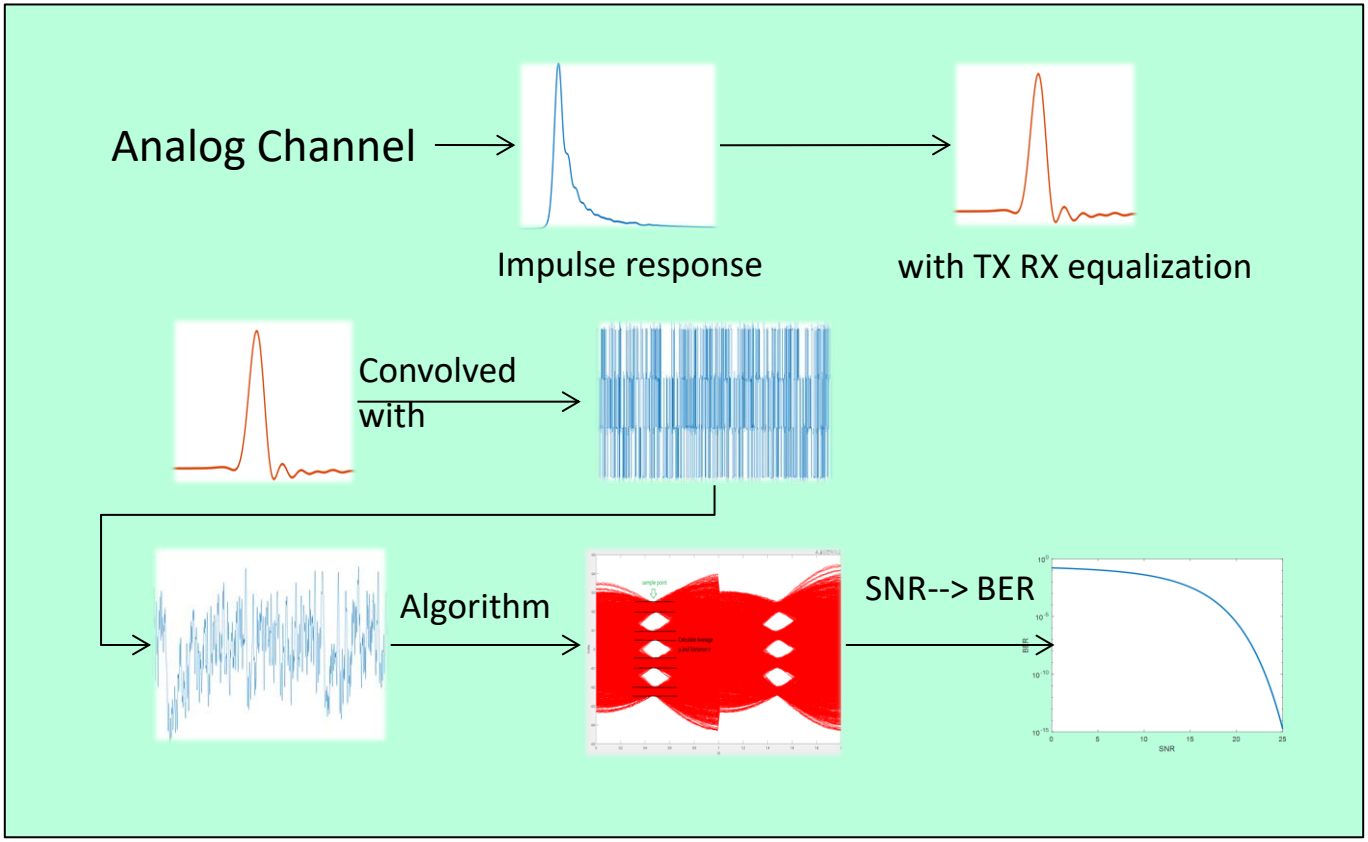
Time-domain Simulation Flow

- As shown in the figure below, it is quite similar to IBIS-AMI time-domain simulation flow.



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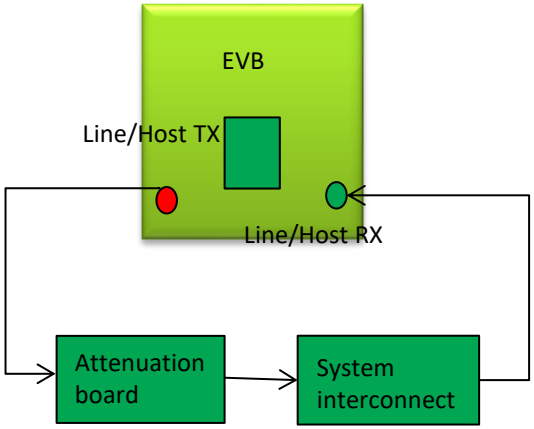
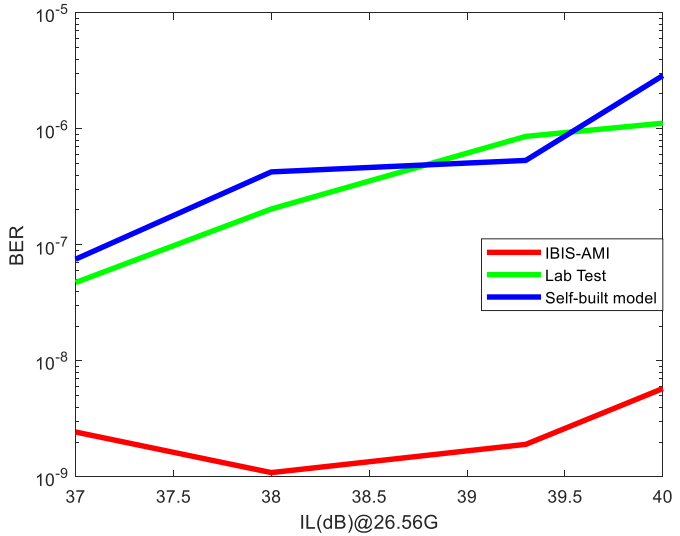
Lab&Simulation -112 Gb/s Links



sketch map of lab test environment



- With lab test data as reference, the self-built model has better accuracy than the simulation data of IBIS-AMI.
- Based on self-built model, parameters are modified to analyze 224 Gb/s links.

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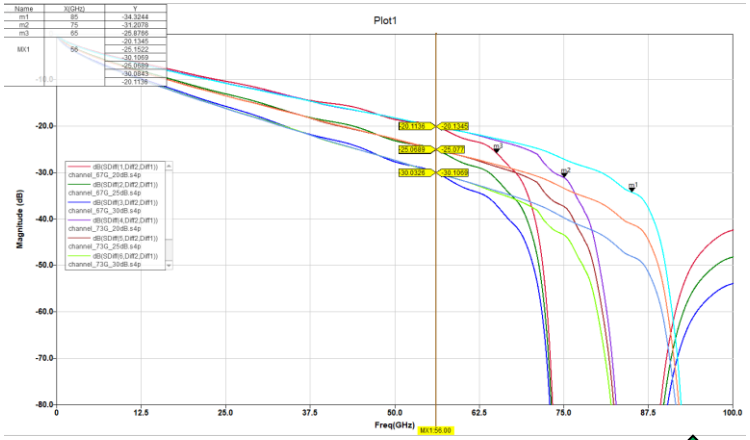
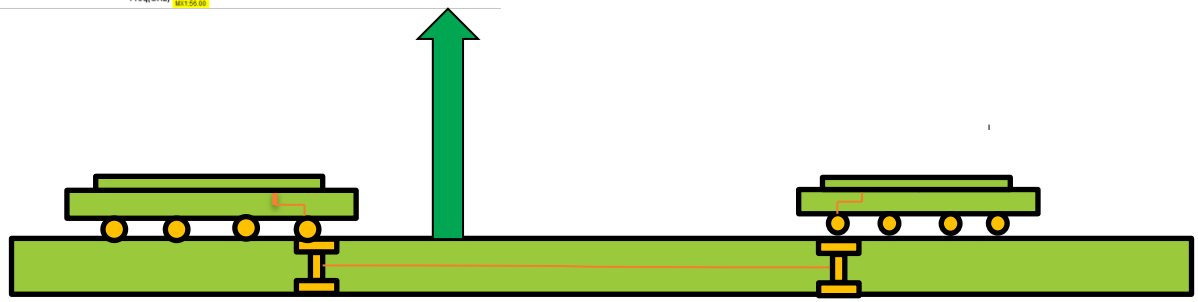
224G Passive Channel

- Since the bandwidth of connector is difficult to exceed 80GHz, only transmission line, via and BGA breakout are used to build 224G channels to eliminate the impact of other factors on the simulation results.



- BGA Via
- Transmission line
- Different bandwidth



*Only through channel.
*Through channel does not include connector as shown in the figure.

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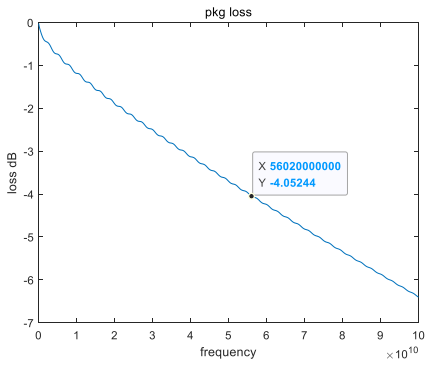
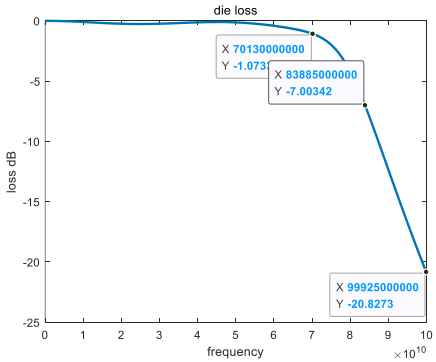
TX/RX Analog

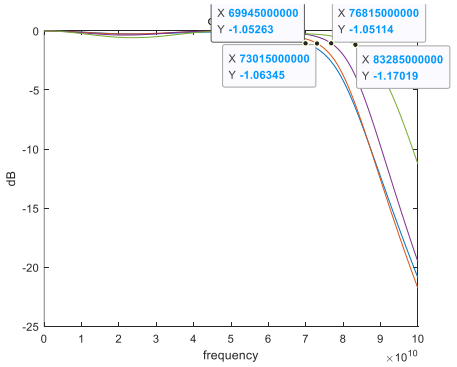
- Package model



- Die model



- Different TX/RX analog bandwidth



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Simulation Results

AFE bandwidth	SNR	BER
60G	18.75	3.81e-5
70G	20.3	1.48e-6
74G	20.48	9.34e-7
78G	20.56	7.71e-7
84G	20.18	1.97e-6

- Channel bandwidth around 80G
- Passive channel inertion loss 25dB@56G

AFE bandwidth	SNR	BER
60G	18.07	1.16e-4
70G	20.18	2.00e-6
74G	20.36	1.28e-6
78G	20.35	1.30e-6
84G	19.98	3.16e-6

- Channel bandwidth around 70G
- Passive channel inertion loss 25dB@56G

AFE bandwidth	SNR	BER
60G	Null	Null
70G	16.65	7.29e-4
74G	16.77	6.43e-4
78G	16.80	6.19e-4
84G	17.16	4.03e-4

- Channel bandwidth around 60G
- Passive channel inertion loss 25dB@56G

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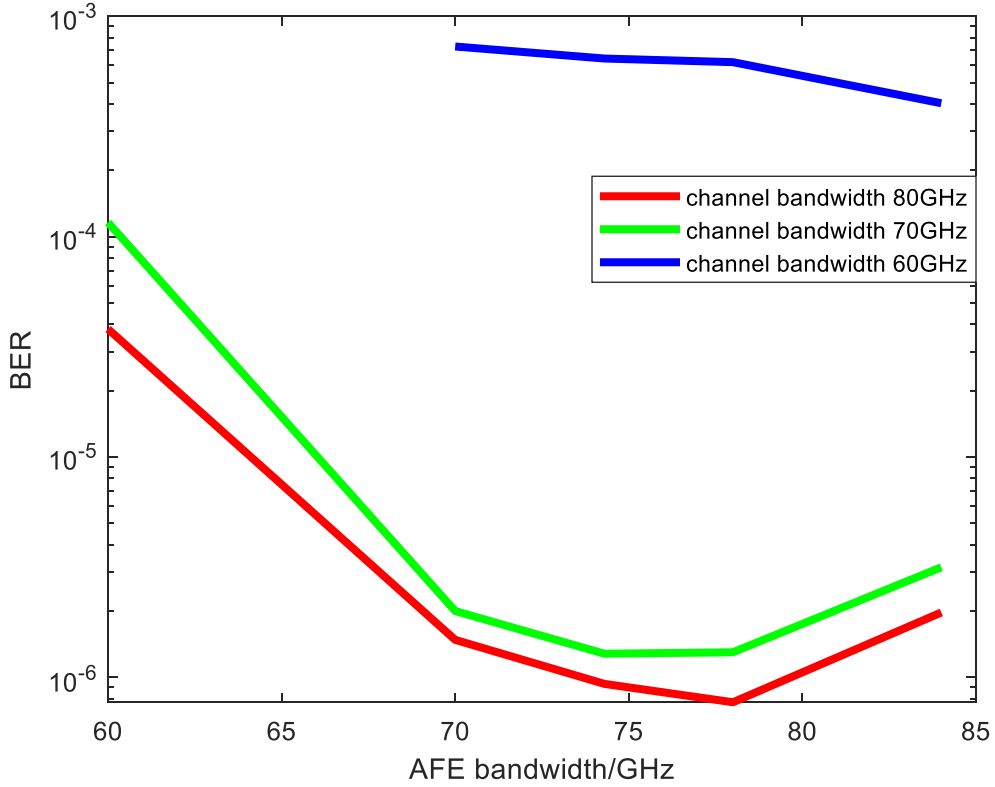
Simulation Results



- Poor system performance when analog channel's bandwidth is insufficient.
- System performance does not always get better when analog channel bandwidth goes higher.

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- Need to increase bandwidth, but there is a limit
  - System bandwidth needs to go higher to meet data rate, but simulation results do not get better when bandwidth increases beyond a specific value.

- Background noise matters
  -There is an inflection point at certain frequency which is related with background noise. Noise energy may increase more than the signal energy under specific background noise.

- Need end-to-end evaluation
  -Next generation high-speed serial interconnection system faces a huge challenge and requires cooperation of different vendors as soon as possible.

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- Thank you !

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