[PSIJ Sensitivity] in IBIS

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Kinger drives CPU+ dGPU better together strategy in mobile platforms and leads strategic PI design tool evolution in Client Computing Group. Kinger was awarded Ph. D by Shanghai Jiao Tong University in 2001, and MBA degree by W.P. Carey business school in ASU in 2008. Kinger works in signal & power integrity domains for 20+ years. Kinger holds 12 granted patents, and published 30+ papers.
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Agenda

▪ Background
▪ HSIO architecture: Serial & Parallel
▪ Status Quo, for jitter analysis
▪ New system jitter analysis methodology
▪ [PSIJ Sensitivity] in IBIS
▪ [PSIJ Sensitivity] application
▪ Next Steps
Background

▪ Data speed-up => Less UI, less jitter budget
  • PCIe Gen3/4/5/6
  • LP(G)/DDR3/4/5/6
  • USB3/3.1/3.2/4, DP & THB

▪ Silicon Disaggregation => more complicated jitter implication
  • EMIB (Embedded Multi-die Interconnect Bridge), Foveros (Die to Die Stacking), and WoW (Wafer-on-Wafer)
  • Differentiated architecture

▪ Process evolution => lower operation voltage, less voltage margin
  • 22/14/10/7/6/5/4/3nm & 20A/18A
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HSIO Architecture Example: Serial or Parallel

- HSIO Tx/Rx PHY with EQ, and CDR in Rx PHY
- HSIO jitter, from Data and Clock, common or independent RefCLK
- HSIO jitter, from SI & PI, of multiple power supplies’ PDNs
- HSIO jitter, of Dj and Rj, in pp or rms
Status Quo, of Jitter Analysis

- SI & PI totally decoupled Sim, $T_j = T_{j_{SI}} + T_{j_{PI}} (T_{j_{PM}} + T_{j_{ctrl1}} + ...)$
  - Over-design with direct superposition of the worst SI & PI cases in TD
    - SIJ heavily frequency-dependent to each circuit block cascaded in the path
    - Jitter contribution from the other circuitry might not be included
    - Jitter contribution significantly different upon different process technology, even for same IP

- SI-PI Co-Sim, $T_j = T_{j_{Eye}} (T_{j_{PM}} + T_{j_{ctrl1}} + ...)$
  - Xtor model based, SI&PI co-sim,
    - very time-consuming, almost impossible to include all circuitry
  - Power-aware IBIS-AMI based sim
    - More efficient, but less accuracy
    - Jitter contribution from the other circuitry not included
  - PM noise needs lab verification
Jitter Analysis with PSIJ Sensitivity

- \( T_j = D_j + R_j \)
- \( R_j \), unbounded, Gaussian distribution, characterized in rms upon BER
- \( D_j \), comes from SI channel & PI noise
- \( D_{j-PI} = \sum_{i=1}^{N} \text{IFFT}[\text{PSIJ}_i * \text{FFT}(V_{noise_i})] \)
- \( D_{j-SI} \) from SI simulation, assuming ideal power supplies
- System total \( D_j \), \( D_j = D_{j-SI} + D_{j-PI} \)

https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=4387157
PSIJ Sensitivity Derivation

- Set up $VCC_m = Vtyp + A \times \sin(f)$,
  - $A = (V_{max} - V_{min})/2$,
  - Keep all other power supplies at their own $Vtyp$

- Observe jitter impact, while sweeping $f$, to get $PSIJ_{VCC_m_ckt_i}$

\[
PSIJ_{VCC_m} = \prod_{i=1}^{N} PSIJ_{VCC_m_ckt_i} \text{ or } \sum_{i=1}^{N} PSIJ_{VCC_m_ckt_i} \text{ or } \text{mix of } \prod_{i=A}^{B} X \text{ and } \sum_{j=C}^{D} Y
\]

- In equations, discrete \{A, B, C, D\} =\{1, 2, ..., N\}, and
- $X, Y$ could be any combinations of $PSIJ_{VCC_m_ckt_i/j}$
Proposal of [PSIJ Sensitivity] in IBIS

**Keyword:** [PSIJ Sensitivity]

**Required:** No. It is optional, unless [PSIJ Sensitivity] is defined for at least one power supply rail in an IO interface.

**Description:** This keyword describes the Power Supply Induced Jitter (PSIJ) sensitivity in PWL (Piece Wise Linear) format in the frequency domain for a power rail.

**Usage Rules:** PSIJ Sensitivity in PWL format, for each power rail listed in [Voltage List], to evaluate the jitter impact to all the circuit blocks from its power supplies' noise respectively.

**Example:**

[PSIJ Sensitivity Group] PCIe_Gen4

[PSIJ Sensitivity] VCC2

<table>
<thead>
<tr>
<th>frequency (Hz)</th>
<th>sensitivity (s/V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1.00E-12</td>
</tr>
<tr>
<td>1.0E+03</td>
<td>1.00E-12</td>
</tr>
<tr>
<td>1.0E+04</td>
<td>2.00E-12</td>
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<tr>
<td>1.0E+05</td>
<td>1.20E-10</td>
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<tr>
<td>4.0E+05</td>
<td>1.20E-09</td>
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<tr>
<td>1.0E+06</td>
<td>3.00E-09</td>
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<tr>
<td>2.0E+06</td>
<td>4.00E-09</td>
</tr>
<tr>
<td>1.0E+07</td>
<td>5.40E-09</td>
</tr>
<tr>
<td>2.0E+07</td>
<td>5.80E-09</td>
</tr>
<tr>
<td>1.0E+08</td>
<td>4.50E-09</td>
</tr>
<tr>
<td>1.0E+09</td>
<td>4.30E-09</td>
</tr>
</tbody>
</table>

[End PSIJ Sensitivity] VCC2

[PSIJ Sensitivity Group] PCIe_Gen4

[Voltage List]

<table>
<thead>
<tr>
<th>V(name)</th>
<th>V(typ)</th>
<th>V(min)</th>
<th>V(max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC1</td>
<td>1.000</td>
<td>0.900</td>
<td>1.100</td>
</tr>
<tr>
<td>VSS</td>
<td>0.000</td>
<td>0.000</td>
<td>0.000</td>
</tr>
</tbody>
</table>

[End Voltage List]
Examples of [PSIJ Sensitivity] in IBIS

[PSIJ Sensitivity Group] DisplayPort

[PSIJ Sensitivity] VDD1
<table>
<thead>
<tr>
<th>frequency(Hz)</th>
<th>sensitivity (s/V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1.0e-9</td>
</tr>
<tr>
<td>10,000</td>
<td>1.0e-9</td>
</tr>
<tr>
<td>100,000</td>
<td>1.1e-9</td>
</tr>
<tr>
<td>1,000,000</td>
<td>2.2e-9</td>
</tr>
<tr>
<td>10,000,000</td>
<td>7.8e-9</td>
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<tr>
<td>100,000,000</td>
<td>4.0e-9</td>
</tr>
<tr>
<td>1,000,000,000</td>
<td>3.9e-9</td>
</tr>
</tbody>
</table>

[End PSIJ Sensitivity] VDD1

[PSIJ Sensitivity] VCC2
<table>
<thead>
<tr>
<th>frequency(Hz)</th>
<th>sensitivity (s/V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>2.0p</td>
</tr>
<tr>
<td>10,000</td>
<td>2.0p</td>
</tr>
<tr>
<td>100,000</td>
<td>2.7n</td>
</tr>
<tr>
<td>1,000,000</td>
<td>3.0n</td>
</tr>
<tr>
<td>10,000,000</td>
<td>4.9n</td>
</tr>
<tr>
<td>100,000,000</td>
<td>4.1n</td>
</tr>
<tr>
<td>1,000,000,000</td>
<td>3.8n</td>
</tr>
</tbody>
</table>

[End PSIJ Sensitivity] VCC2

[PSIJ Sensitivity Group] DisplayPort

[Voltage List]

<table>
<thead>
<tr>
<th>V(name)</th>
<th>V(typ)</th>
<th>V(min)</th>
<th>V(max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD1</td>
<td>1.800</td>
<td>1.710</td>
<td>1.890</td>
</tr>
<tr>
<td>VCC2</td>
<td>0.600</td>
<td>0.540</td>
<td>0.660</td>
</tr>
<tr>
<td>VSS</td>
<td>0.000</td>
<td>0.000</td>
<td>0.000</td>
</tr>
</tbody>
</table>

[End Voltage List]
Quick IP Selection, based upon [PSIJ Sensitivity]

- Same IP is better:
  - from vendor2 than
  - from vendor1

- Same IP is better:
  - upon process1 than
  - upon process2

- Same IP is the best
  - from vendor2 and
  - upon process1.
Next Steps

▪ Submit IBIS BIRD to include [PSIJ Sensitivity] in IBIS.

▪ Call for EDA vendors to support [PSIJ Sensitivity] in IBIS

▪ Call for chip vendors to support [PSIJ Sensitivity] in IBIS

▪ Call for platform designers to support [PSIJ Sensitivity] in IBIS
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