

# IBIS Electrical Module Description (EMD) Overview

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# Introduction

- BIRD202.3
  - [Electrical Descriptions of Modules](#)
  - Goal was to replace the legacy Electrical Board Description (EBD)
    - Top-level model for subsystems: DIMMs, multi-chip modules, PCBs
    - Adds support for generic SPICE (IBIS-ISS) and Touchstone models
  - Approved by the IBIS Open Forum on March 12, 2021
  - Included in IBIS 7.1
    - Ratified December 10, 2021
- Minor updates in BIRD218 targeted for IBIS 7.2

# Outline

- Review IBIS EBD Modeling
- EMD Goals
- Overview
- Syntax Details
- Key Rules
- EMD Examples
- Conclusions

# Legacy EBD (Electrical Board Description)

- Allows for complex topologies with discontinuities/stubs and one-to-many pins
- Used for multi-die packages and circuit board models
- Limitations:
  - Inductance and capacitance characteristics need to be derived with respect to well defined reference plane(s)
  - No coupling between paths
    - Differential signaling not modeled properly
    - No crosstalk can be simulated
  - Assumes ideal power and ground networks
  - Only RLC parameters with no loss term or G-element
  - Insufficient connector modeling
  - Cannot model traces after Register/Databuffer on RDIMMs/LRDIMMs

# EMD Improvements

# EMD Improvement Goals

- Support:
  - Loss (frequency dependent)
  - Crosstalk
  - PDN models (many-to-many connections)
  - SPICE style nodal connections
  - S-parameters
  - Model partitioning
  - One-to-many, many-to-one, or many-to-many EMD pin to designator pin signal (I/O) connections
- Leverage existing standards:
  - **IBIS-ISS** (SPICE) models
  - **Touchstone S-parameter** models
- Integrate lower-level connections to designator components (IBIS) or nested EMD modules

# IBIS-ISS

- **IBIS-ISS: IBIS Interconnect SPICE Subcircuits**
  - Limited set of common, basic elements for passive interconnects
  - Based on Synopsys HSPICE
  - Developed and approved by the IBIS Open Forum
- **Goals:**
  - Industry standardized SPICE syntax language
  - Portable across EDA tools
  - Limited to passive interconnect circuits
  - Enable interconnect models to be defined as SPICE subcircuits
- **IBIS-ISS Specification:**
  - [https://ibis.org/ibis-iss\\_ver1.0/ibis-iss\\_ver1\\_0.pdf](https://ibis.org/ibis-iss_ver1.0/ibis-iss_ver1_0.pdf)

# IBIS-ISS Supported Features

- Supported features:
  - Basic circuit elements:
    - Resistors, Inductors, Capacitors: R, L, K, C
    - Dependent Sources: E, F, G, H (various limited functions)
    - Voltage Source: V (DC only)
    - Subcircuits: X, .subckt, .ends
  - Interconnect elements:
    - T-element (lossless T-line)
    - W-element (RLGC Model, Table Model)
    - S-element (Touchstone)
  - Basic commands:
    - .include, .param
- IBIS-ISS does **not** support:
  - Transistor models, diode models, active device models, etc.
  - SPICE engine controls/options, sweep control, measurement, printing, probing, encryption, etc.



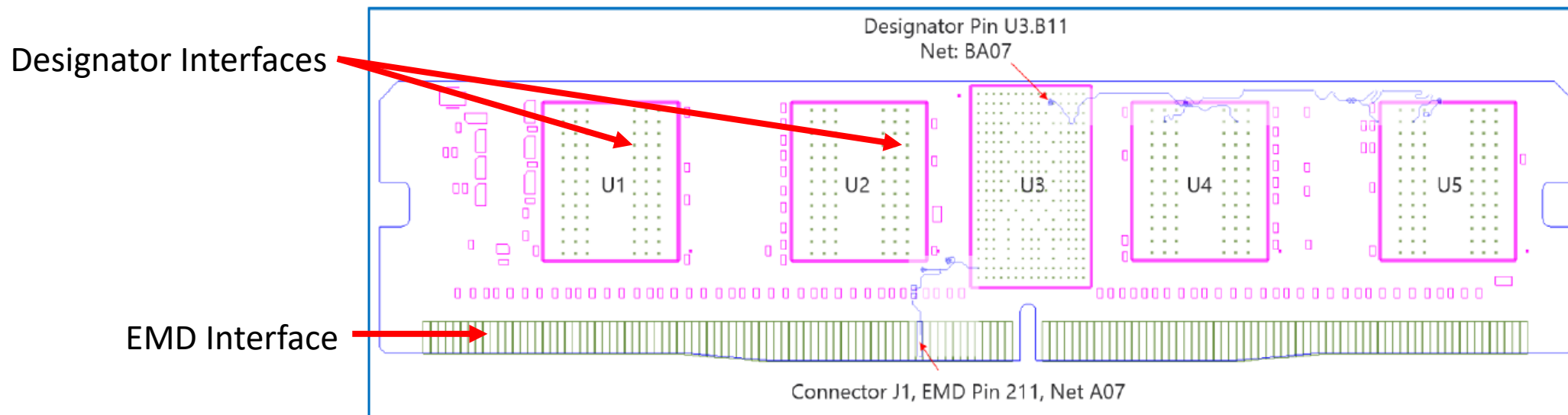
# EMD Overview and Important Concepts

# EMD Key Features

- Capability to use IBIS-ISS and Touchstone models in IBIS
  - Gives flexibility for complex, coupled, frequency dependent interconnect models
  - Enables combined I/O and PDN model connections
- An EMD model defines an electrical model of the interconnect between:
  - External pins of the module (EMD pins) and pins of designators (e.g., U1)
  - Designator pins and designator pins (e.g., post-register)
- Support for multiple methods of modeling series terminations of signals (extended nets)
- Define voltages of rails (informational for EDA tool)
- Capability for partitioned models (e.g., DQ byte lane, CA bus)
  - Aggressor\_Only (for crosstalk victim/aggressor designations)
  - EMD Groups and EMD Sets (creating model grouping and hierarchy)
- Additional bus\_label syntax to connect POWER and GND rails, allowing complex or simplified PDN modeling

# EMD Interface Details

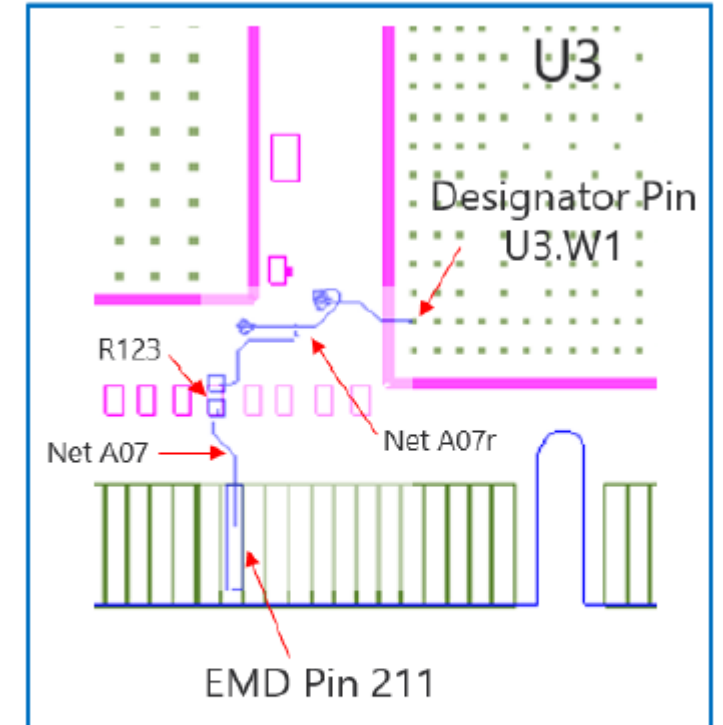
- Interface Concept
  - EMD Pin (external pin)
  - Designator Pin (at pins of designators connecting to IBIS components or another nested EMD)
- New Capability
  - Describe interconnect between designator pins



**Figure 54 – DDR4 Registered DIMM with Labeling**

# EMD Extended Nets

- Series resistors or capacitors in a net require a choice of modeling options:
  - Two nets can be combined into an “extended net”. All the pins in the two CAD nets will use the extended net name as their signal\_name in the EMD file. The resistor or capacitor would be included in the EMD Models for this extended net.
  - Create separate EMD Models for each CAD net. The series component must be assigned a designator in this case.
- Example: Net A07/A07r can be within one EMD Model or two EMD Models with designator R123



**Figure 55 – Extended Net**

# EMD Models

- [EMD Model] Keyword
  - Defines how IBIS wraps and connects the terminals of:
    - IBIS-ISS models
    - Touchstone models
  - Terminal connections defined at the **EMD Pin** or **Designator Pin** interfaces
  - Syntax distinguishes between **I/O** (signal) and **Rail** (power/ground) terminals
  - **Rail** terminal qualifiers identify the association between a terminal and a specific:
    - pin\_name
    - signal\_name
    - bus\_label
  - **I/O** terminal qualifier: pin\_name (I/O terminals always specified at Pins)
    - Terminals at the same interface or at any designator interface that have the same signal\_name are considered “connected” in the same electrical net Terminal line

# EMD Model Hierarchy: Sets and Groups

- [EMD Set] keyword
  - Wraps one or more EMD Models
  - Can be contained in a separate .ems file or in the .emd file itself
- An EMD Set contains a list of EMD Models that have a logical association such as:
  - All signals in a bus (e.g., DDR4, or PCI Express)
  - Full Power Delivery Network (PDN) structures from EMD pins to designator pins
  - Full PDN structures from EMD pins to EMD pins
  - All I/O structures between EMD pins and designator pins
  - I/O structures from designator pins to designator pins
  - Combinations of I/O and PDN structures
  - Coupled models
  - Touchstone electrical models
  - Decoupling capacitor models
  - IBIS-ISS electrical models

# EMD Model Hierarchy: Sets and Groups

- [EMD Group] keyword
  - Groups one or more EMD Sets to be used together
  - Selection mechanism
    - Only one EMD Group selected for a simulation
    - Creates the netlist of EMD Models for a simulation
- Example groupings and applications
  - **Groups** combining an EMD Set for a data bus with an EMD Set of the PDN model
  - Separate **Groups** for coupled vs. single-line models
  - **Groups** of EMD Sets with high/low impedance or fast/slow signal propagation

# Aggressor\_Only Concept

- Aggressor\_Only designates:
  - Signal should only be used as an aggressor
  - **Not** a suitable victim
  - All the crosstalk effect is **not** considered for that signal
- Multi-line EMD Models may describe only a subset of a coupled structure (e.g., a 64-line bus may be described by a four-line EMD Model). As a result, while the interconnects at the edges of the EMD Model may induce crosstalk onto other interconnects nearby, being on the edge of the EMD Model, they may not themselves experience the full crosstalk impact that the corresponding interconnect experiences in the real, full structure.
- Crosstalk simulations use coupled interconnect models consisting of nets, or extended nets that may span packages, EMDs, boards, and connectors. **If any terminal in any net or extended net in the coupled interconnect model is marked Aggressor\_Only, then the crosstalk contributions included in the simulation results reported for this net or extended net will be incomplete.**



# A\_gnd Concept

- A\_gnd = SPICE node 0 (ideal ground/simulator reference node)
- Optional Terminal\_type (to identify a terminal as a reference)
  - Connects any terminal to node 0
  - Available at any EMD Pin or Designator Pin interface
- For IBIS-ISS
  - A\_gnd may be used any number of times
  - Useful for connecting capacitor references to node 0
- For Touchstone
  - A\_gnd is permitted only once for the N+1 (reference) terminal
  - Useful for connecting S-parameter references to node 0

# Unused\_port\_termination Concept

- Unused\_port\_termination subparameter
  - Defines how to handle unused ports for Touchstone models (not IBIS-ISS)
  - Required if the EMD Model does not connect to all the Touchstone ports
  - EDA tool could do port reduction
- Setting Options:
  - Open - unconnected
  - Reference - use Touchstone per-port reference impedance
  - Resistance - specify single resistance value
- Considerations:
  - Touchstone 2.0 allows per-port reference impedance
  - [EMD Model] does not provide per-port termination values capability
  - EDA tools may allow the user to override the termination setting
  - Alternative is to wrap a Touchstone file in an IBIS-ISS subcircuit to terminate each port uniquely

# EMD Syntax Details

# EMD File Overview

- A .emd file is intended to be a stand-alone file, not referenced by or included in any .ibs, .ebd, or .pkg file.
- A .emd file is structured like a standard .ibs file.
  - It must contain the following keywords, as defined in IBIS: [IBIS Ver], [File Name], [File Rev], and [End].
  - It may also contain the following optional keywords: [Comment Char], [Date], [Source], [Notes], [Disclaimer], and [Copyright].
  - The actual module description is contained between the keywords [Begin EMD] and [End EMD]
- EMD File Keywords:
  - [Begin EMD]
  - [Manufacturer]
  - [Description]
  - [Number Of EMD Pins]
  - [EMD Pin List]
  - [End EMD Pin List]
  - [EMD Parts]
  - [End EMD Parts]
  - [EMD Designator List]
  - [End EMD Designator List]
  - [Designator Pin List]
  - [End Designator Pin List]
  - [Voltage List]
  - [End Voltage List]
  - [EMD Group]
  - [End EMD Group]
  - [End EMD]
  - EMD Sets can be in .emd file or separate .ems file
    - [EMD Set]
    - [Manufacturer]
    - [Description]
    - [EMD Model]
    - [End EMD Model]
    - [End EMD Set]

# [EMD Pin List]

- Defines external interface pins
  - For I/O Pins, only pin\_name and signal\_name are required
    - Signal\_type can be set to “NC” when there is no valid IBIS model or connection at this top-level
  - For Rail Pins, the signal\_type should be POWER or GND
    - Bus\_label can be added to further separate supply rails

```
[EMD Pin List] signal_name signal_type bus_label
| I/O Pins          (NO signal_type bus_label)
C5                DQ0
C6                DQ1
| Rail Pins
A3                VSS          GND
A4                VDD          POWER
A5                VSS          GND
B3                VDD          POWER      VDDU1
B4                VDD          POWER      VDDU2
C4                VDD          POWER
[End EMD Pin List]
```

# [EMD Designator List] and [EMD Parts]

- [EMD Parts]

- Defines EMD part names
- Maps an EMD part\_name to an IBIS component or EMD module
- EMD files can be called by another EMD (“nested” case)
- EBDs are not supported

[EMD Parts]

| part_name     | file           | Component     |
|---------------|----------------|---------------|
| DDR4_Reg_253b | register.ibs   | DDR4_Register |
| DDR4_x8_78b   | z22a.ibs       | MT40A2G8VA    |
| 510-500874    | resistors.ibs  | RES_22ohms    |
| 510-501618    | resistors.ibs  | RPACK4_33ohms |
| Stacked_die   | dram_stack.emd | EMD_name      |

[End EMD Parts]

- [EMD Designator List]

- Defines the designators on the module
- Maps an EMD designator to an EMD part name

[EMD Designator List]

|      |               |
|------|---------------|
| U3   | DDR4_Reg_253b |
| U4   | DDR4_x8_78b   |
| U5   | DDR4_x8_78b   |
| U7   | DDR4_x8_78b   |
| U8   | DDR4_x8_78b   |
| R123 | 510-500874    |
| RN13 | 510-501618    |

[End EMD Designator List]

# [Designator Pin List]

- Defines the pin names of the designator pins
  - Designator pins = internal pins to the IBIS component (or lower level EMD)
  - The syntax for the designator pin name is <designator>.<pin\_name>
- Signal\_name defines the logical connection for the path
  - Should match the datasheet name
  - The logical path can be continued for extended nets with series resistors (see examples in BIRD202.3)
- Signal\_type is required to define rails as POWER, GND, or NC
  - “NC” designation to be added by BIRD218 in IBIS 7.2. For documentation, as NC pins cannot appear in any Terminal lines of EMD Models
  - Bus\_label can be added to further separate supply rails

| [Designator Pin List] | signal_name | signal_type | bus_label |
|-----------------------|-------------|-------------|-----------|
| U3.B9                 | VDD         | POWER       | VDD1      |
| U3.B11                | BA07        |             |           |
| U3.B12                | VSS         | GND         |           |
| U3.V3                 | VDD         | POWER       | VDD1      |
| U3.W1                 | A07r        |             |           |
| U3.W3                 | VSS         | GND         |           |
| U4.K9                 | VSS         | GND         |           |
| U4.M8                 | BA07        |             |           |
| U4.N9                 | VDD         | POWER       | VDD1      |
| U5.K9                 | VSS         | GND         |           |
| U5.M8                 | BA07        |             |           |
| U5.N9                 | VDD         | POWER       | VDD1      |
| U7.K9                 | VSS         | GND         |           |
| U7.M8                 | BA07        |             |           |
| U7.N9                 | VDD         | POWER       | VDD1      |
| U8.K9                 | VSS         | GND         |           |
| U8.M8                 | BA07        |             |           |
| U8.N9                 | VDD         | POWER       | VDD1      |
| R123.1                | A07         |             |           |
| R123.2                | A07r        |             |           |
| RN13.2                | VTT         | POWER       |           |
| RN13.7                | BA07        |             |           |

[End Designator Pin List]

# [EMD Group] and [EMD Set]

- [EMD Set] Keyword
  - Wraps one or more EMD Models
  - Can be contained in a separate .ems file or in the .emd file itself
- [EMD Group] Keyword
  - Groups one or more EMD Sets to be used together
  - Selection mechanism
    - Only one EMD Group selected for a simulation
    - Creates the netlist of EMD Models for a simulation
- Example groupings and applications
  - Different **Sets** based on model extraction techniques
  - **Groups** for each bus (DQ, Address/Command, etc.)
  - Separate **Groups** for coupled vs. single-line models

```
[EMD Group]      Addr_07_Group_1
Addr_07_1  NA
[End EMD Group]
[End EMD]
```

```
[EMD Set]        Addr_07_1
[EMD Model]      A07_1
File_IBIS-ISS    A07.iss          A07_1
Number_of_terminals = 6
...
[End EMD Model]
```

```
[EMD Model]      BA07_1
File_IBIS-ISS    A07.iss          BA07_1
Number_of_terminals = 19
...
[End EMD Model]
```

```
[END EMD Set]
```



# [EMD Model]

- Defines connections to the electrical model of the interconnect between EMD pins and designator pins
  - Calls the SPICE file or Touchstone file
  - Defines the terminal lines
- Syntax:
  - Param (optional)
  - File\_IBIS-ISS or File\_TS
  - Unused\_port\_termination (only for Touchstone files)
  - Number\_of\_terminals
  - <Terminal lines>

```
[EMD Model]      BA07_2
File_IBIS-ISS    A07.iss      BA07_2
Number_of_terminals = 19
1 Pin_I/O        pin_name      U3.B11
2 Pin_Rail       bus_label     U3.VDD1
3 Pin_Rail       signal_name   U3.VSS
4 Pin_I/O        pin_name      U4.M8
5 Pin_Rail       bus_label     U4.VDD1
6 Pin_Rail       signal_name   U4.VSS
7 Pin_I/O        pin_name      U5.M8
8 Pin_Rail       bus_label     U5.VDD1
9 Pin_Rail       signal_name   U5.VSS
10 Pin_I/O       pin_name      U7.M8
11 Pin_Rail      bus_label     U7.VDD1
12 Pin_Rail      signal_name   U7.VSS
13 Pin_I/O       pin_name      U8.M8
14 Pin_Rail      bus_label     U8.VDD1
15 Pin_Rail      signal_name   U8.VSS
16 Pin_I/O       pin_name      RN13.7
17 Pin_Rail      bus_label     VDD1
18 Pin_Rail      signal_name   RN13.VTT
19 Pin_Rail      signal_name   VSS
[End EMD Model]
```

# Terminal lines

- Defines the pin connections to the [EMD Model] terminals
- Syntax:
  - `<Terminal_number> <Terminal_type>`  
`<Terminal_type_qualifier> <Qualifier_entry>`  
`[Aggressor_Only]`
    - Terminal\_number: File\_IBIS-ISS .subckt node position or File\_TS Touchstone port number
    - Terminal\_type: Identifies the terminal
      - A\_gnd = reference
      - Pin\_Rail = supply
      - Pin\_I/O = I/O signal
    - Terminal\_type\_qualifier: Association type for the terminal to a pin\_name, signal\_name, or bus\_label
    - Qualifier\_entry: Entry of the pin\_name, signal\_name, or bus\_label connecting to the terminal
    - Aggressor\_Only: Optional flag declaring that the terminal is not a suitable victim for crosstalk simulations

| Terminal_number | Terminal_type | Terminal_type_qualifier | Qualifier_entry |
|-----------------|---------------|-------------------------|-----------------|
| 1               | Pin_I/O       | pin_name                | U3.B11          |
| 2               | Pin_Rail      | bus_label               | U3.VDD1         |
| 3               | Pin_Rail      | signal_name             | U3.VSS          |
| 4               | Pin_I/O       | pin_name                | U4.M8           |
| 5               | Pin_Rail      | bus_label               | U4.VDD1         |
| 6               | Pin_Rail      | signal_name             | U4.VSS          |
| 7               | Pin_I/O       | pin_name                | U5.M8           |
| 8               | Pin_Rail      | bus_label               | U5.VDD1         |
| 9               | Pin_Rail      | signal_name             | U5.VSS          |
| 10              | Pin_I/O       | pin_name                | U7.M8           |
| 11              | Pin_Rail      | bus_label               | U7.VDD1         |
| 12              | Pin_Rail      | signal_name             | U7.VSS          |
| 13              | Pin_I/O       | pin_name                | U8.M8           |
| 14              | Pin_Rail      | bus_label               | U8.VDD1         |
| 15              | Pin_Rail      | signal_name             | U8.VSS          |
| 16              | Pin_I/O       | pin_name                | RN13.7          |
| 17              | Pin_Rail      | bus_label               | VDD1            |
| 18              | Pin_Rail      | signal_name             | RN13.VTT        |
| 19              | Pin_Rail      | signal_name             | VSS             |

# Terminal\_type\_qualifier Options

| Terminal_type | Terminal_type_qualifier |             |           | Aggressor_Only |
|---------------|-------------------------|-------------|-----------|----------------|
|               | pin_name                | signal_name | bus_label |                |
| Pin_I/O       | X                       |             |           | A              |
| Pin_Rail      | Y                       | Y           | Y         |                |
| Pin_Rail      |                         | *.Y         | *.Y       |                |
| A_gnd         |                         |             |           |                |

“X” = I/O pin\_names; “Y” = POWER and GND names; “A” = Aggressor\_Only

- Applies to both [EMD Pin List] and [Designator Pin List]
- The format for designator terminals is:
  - <Terminal\_number> <Terminal\_type> <Terminal\_type\_qualifier> <designator>.<Qualifier\_entry>
  - “\*.Y” indicates that all of the “Y” named POWER and GND terminals on each of the [Designator Pin List] interfaces are shorted together

## [Voltage List]

- Defines the signal\_names or bus\_labels that are rail signals, as well as their voltage values.
- Provides information about expected voltage source values at EMD Pin List and Designator Pin List interfaces for any or all the rail signals. The EDA tool can override these values.
- Optional keyword

```
[Voltage List]
| V(name) V(typ) V(min) V(max)
VSS      0.0    0.0    0.0
VDD      1.2    1.1    1.3
[End Voltage List]
```

What's Next?

# What's Next for EMD?

- BIRD218: [Designator Pin List Relaxation](#)
  - To be included in IBIS 7.2
  - Removes the requirement of having to list “all pin\_name pins for each designator” in the [Designator Pin List] keyword. Reduces the need to include NC pins and unused designator pins.
  - Adds “NC” signal\_type for Designator Pin List to allow documentation of NC pins
- EMD currently supported in multiple EDA tools
- Several EMD models for multi-die memory packages available for EDA tool testing and model development
  - Contact me for support ([rrwolff@micron.com](mailto:rrwolff@micron.com))

