Challenges and Solutions in Supporting USB4 Interface

Asian IBIS Summit, Shanghai PRC

Jianping Kong

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cadence®

Agenda

- USB4 Challenges
- Compliance Kit setup
- AMI Model parameters
- Requirements to pass USB4 Gen 4 Compliance
- USB4 Spec
  - This presentation refers to tables and sections defined in the USB4 Specification V2.0
  - https://www.usb.org/document-library/usb4r-specification-v20

USB4 Gen 4 Compliance Challenges

- Equalization
  - Tx AMI Model
    - 42 presets
    - 2 precursor taps
    - 1 postcursor tap
  - Rx AMI Model
    - 2 stage CTLE
    - 12 tap DFE
- SNDR (Signal to Noise Distortion Ratio)
  - Not a standard serial link measurement

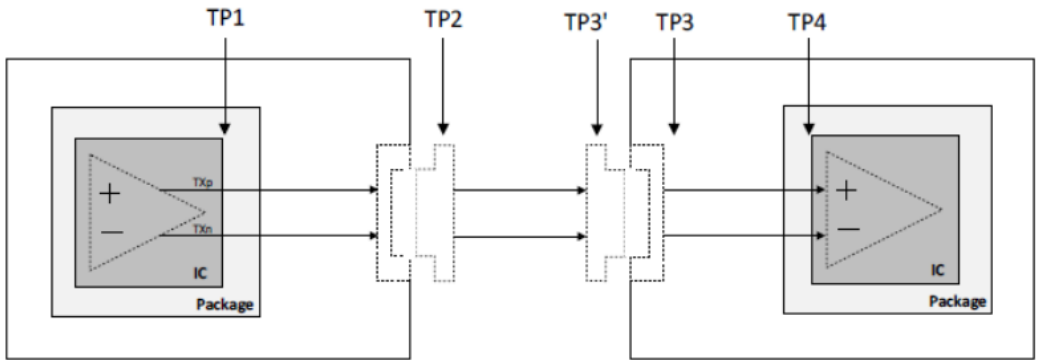
Compliance Tests

USB 4 - Gen 4 Compliance Kit

Choose Compliance Items

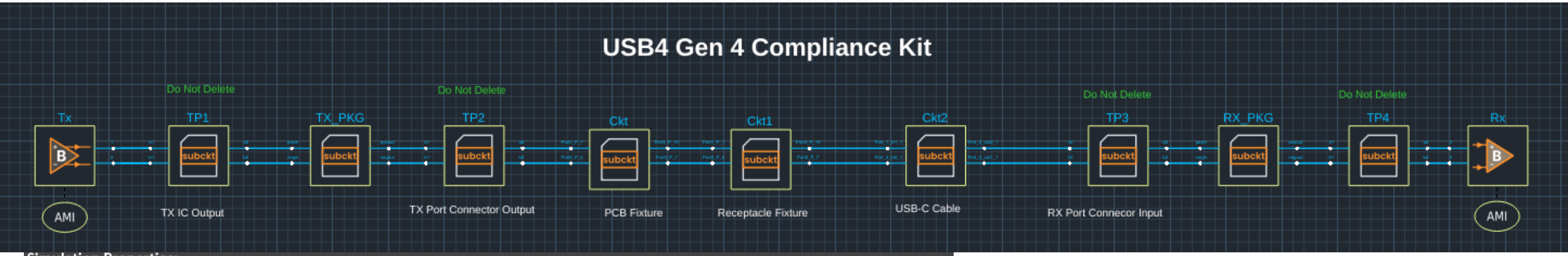
No.	Parameter	Values	☐
Transmitter Tests (Table 3-22)			
1	Tx Level		☐
2	Tx Differential Return Loss		☐
3	Tx Signal to Noise Distortion Ratio (SNDR) (Section 3.2.3.4)	32.5 dB	☐
Receiver Tests			
4	End to End Channel Differential Insertion Loss @ 12.8 GHz	28.5 dB	☐
5	Rx Differential Return Loss		☐
6	Receiver Tolerance Test (Section 3.2.4.2)		☐

Figure 3-27. Gen 4 Compliance Test Point Definitions



- Tx Tests
  - Tx Level
  - Tx Differential Return Loss (Figure 3-31)
  - Tx Signal to Noise Distortion Ration (SNDR) (Section 3.2.3.4)
- Rx Tests
  - End to End Channel Differential Insertion Loss @12.8 GHz
  - Differential Return Loss Mask (Figure 3-35)
  - Receiver Tolerance Test (Section 3.2.4.2)

Compliance Kit Setup



Simulation Properties:

Data Rate (Gbps)	Log BER	Ignore Time (ns)	Minimum # of Bits	Bit Sampling Rate	BER Floor
38.4	-8	200	100000	32	1e-8

- 25.6GBaud/S PAM3 Signaling (40 GBPs)
- 42 Preset TX AMI Model
- Dual Stage CTLE with 12 Tap DFE RX AMI Model
- Users can replace all Rx, Tx, PKG, and interconnect models with their own

Figure 3-27. Gen 4 Compliance Test Point Definitions

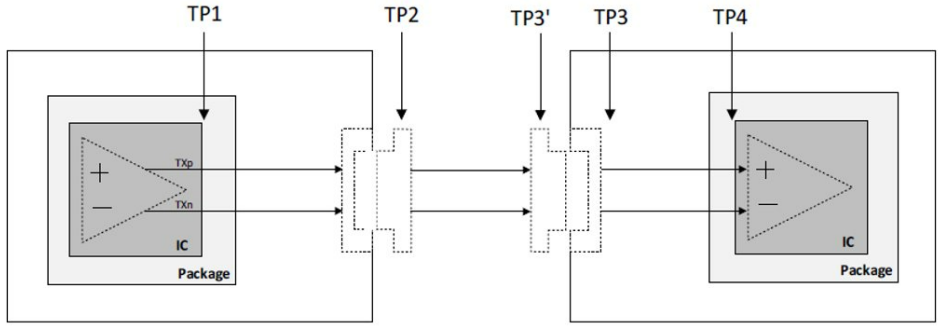


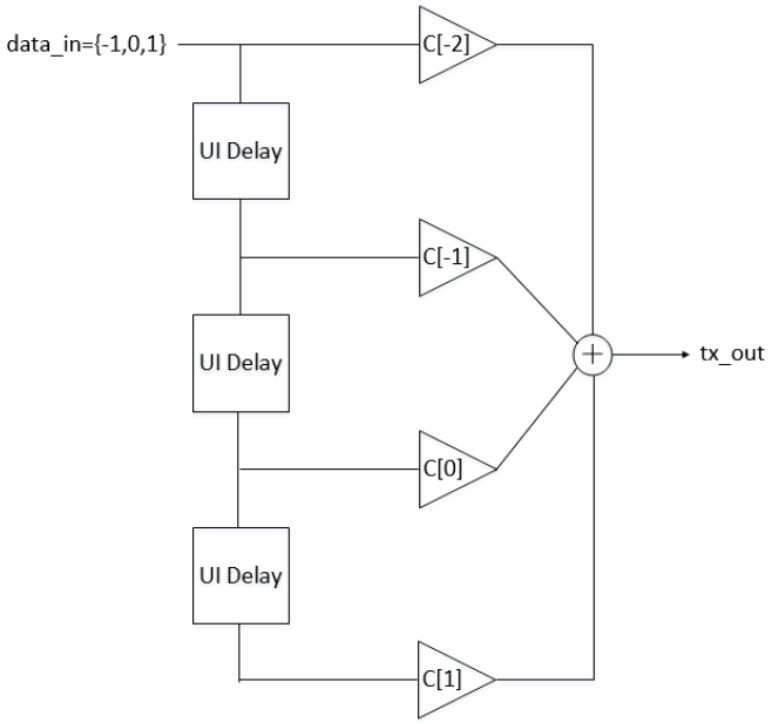
Table 3-21. Electrical Compliance Test Points

Test Point	Description	Comments
TP1	Transmitter IC output	Not used for Gen 4 electrical testing.
TP2	Transmitter port connector output	Defined at the output of a compliance plug fixture.
TP3	Receiver port connector output	Defined at the receptacle side of the connector. All measurements at this point shall be done while applying the reference equalization function.
TP3'	Receiver port connector input	Defined at the output of a compliance plug fixture.
TP4	Receiver IC input	Not used for Gen 4 electrical testing.

Tx AMI

- Tx Equalization
  - 42 presets defined in USB4 Spec
  - Default preset of Tx shall be configured to setting that obtains lowest data dependent jitter

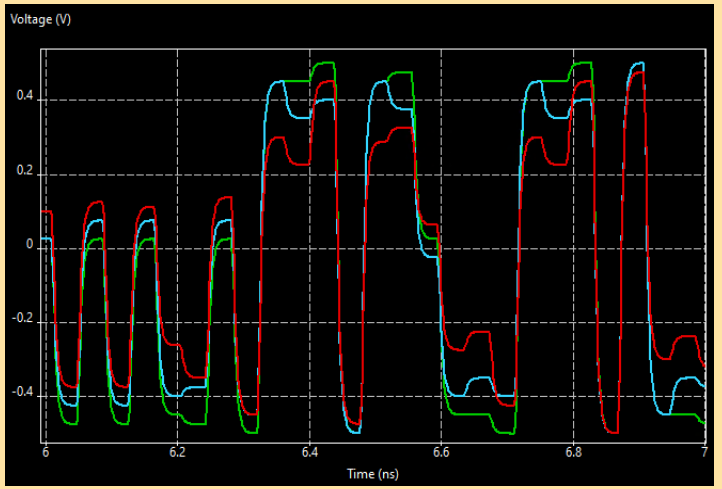
Figure 3-32. Transmitter Equalizer Structure



USB4 Gen4 TXAMI Model

Table 3-24. Transmitter Equalization Presets

Preset Number	C[-2]	C[-1]	C[0]	C[1]
0	0	0	1	0
1	0	0	0.95	-0.05
2	0	0	0.9	-0.1
3	0	0	0.85	-0.15
37	0.05	-0.25	0.65	-0.05
38	0.075	-0.25	0.675	0
39	0.075	-0.25	0.625	-0.05
40	0	-0.10	0.40	0
41	0	0	0.50	0



Rx AMI

- Rx Equalization
- Dual stage CTLE with 12 tap DFE
  - All measurements at TP3 shall be taken while applying the reference equalization function

CTLE:

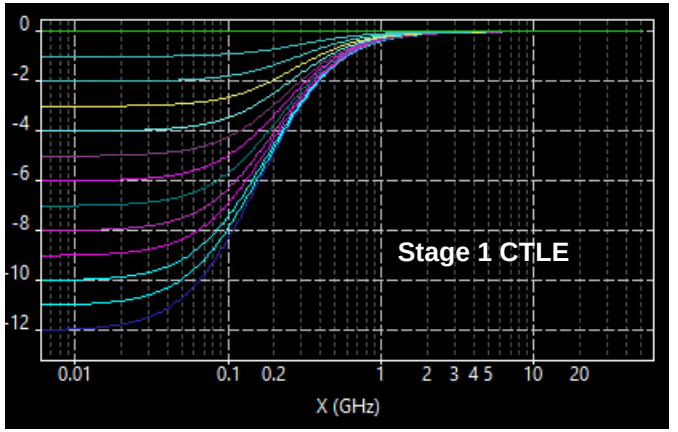
$$H(s) = \frac{(s + 2\pi f_{LP} \cdot A_{DC\_LP})}{(s + 2\pi f_{LP})} \cdot \frac{f_{p1} \cdot (s + 2\pi f_{z1} \cdot A_{DC\_1})}{f_{z1} \cdot (s + 2\pi f_{p1})} \cdot \frac{2\pi f_{p2}}{(s + 2\pi f_{p2})}$$

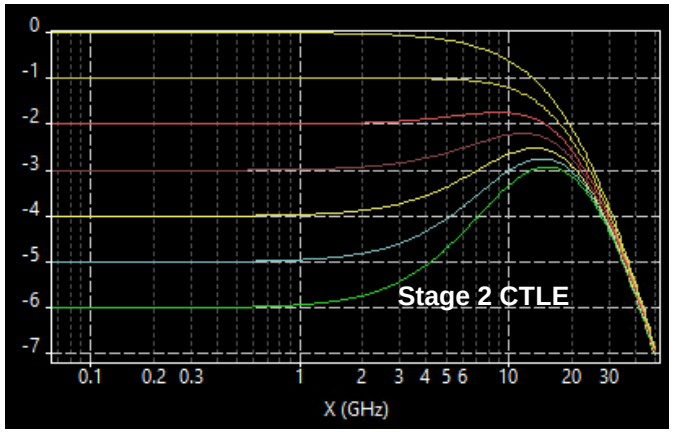
Nominal setting: $f_{LP}=F_{baud}/80$

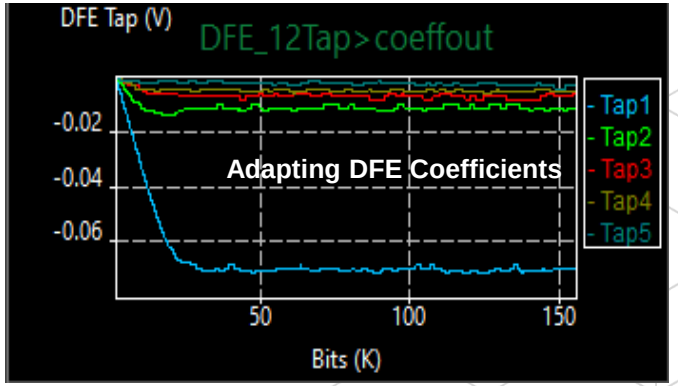
Nominal setting: $f_{p1}=f_{z1}=F_{baud}/2.5$

Nominal setting: $f_{p2}=F_{baud}$

RX EQ Settings			
g_DC	[-12:1:0]	dB	CTLE stage1 (high pole) DC attenuation
g_DC_HP	[-6:1:0]		CTLE stage2 (low pole) DC attenuation
f_HP_PZ	0.32	GHz	CTLE stage2 pole location
f_z	10.24	GHz	CTLE stage1 zero location
f_p1	10.24	GHz	CTLE stage1 first pole location
f_p2	25.6	GHz	CTLE stage1 second pole location
N_b	12	UI	Number of DFE taps
b_max(1)	0.75		Dynamic range limitation for the DFE first tap (referenc
b_max(2..N_b)	0.2		Dynamic range limitation for the DFE taps 2 and above



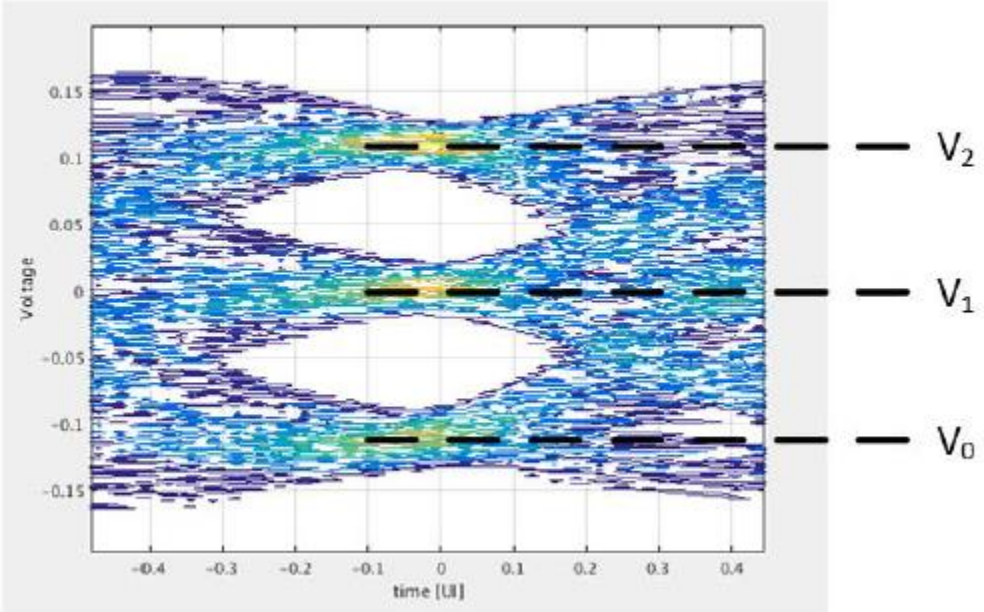




Tx Level

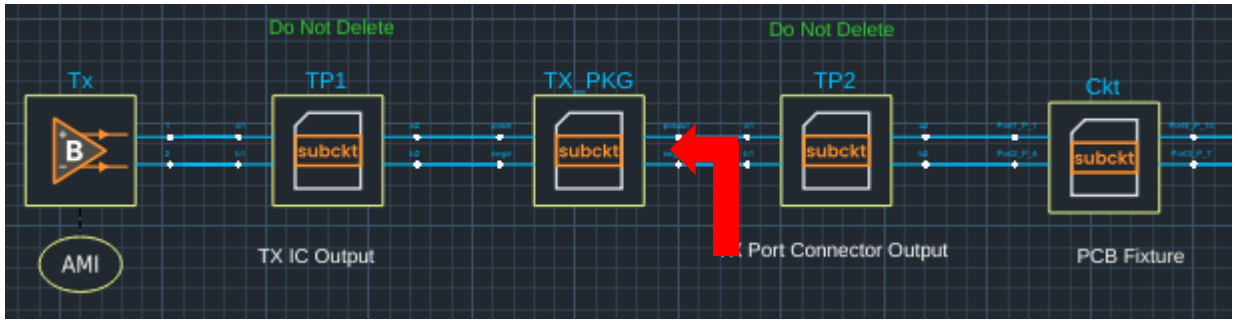
- Tx levels mismatch ratio is calculated as a function of the mean PAM3 constellation levels
- TX_LEVELS_MISMATCH = min{(V2-V1)/Δ, (V1-V0)/Δ}
- TX_LEVELS_MISMATCH >= 0.975

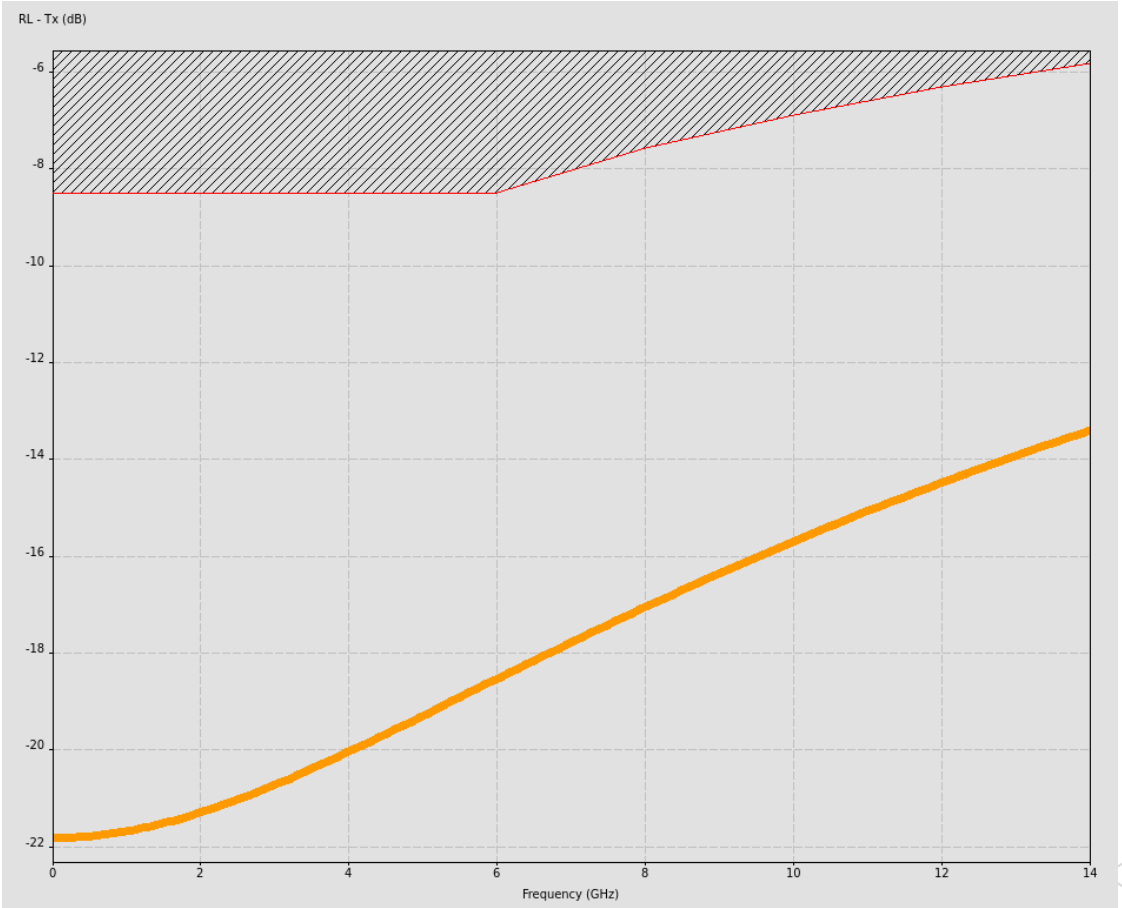
Figure 3-29. PAM3 Constellation Levels



Tx Differential Return Loss – 3.2.3.7

- Tx Return Loss should only include Tx and PKG
- IBIS File usage
  - Calculate output impedance and use C_Comp
  - Will use external model if pointed to in IBIS





$$\mathrm{SDD22(f)} = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 6 \\ -5.84 + 7.2 \cdot \log 10\left(\frac{f_{GHz}}{14}\right) & 6 < f_{GHz} \leq 14 \end{cases}$$

Tx Signal to Noise and Distortion (SNDR) – 3.2.3.4

- Ratio between linear fit pulse peak and the root square sum of linear fit error and additive noise
  - SNDR is the variation between the ideal signal and the measured signal
  - Same as IEEE Ethernet standards
- TX_SNDR >= 32.5dB

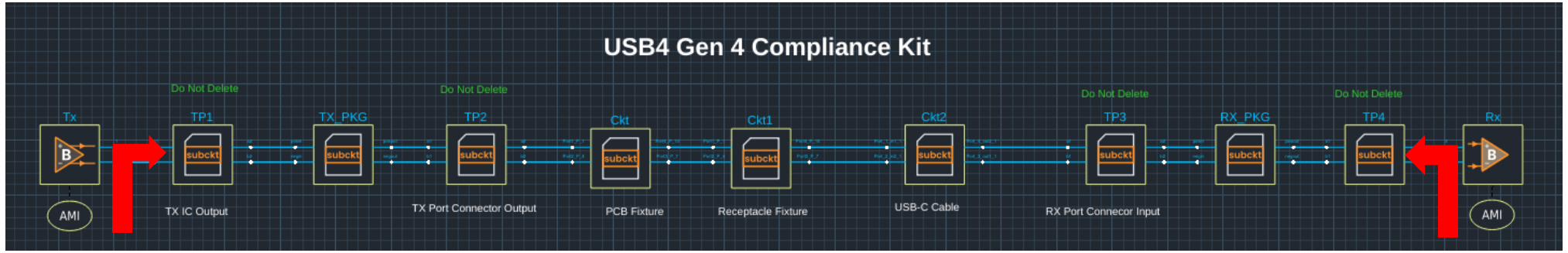
The TX_SNDR is defined as follows:

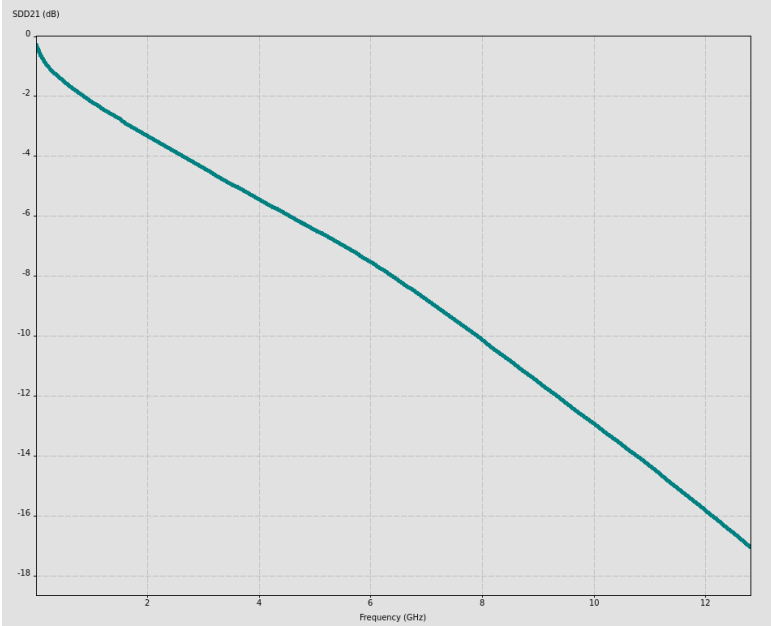
$$TX\_SNDR = 20 \cdot log_{10}\left(\frac{P_{max}}{\sqrt{\sigma_e^2 + \sigma_n^2}}\right)$$

where, P_{max} is the maximum value of the linear fit pulse response p(k).

End to End Channel Differential Insertion Loss – 3.2.4.2

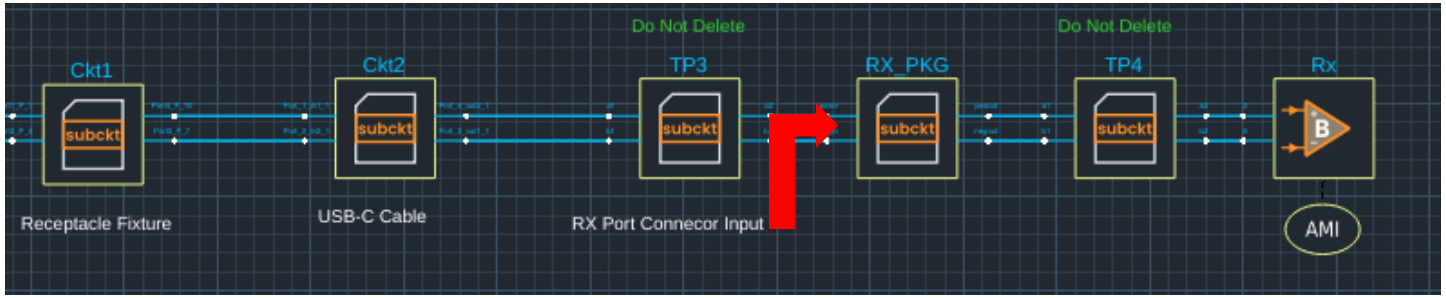
- Single point test at 12.8GHz
  - IL < -28.5 dB @ 12.8GHz
  - Package to package

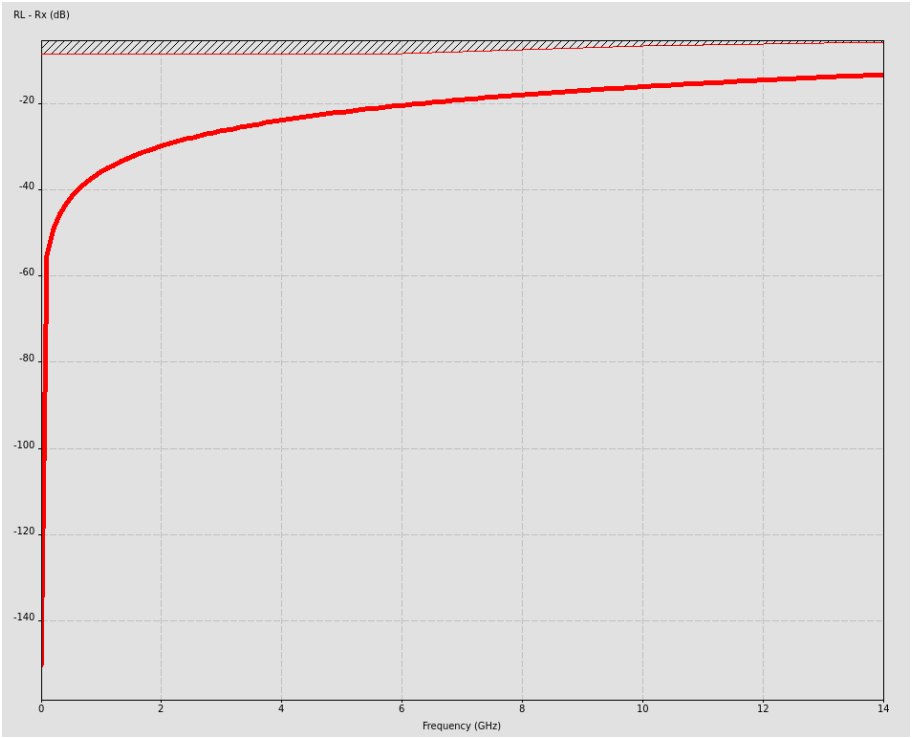




Rx Differential Return Loss – 3.2.4.1.2

- Rx Return Loss should only include Rx and PKG
- IBIS File usage
  - Calculate input impedance and use C_Comp
  - Will use external model if pointed to in IBIS





Receiver Tolerance Testing – 3.2.4.2

- Receiver tested by injecting different sinusoidal jitter (SJ) one at a time.
  - Jitter frequencies 1 MHz, 2 MHz, 10 MHz, 50 MHz, and 100 MHz
- Tx parameters configured to Table 3-27
- Operate at BER of 1E-8 or lower

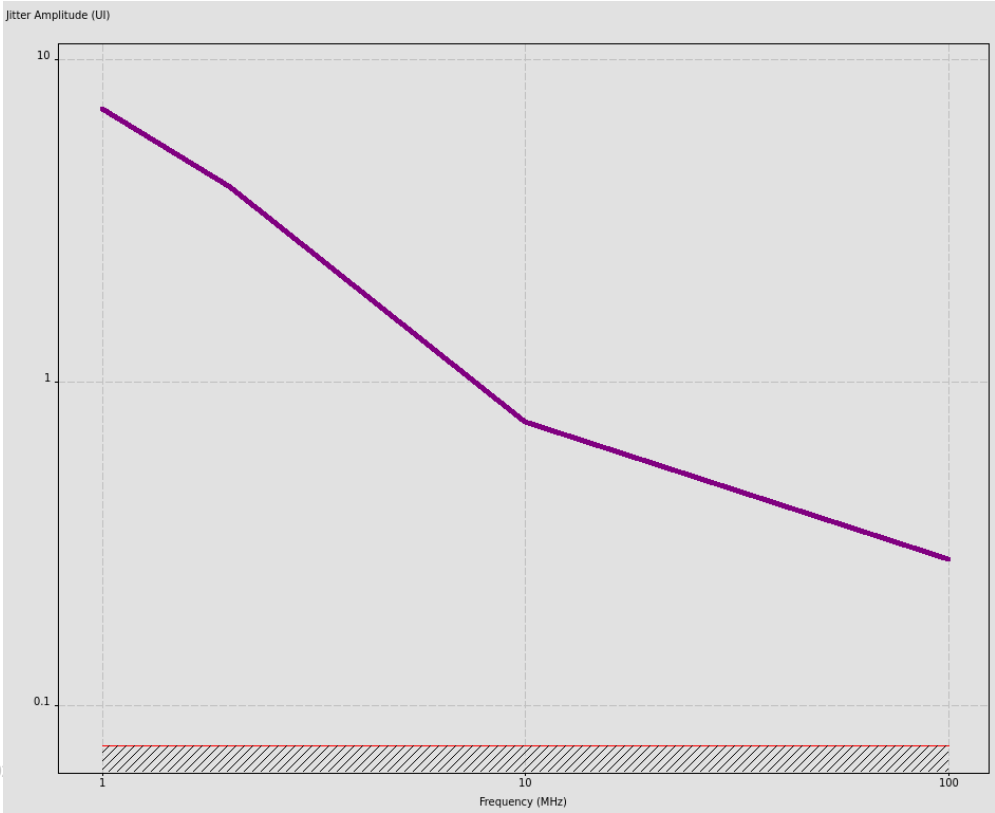


Table 3-27. Stressed Signal for Gen 4 Receiver Compliance Testing

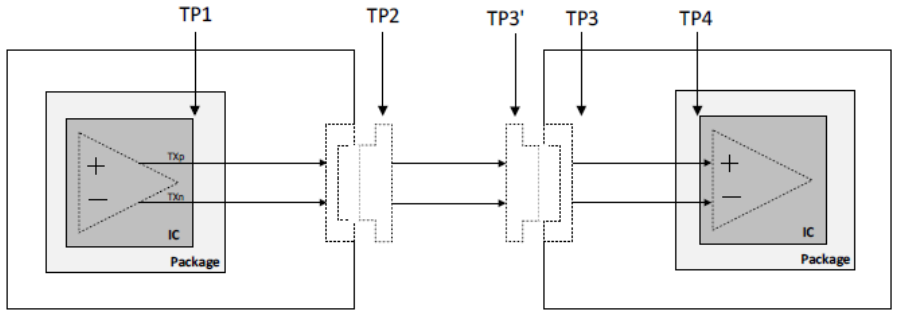
Test Case	Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
1	1000	32.5	0.975	100	0.085	0.0085
2a+2b	800	32.5	0.975	100	0.075	0.0085

USB4 Compliance Report

USB 4 - Gen 4 Compliance Report

Sep 14, 2023

Figure 3-27. Gen 4 Compliance Test Point Definitions



General Information

- **Project File:** usb4_compliance.topx
- **Circuit Simulator:** SPDSIM

Summary of Results

Transmitter Tests (Table 3-22)

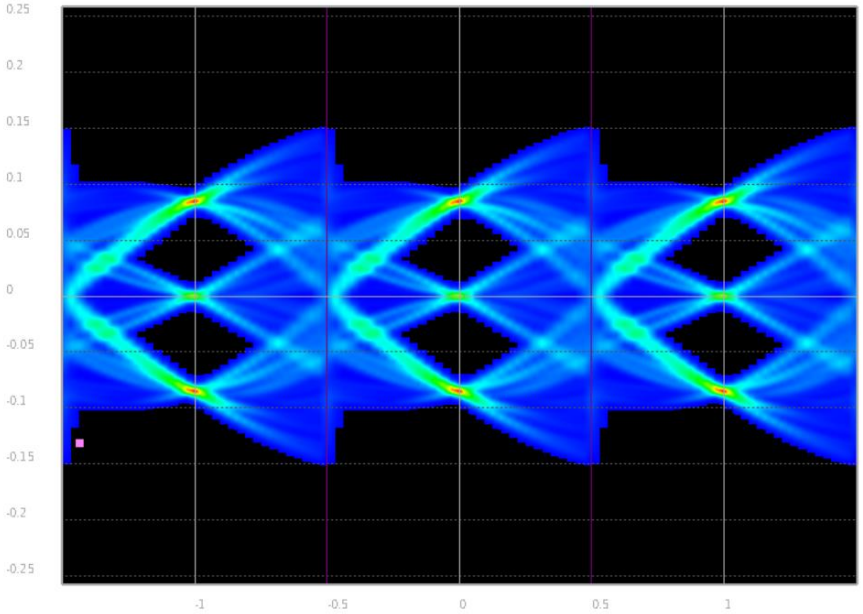
Item	Value	Simulation Results	Pass/Fail
Tx Level	800 mV	800.009	Pass
Tx Differential Return Loss		RL - Tx	Pass
Tx Signal to Noise Distortion Ratio (SNDR) (Section 3.2.3.4)	32.5 dB	83.692	Pass

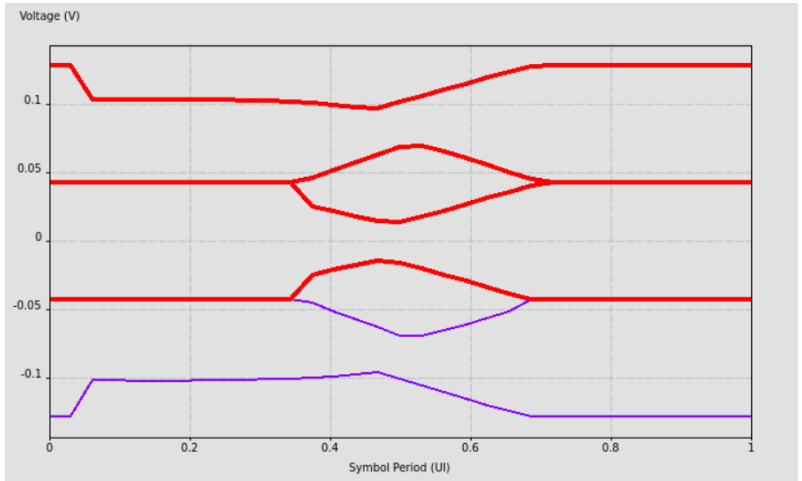
Receiver Tests

Item	Value	Simulation Results	Pass/Fail
End to End Channel Differential Insertion Loss @ 12.8 GHz		SDD21	Pass
Rx Differential Return Loss		RL - Rx	Pass
Receiver Tolerance Test (Section 3.2.4.2)		Jitter	Pass

USB4 Simulation Results

Eye Density





Eye Contours

******* pam0 *******

Eye Contour Measurements:

Eye Height = 53 mV
Eye Height Measured at = 0.5 UI
Eye Jitter = 0.65 UI
Eye Jitter Measured at = -42 mV
Eye Norm Jitter and Noise (NJN) = 0.92
Channel Operating Margin (COM) = 8.70 dB

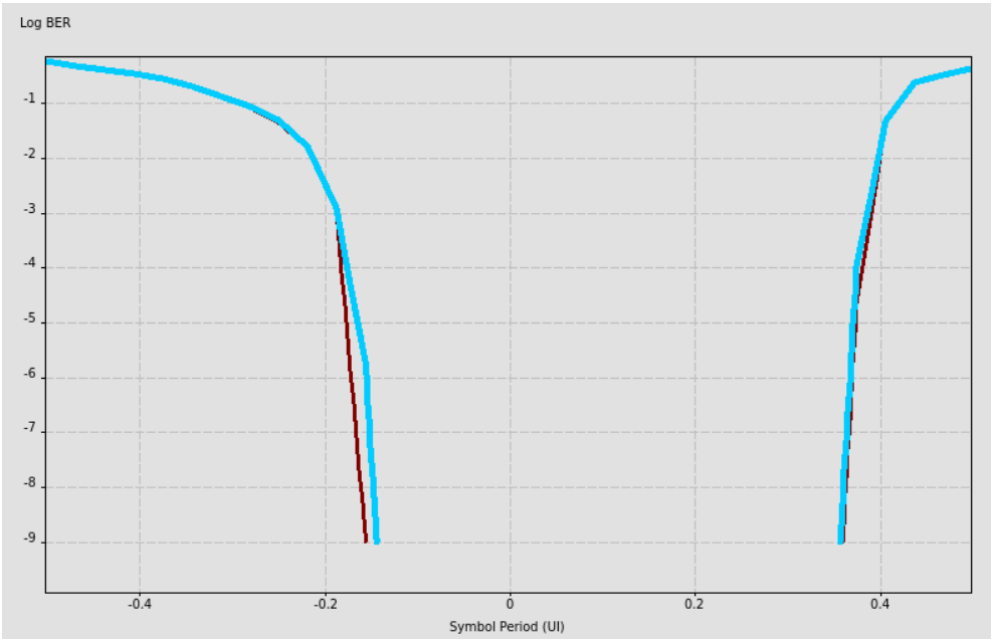
Eye Density Signal to Noise Ratio (SNR) = 152.12

BER Measurements:

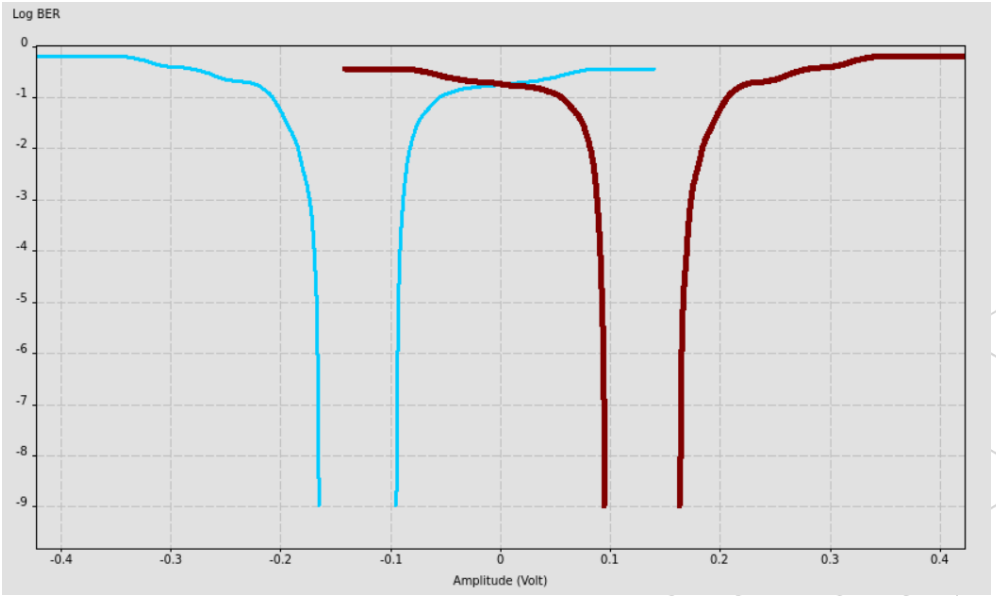
LBER(log BER)	Eye Width(UI)
-9	0.24
-8	0.26
-7	0.27
-6	0.30
-5	0.33
-4	0.37
-3	0.41

mV BER Measurements:

LBER(log BER)	Eye Height(mV)
-9	38
-8	41
-7	45
-6	50
-5	54
-4	60
-3	65



Bathtub Curve



Noise Bathtub

Conclusion

- Challenges simulating next-gen interfaces
  - Unique measurements
  - Higher speeds and encoding
- USB4 Compliance Kit
  - Tx & Rx Checks
  - Interconnect, Channels Checks
  - IBIS, AMI Models

Possible Questions

- PAM3 Encoding
  - Each symbol encodes 1.57 bits obtained through 11-bits to 7-trits mapping. USB4 Gen 4 operate with Trit Error Ratio (TER) of 1E-8. How does this compliance kit handle this bit-to-trit mapping?
    - We are currently developing user controlled bit-to-trit mapping. Through testing BER of 1E-8 and TER of 1E-8 at this level of mapping has shown negligible difference.