KEYSIGHT

Advanced SerDes & DDR AMI Modeling and Simulation

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Keysight Technologies

Asian IBIS Summit (Shanghai)
November 10, 2023

Agenda

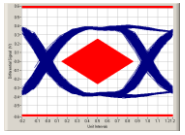
- **Development Trends & Challenges in High-Speed Digital Design**
- Modeling and Simulation Challenges
- AMI Modeling and Simulation Solutions
- Summary

Development Trends & Challenges in High-Speed Digital Design

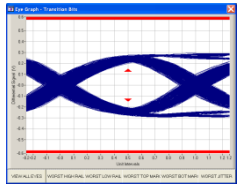
Acceleration of Innovation

- Increased speed means Increased complexity
- New design and measurement challenges are here
- No sign of slowing…

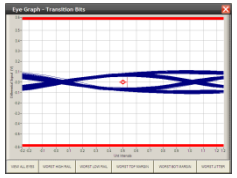
2003
PCIe 1.0 (2.5 GT/s)



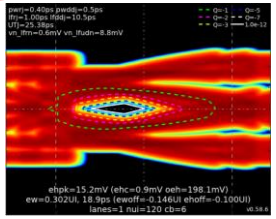
2006
PCIe 2.0 (5 GT/s)



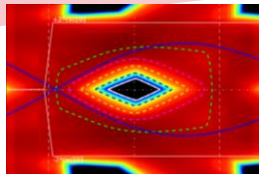
2010
PCIe 3.0 (8 GT/s)



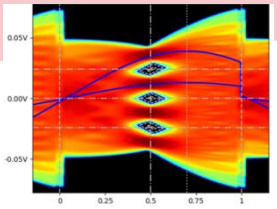
2017
PCIe 4.0 (16 GT/s)



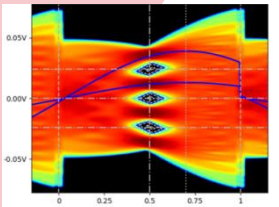
2019
PCIe 5.0 (32 GT/s)



2022
PCIe 6.0 (64 GT/s)



2024-2025
PCIe 7.0 (128 GT/s)

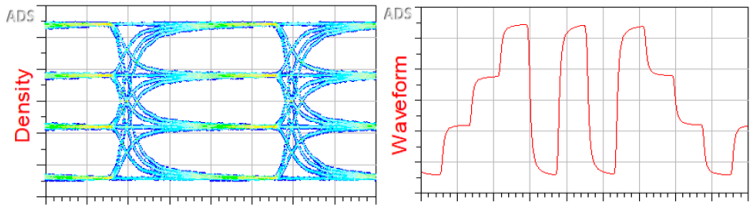


Development Trends & Challenges in High-Speed Digital Design

PAM-n modulation

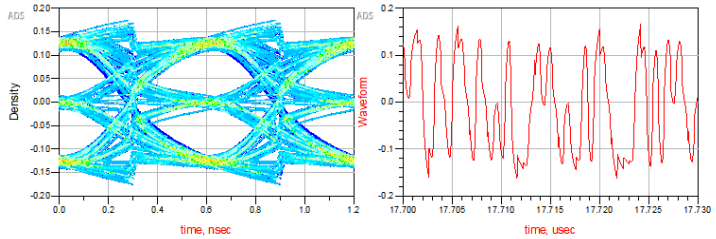
Multi-Level Signaling Methodologies:PAM-2(NRZ), PAM-3, PAM-4, PAM-8, PAM16

PAM4 modulation



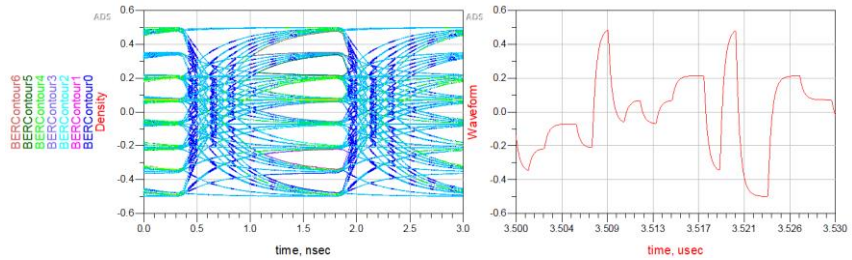
- PCIe6/PCIe7
- Ethernet
- GDDR6X

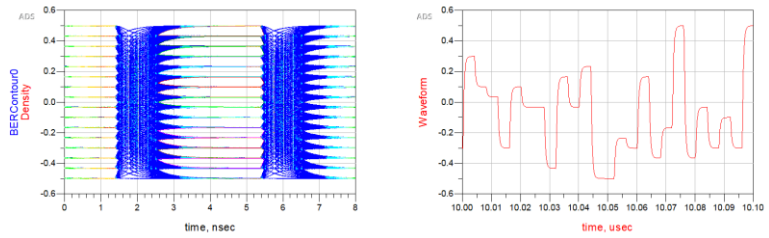
PAM3 modulation



- USB4 V2
- GDDR7

PAM8/16 modulation





- MIPI A-PHY

Development Trends & Challenges in High-Speed Digital Design

PAM-n Signaling Benefits and Challenges

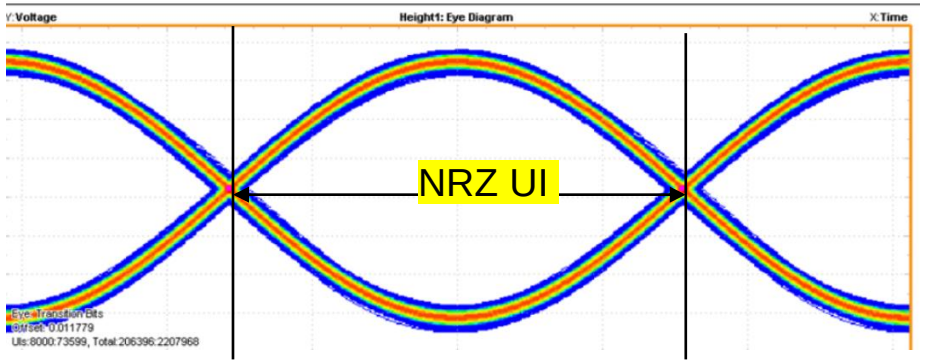
Benefits

- PAM-n improves transmission efficiency
- PAM-n could reduce bandwidth limitation

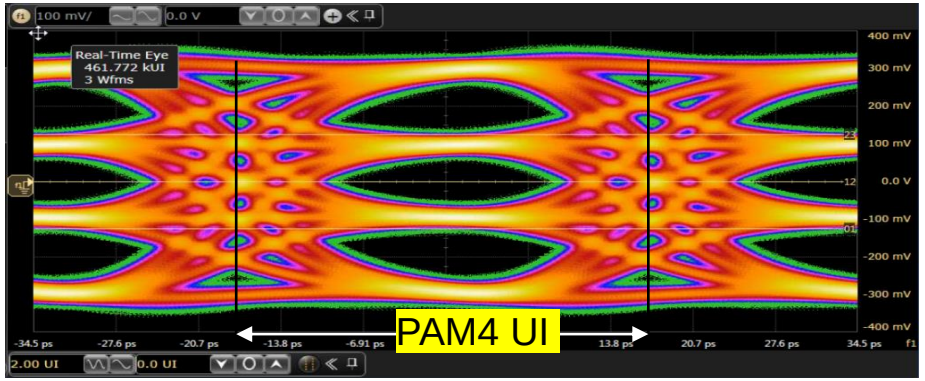
	Nyquist Frequency	Insertion Loss	Signal Mapping	Baud Rate	Bit Rate
NRZ (PAM-2)	10 GHz	22.5 dB	1 bit to 1 symbol	20 Gbaud/s	20 Gbps
PAM-3	10 GHz	22.5 dB	3 bits to 2 symbols	20 Gbaud/s	30 Gbps
PAM-4	10 GHz	22.5 dB	2 bits per symbol	20 Gbaud/s	40 Gbps
PAM-8	10 GHz	22.5 dB	4 bits per symbol	20 Gbaud/s	80 Gbps

Challenges

- 1/3 reduction in amplitude (9 dB SNR degradation)
- ~ 33% UI timing loss due to level transitions



Sensitivity to noise (xtalk, reflection, and other noise sources) is a key challenge.



Agenda

- Development Trends & Challenges in High-Speed Digital Design
- **Modeling and Simulation Challenges**
- Modeling and Simulation Insights
- Summary

PAM-N Modeling Challenges

Transmitter Linearity, Noise and Distortions

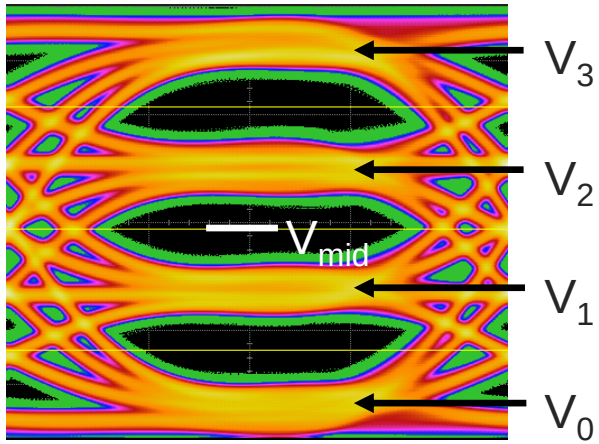
- **RLM (Level Separation Mismatch Ratio)** R_{LM}
  - Identify **transmitter nonlinearity**.
  - Verify linear spacing of the PAM-N levels
  - Ideal PAM4: {-0.5, -1/6, 1/6, 0.5}
  - Assuming non-ideal mapping table is {V_0 ,V_1 , V_2, V_3}

$V_{mid} = (V_0 + V_3) / 2$

$ES_1 = (V_1 - V_{mid}) / (V_0 - V_{mid})$

$ES_2 = (V_2 - V_{mid}) / (V_3 - V_{mid})$

$R_{LM} = \min((3*ES_1), (3*ES_2), (2 – 3*ES_1), (2 – 3*ES_2))$



- **SNDR (Signal to Noise and Distortion Ratio)**
  - Distortion: Introduced by level mismatch.
  - Noise: Uncorrelated RMS amplitude noise of each symbol level

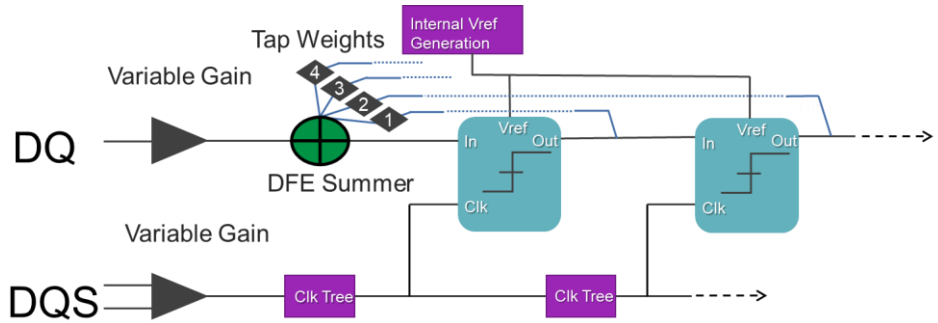
$$SNDR = 10\log_{10}\left(\frac{p_{\max}^2}{\sigma_e^2 + \sigma_n^2}\right)$$

PAM-N Modeling Challenges

Receiver Non-linearity

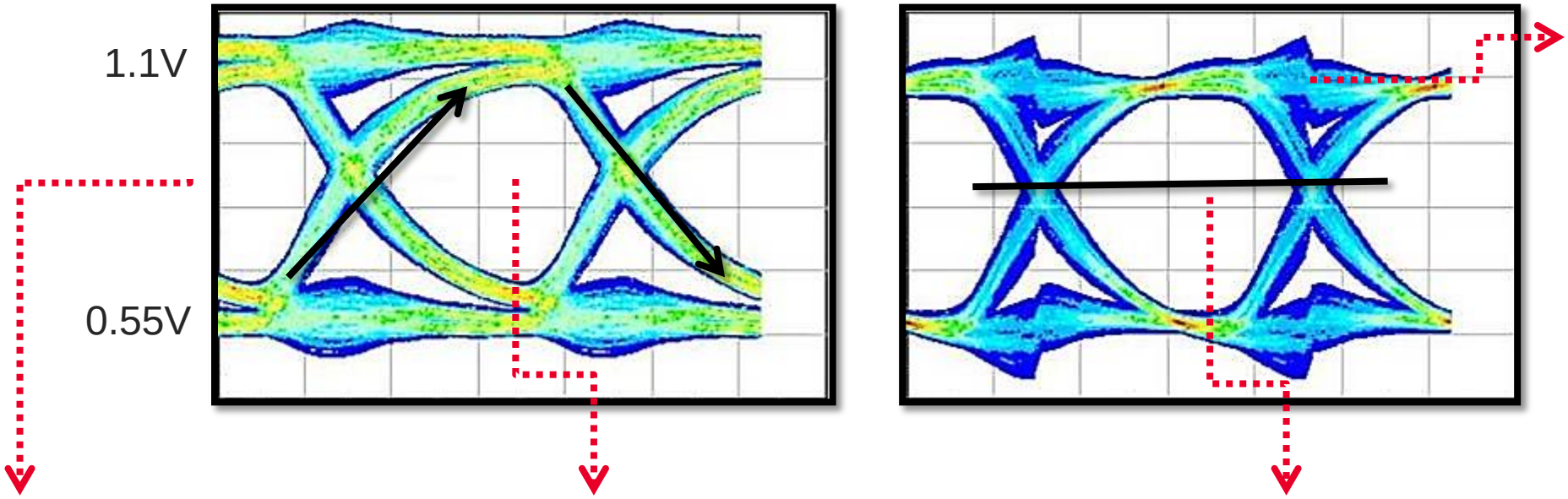
- **Gain Compression**
  - Output/input relationship
  - Causes reduction of gain
  - Should be modeled for simulation accuracy
- **Automatic Gain Control**
  - Maintain a relatively flat output level
  - Should be included for simulation accuracy

DDR Modeling Challenges



Input to DRAM

After Gain & 4 Tap DFE



DFE Clocked by DQS:

- Correlated Jitter on DQ & DQS cancels out
- Uncorrelated Jitter on DQS is transferred to DQ

Single-Ended Signal

Asymmetric Eye:
Rise Time ≠ Fall Time

Asymmetric Eye:
Crossing Points are shifted in the Equalized Eye

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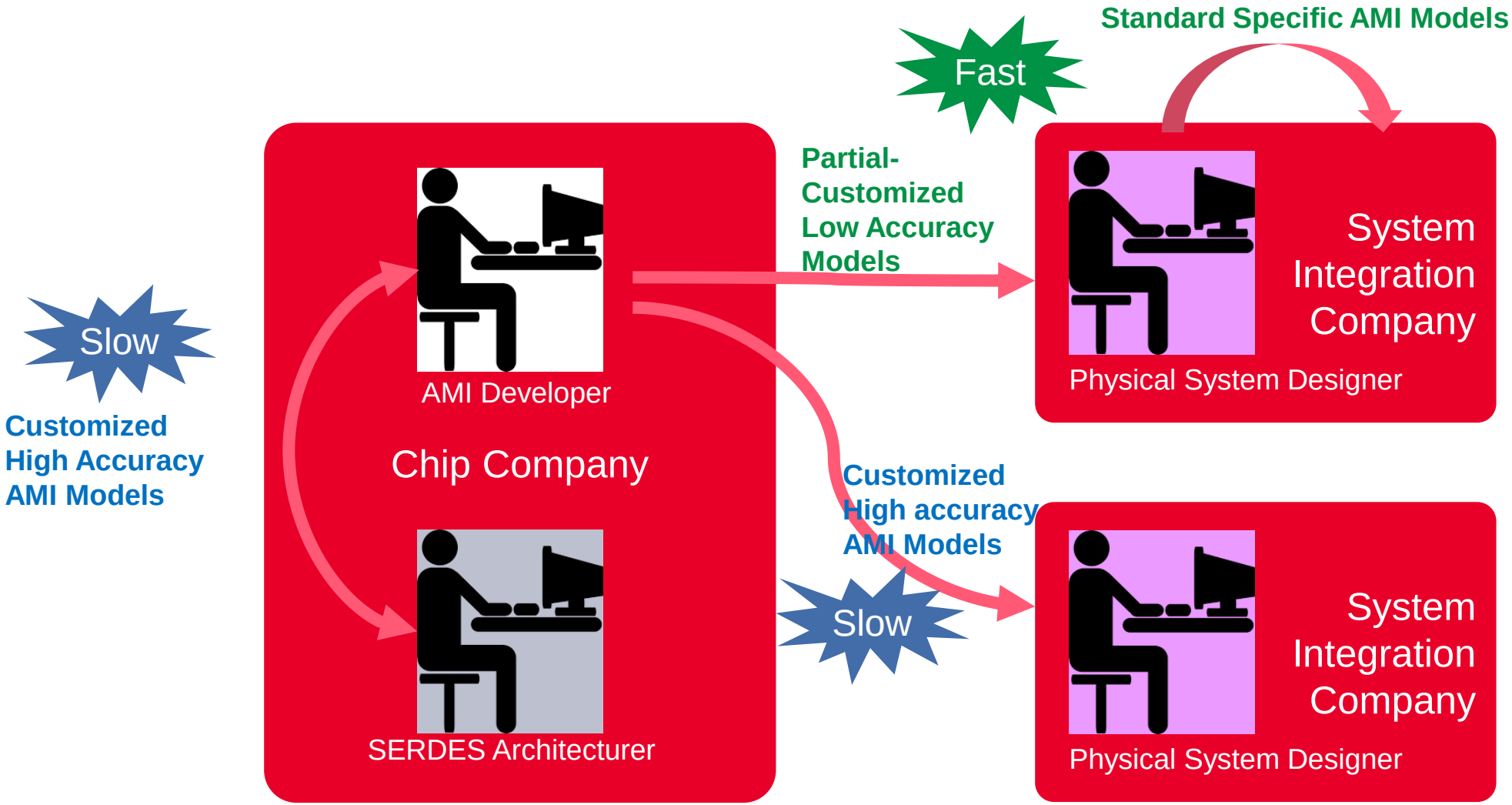
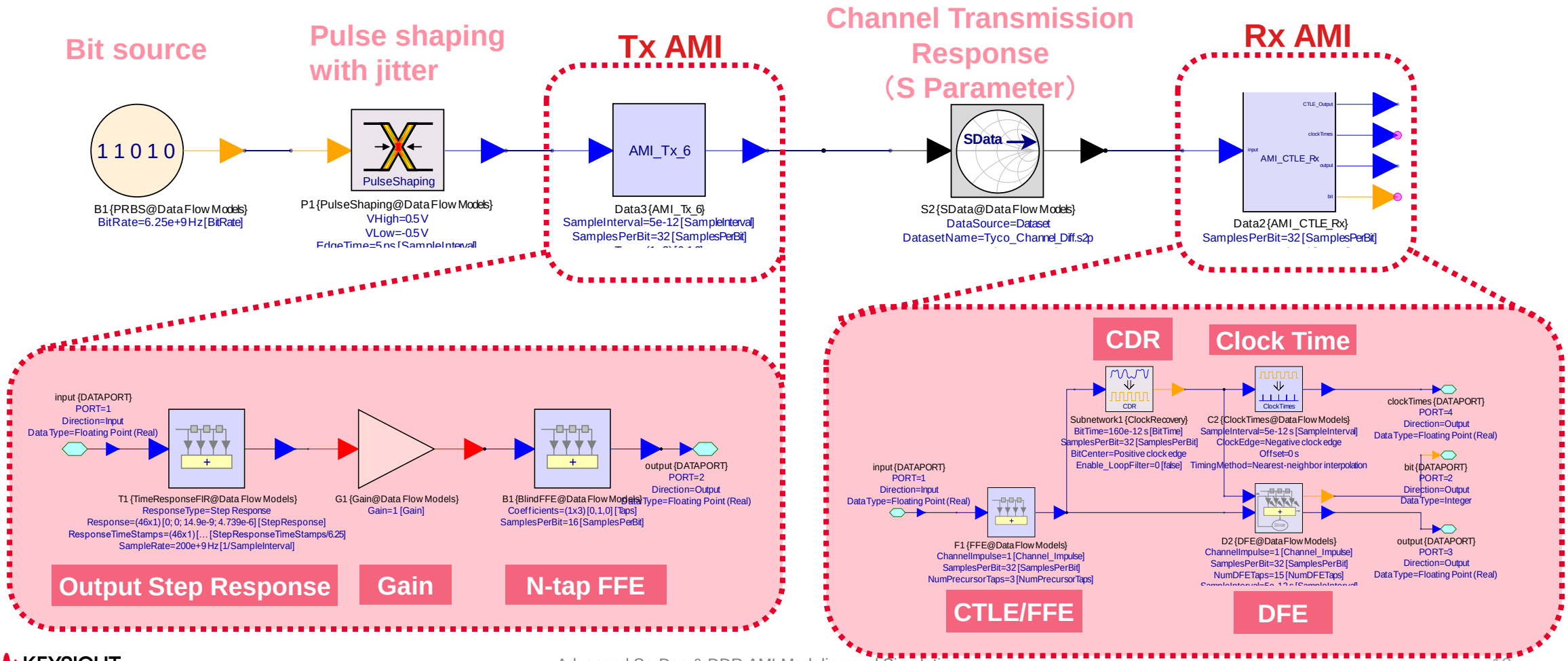
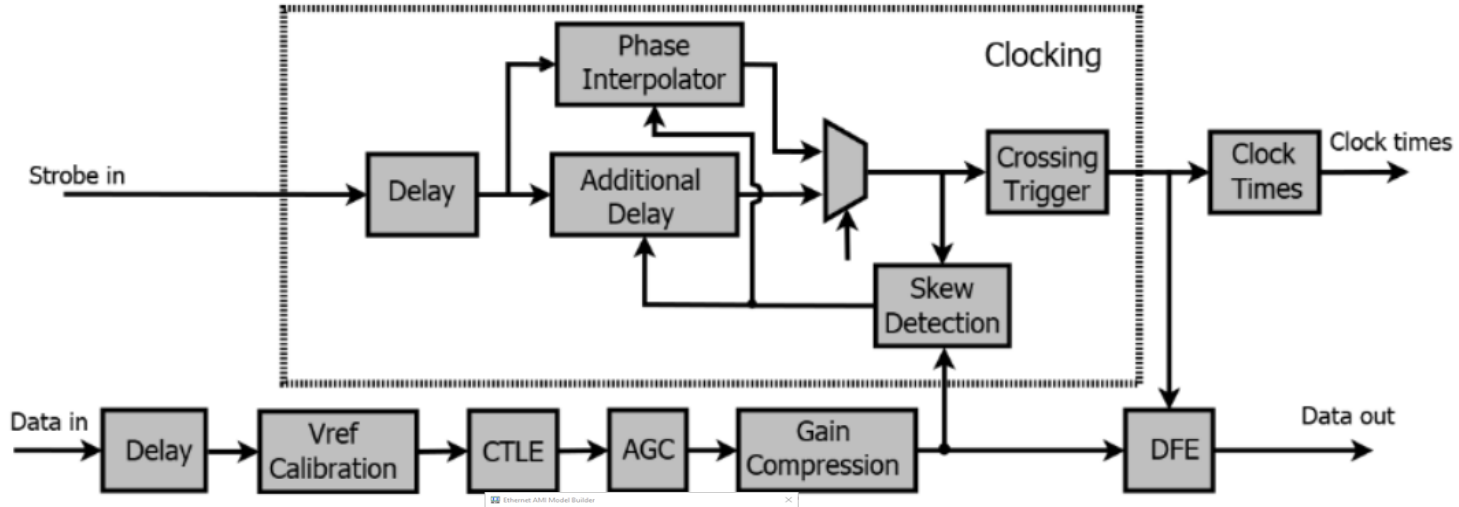
Designer Faced Questions?

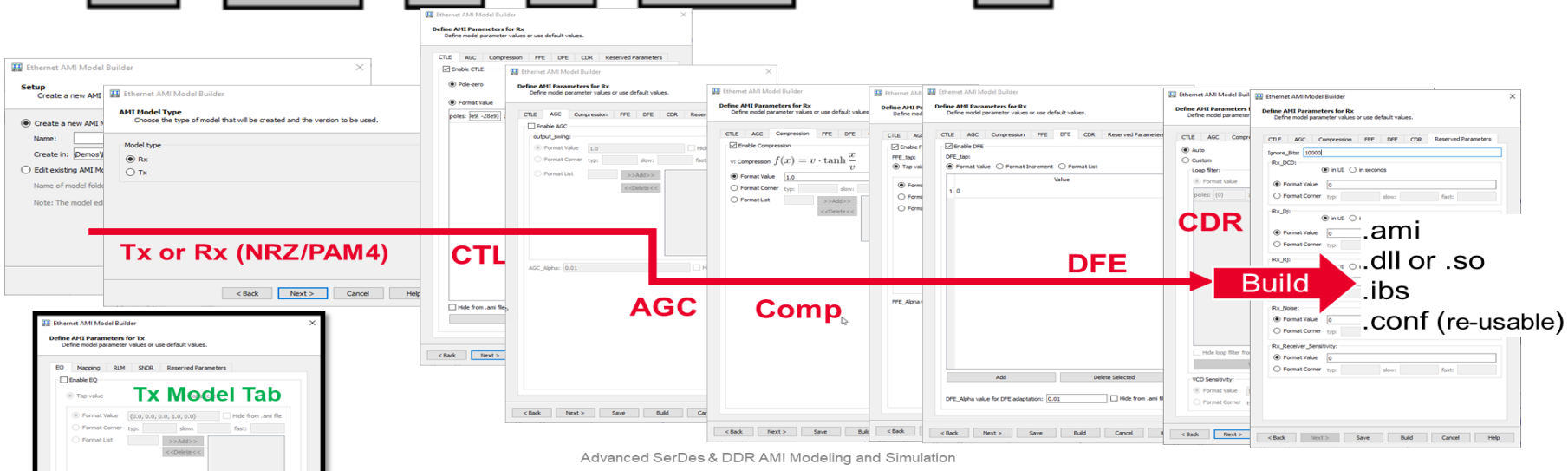


Model-Based AMI Modeling Platform – EDA Tool



Wizard-Driven AMI Modeler – EDA Tool





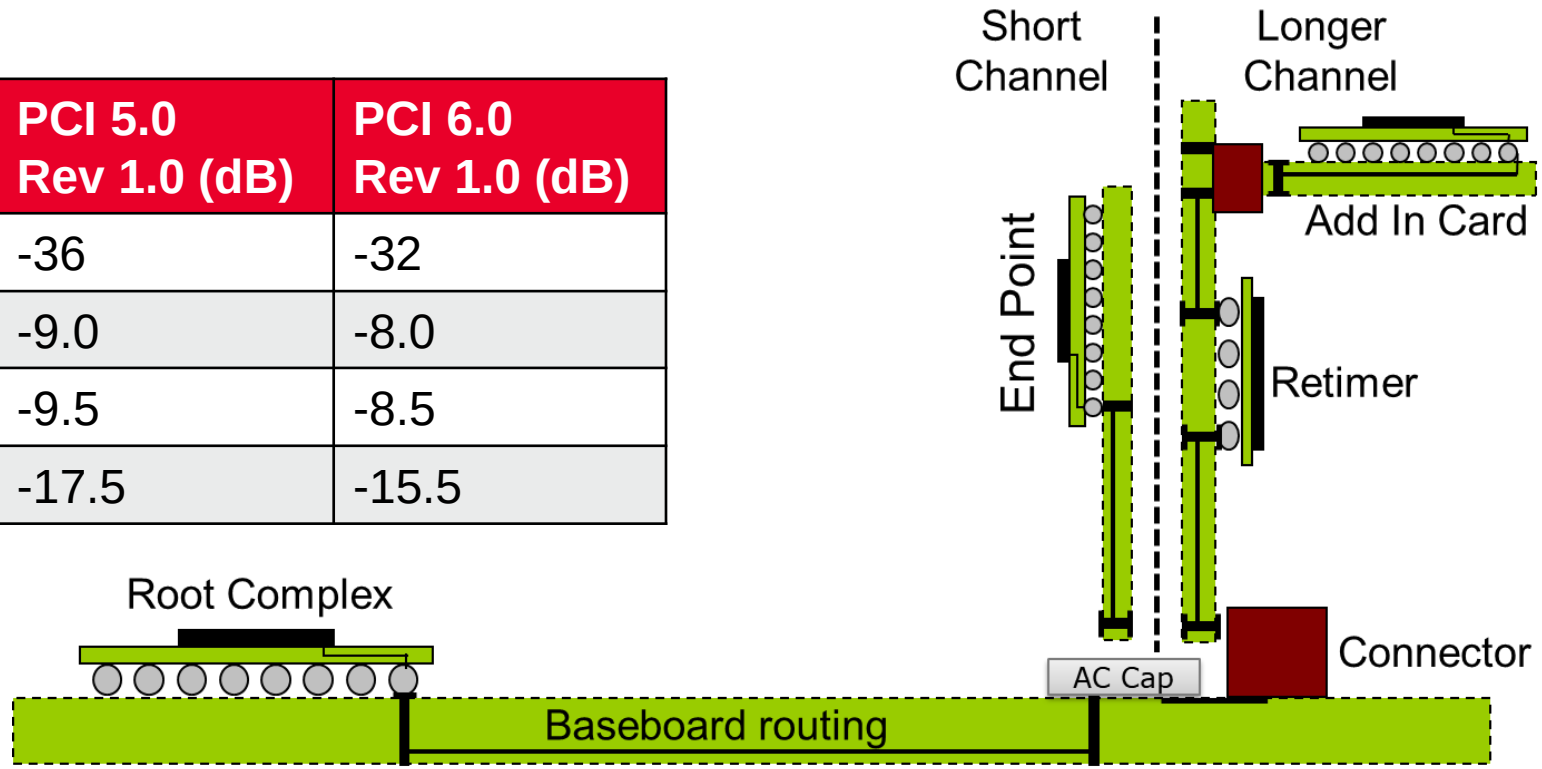
For PAM-n Tx:

- RLM
- SNDR

Compliance Simulation for PCIe

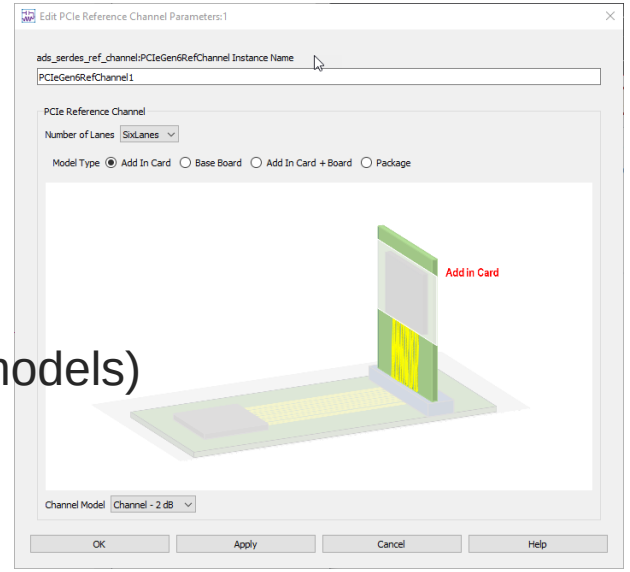
- Pad-to-Pad loss and system routing length
- PAM4
- Reference clock jitter

Loss Parameters	PCI 5.0 Rev 1.0 (dB)	PCI 6.0 Rev 1.0 (dB)
Pad-to-Pad Loss at 16Hz	-36	-32
Root Complex Pkg (RC)	-9.0	-8.0
Add-in-Card (AIC)	-9.5	-8.5
System Trace Loss (RC)	-17.5	-15.5

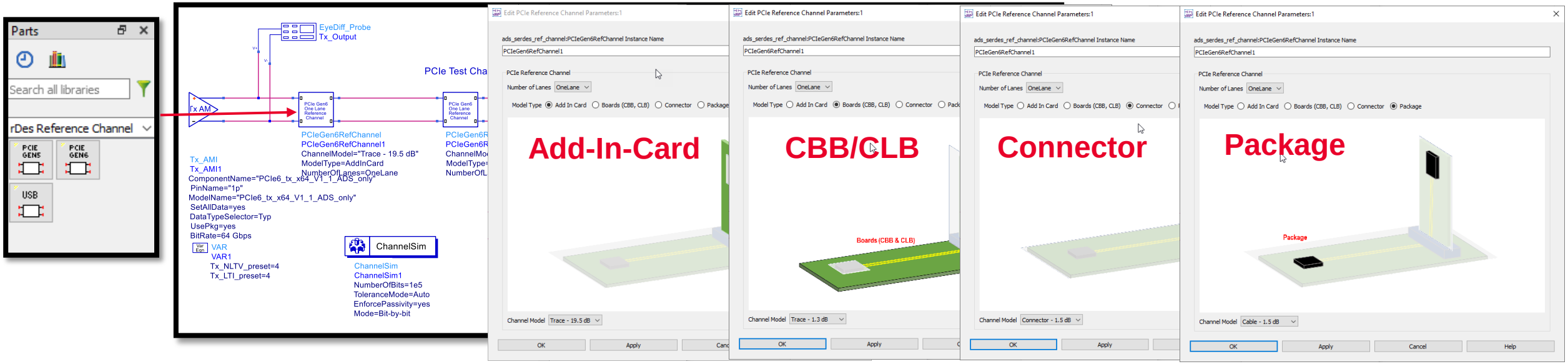


PCIe Reference Channel

AIC,CBB/CLB, Connector, Package models

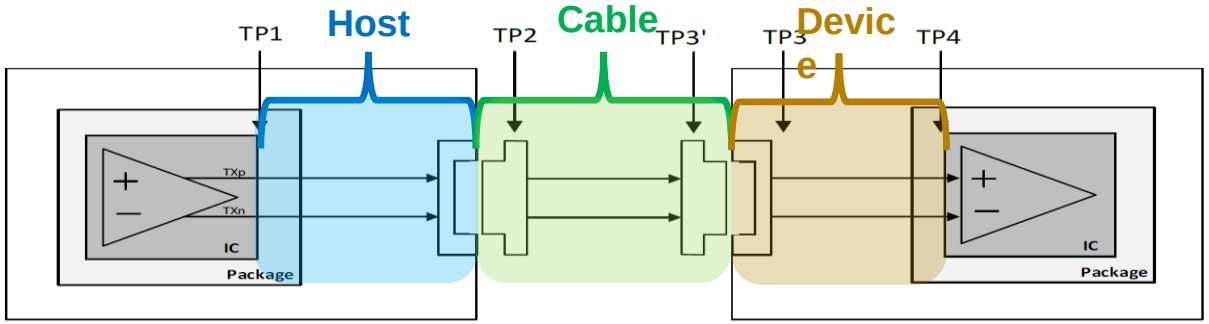


- Provides PCIe Gen5/Gen6 reference channel models (Single-Lane and 6-Lane models)
  - Add-In-Card, CBB/CLB, Connector, and Package models
- Visual aid for a model selection
- IBIS-AMI model maker

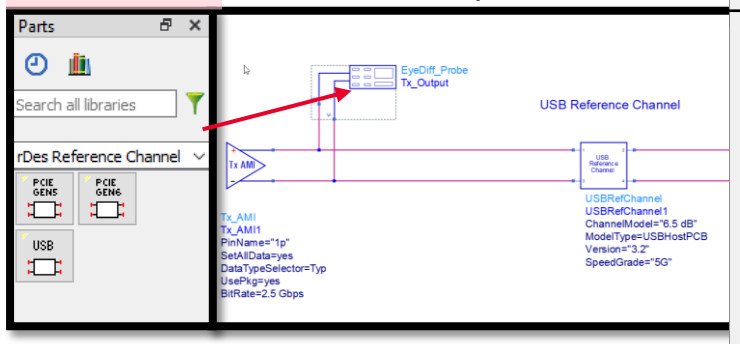


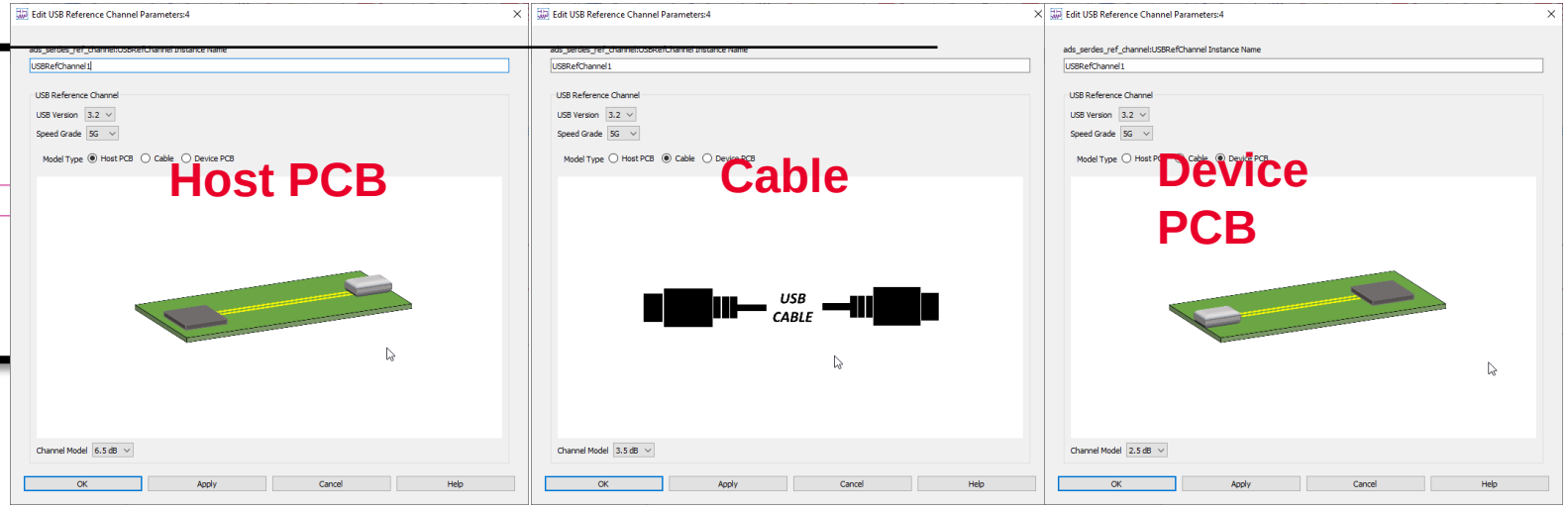
USB Reference Channel

Host PCB, Cable, and Device PCB models

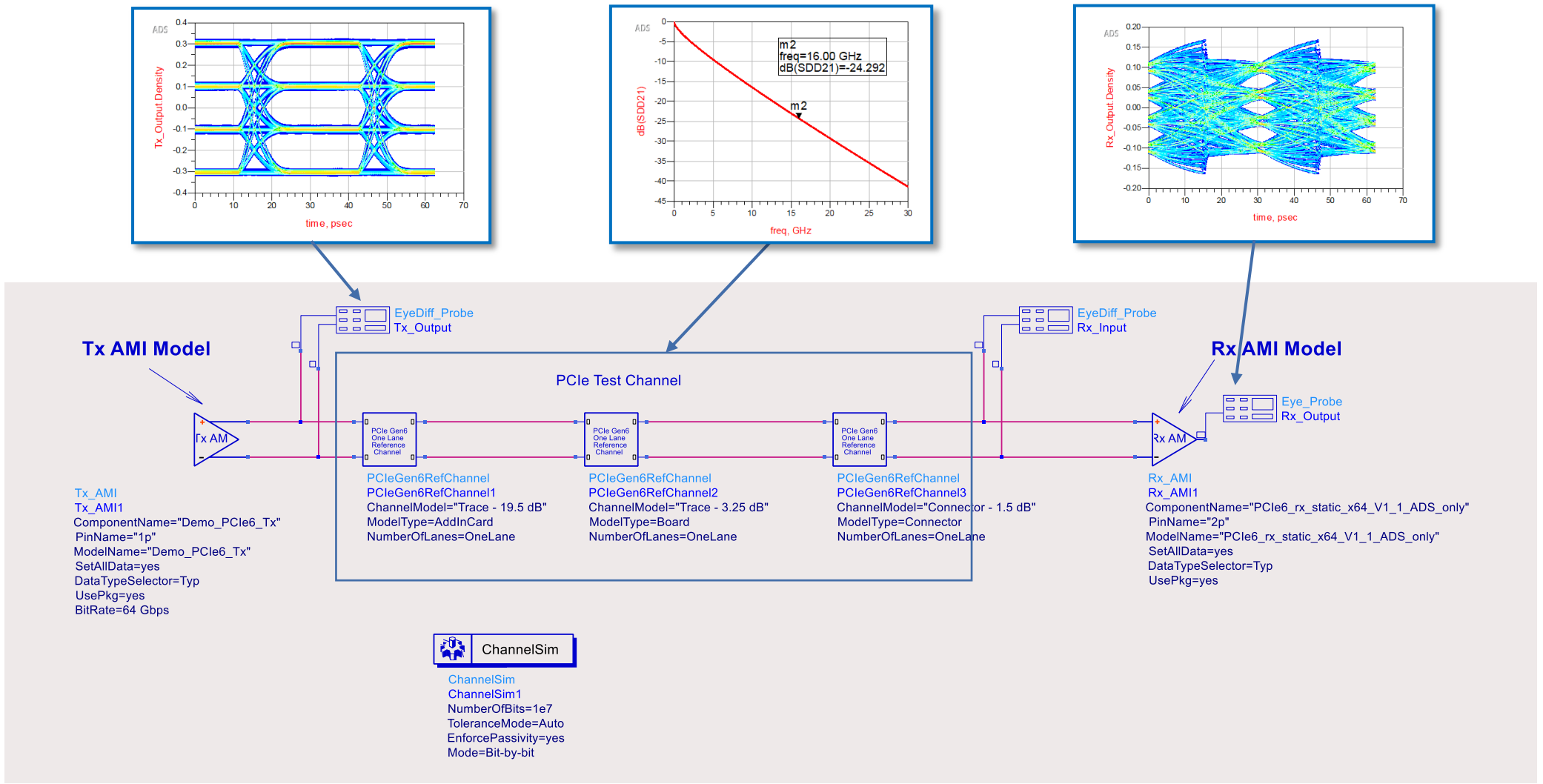


	Speed	Total Loss Budget (dB)	Host (dB)	Cable (dB)	Device(dB)
USB4	10 Gbps (Gen2)	23	5.5	12	5.5
	20 Gbps (Gen3)	22.5	7.5	7.5	7.5
USB3.2	10 Gbps	23	8.5	6	8.5
	5 Gbps (Type C-C connector)	20	6.5	7	6.5



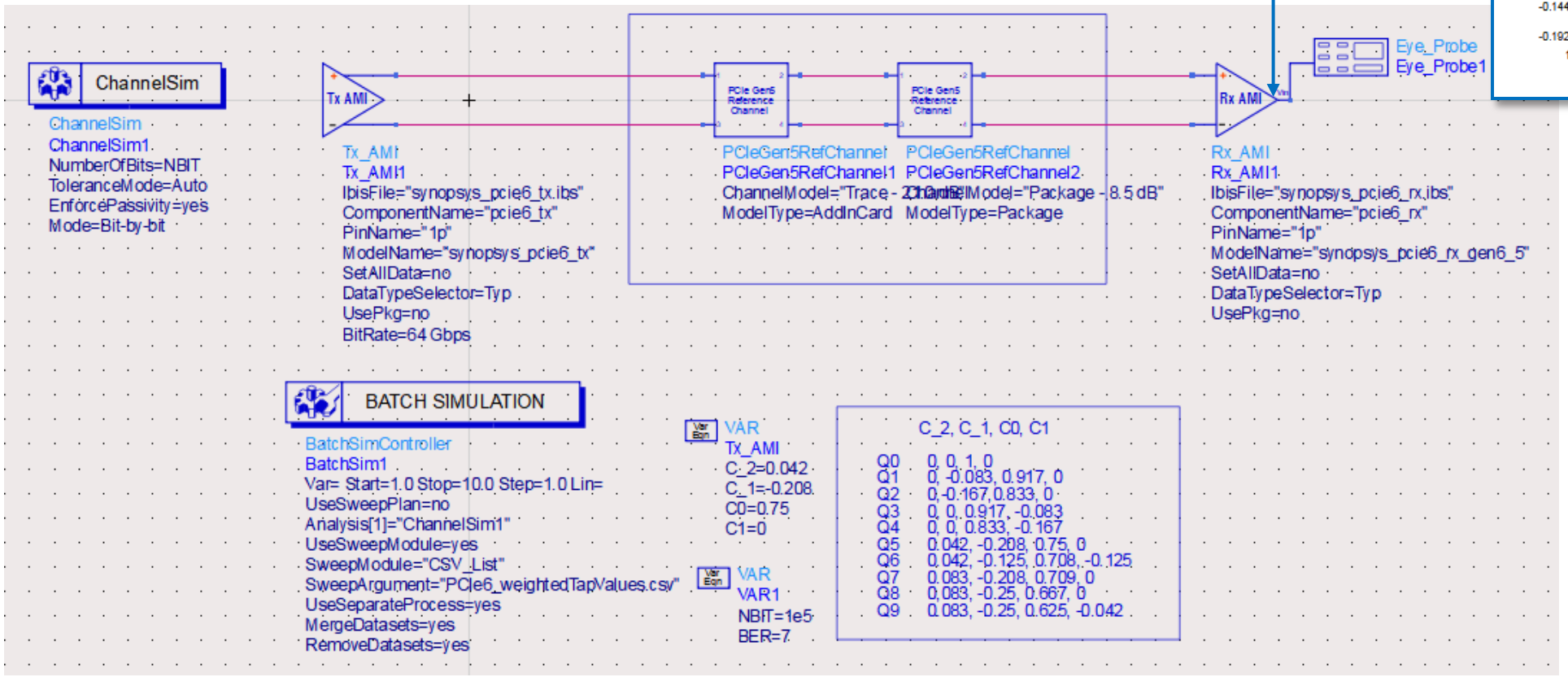


Example: PCIe 6.0 End to End Simulation

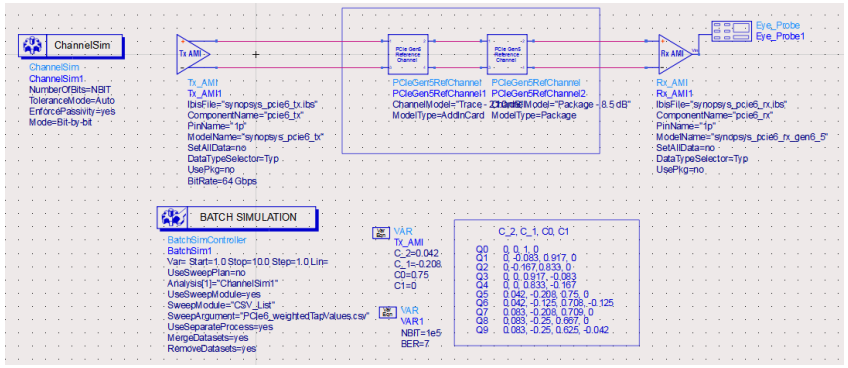


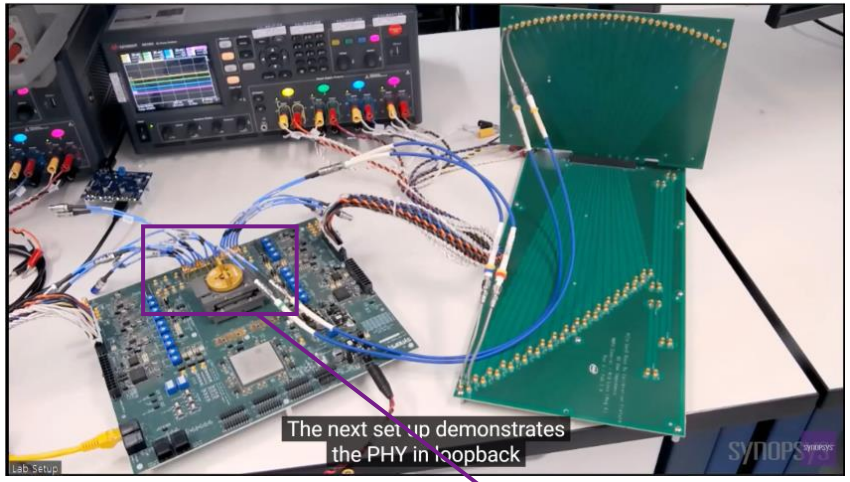
Example: PCIe 6.0 Simulation vs. Measurement Correlation

- PCIe 6.0 Simulation



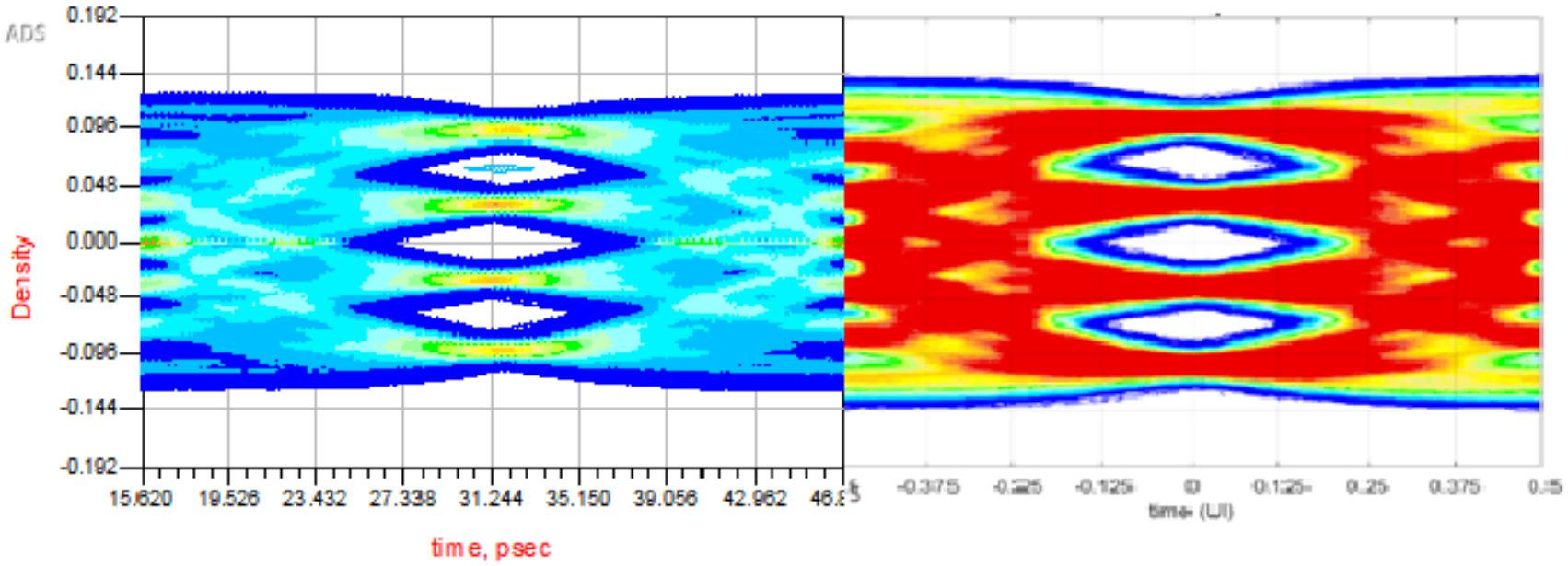
Example: PCIe 6.0 Simulation vs. Measurement Correlation





Synopsys DesignWare® PCIe 6.0 PHY IP

EDA Tool



Silicon Eye

Support Rx_Use_Clock_Input for PAM-n

Previously, GetWave2, Keysight Proprietary IP

- AMI was developed for SerDes, for embedded clocking
- Memory systems use clock forwarding with a separate clock signal DQS, RDQS, or WCK
- BIRD 209 (2021) was accepted and ratified in IBIS 7.1 to support the clock-forwarding technology with Rx_Use_Clock_Input
- Previously GetWave2, the true support of clock forwarding, only supported NRZ modulation
- Rx_Use_Clock_Input for any modulations, PAM3, PAM4, PAM6, PAM8, PAM16, etc.

No clock forwarding (for SE)

Function: **AMI_GetWave**
Required: No
Declaration:

```
long AMI_GetWave (double *wave,
        long wave_size,
        double *clock_times,
        char **AMI_parameters_out,
        void *AMI_memory)
```

BIRD 209 was proposed

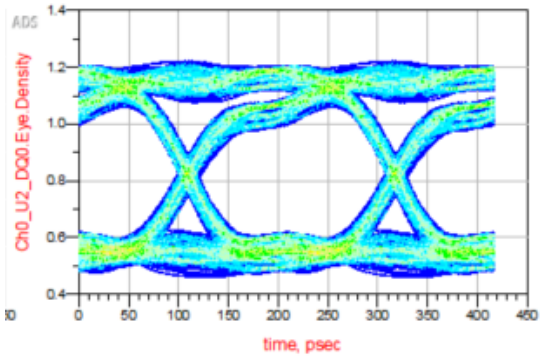
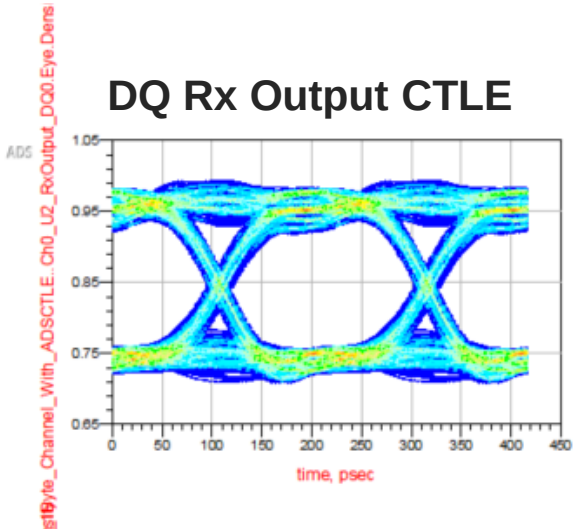
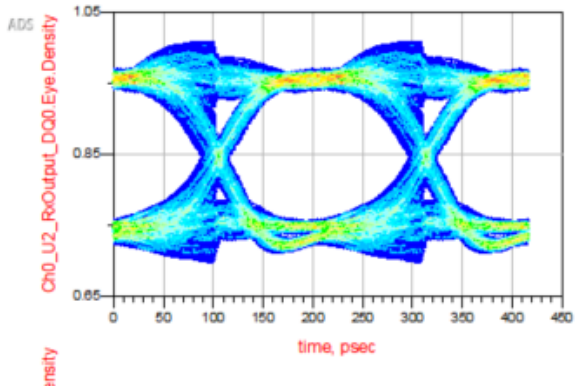
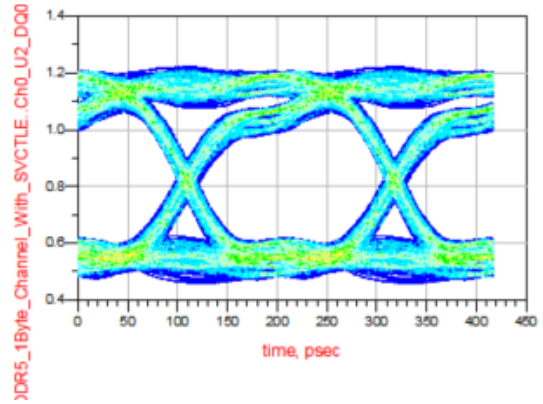
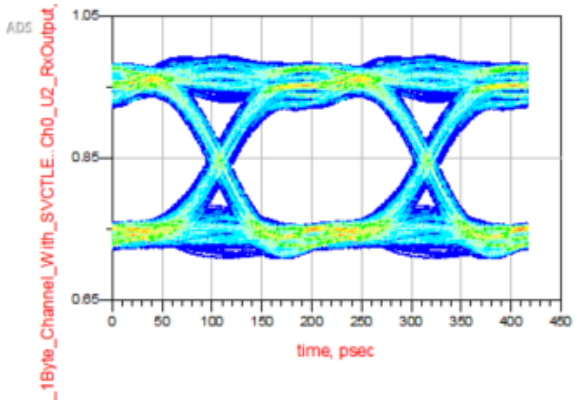
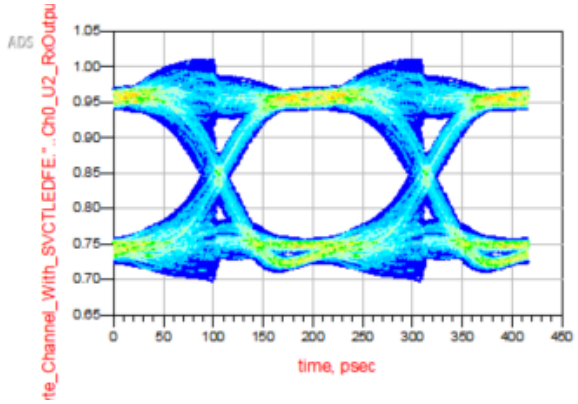
Parameter: **Rx_Use_Clock_Input**
Required: No, and illegal before AMI_Version 7.1
Direction: Rx
Descriptors:

Usage:	In
Type:	String
Format:	List, Value
Default:	<string_literal>
Description:	<string>

"None", "Times" and "Wave"

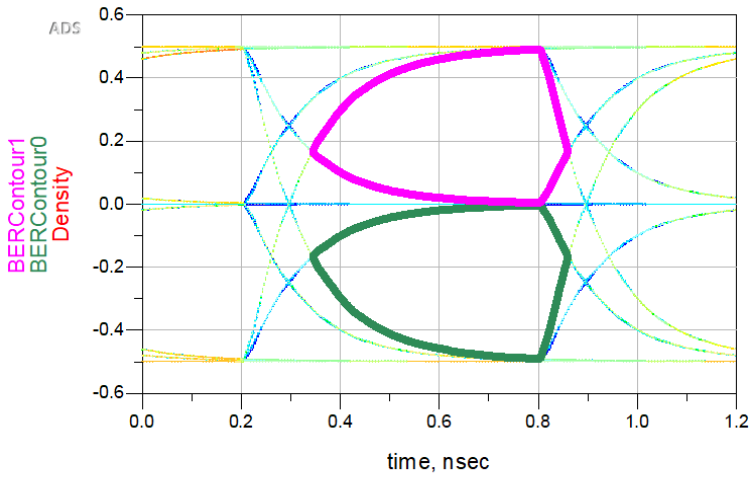
Example: Comparison of model simulation results generated by 2 methods

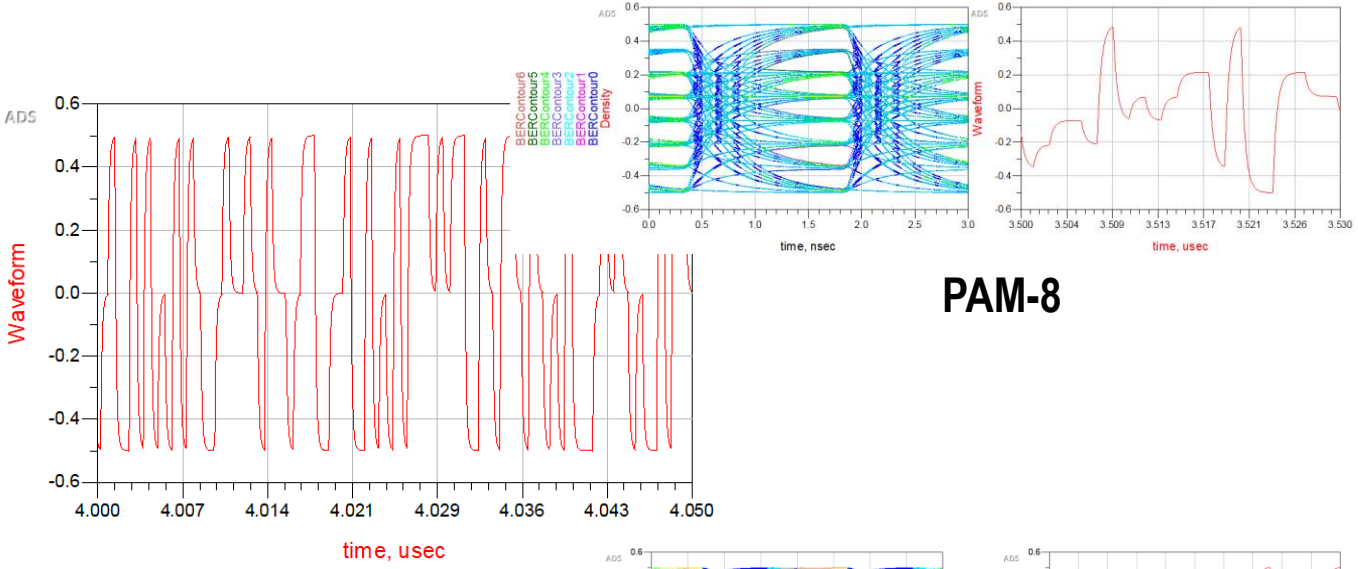
CTLE + DFE

	DQ Rx Package	DQ Rx Output CTLE	DQ Rx Output CTLE+DFE
Wizard-Driven Modeling Tool			
Model-Based Modeling Tool			

Other Modulation Levels

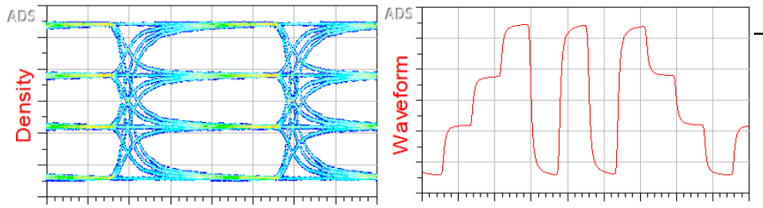
- Channel Simulator supports Various Multi-Level Signaling Methodologies
  - PAM-2 (NRZ)
  - PAM-3
  - PAM-4
  - PAM-6
  - PAM-8
  - PAM-16



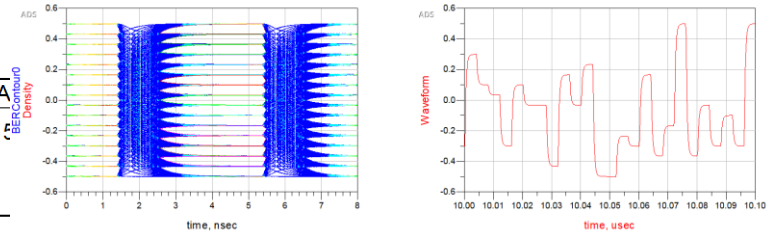


PAM-8

BER	...robe1.HeightAtBERList	...robe1.HeightAtBERList	...robe1.WidthAtBERList	...robe1.WidthA
1.000E-6	0.486	0.486	5.160E-10	5



PAM-4



PAM-16

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- Development Trends & Challenges in High-Speed Digital Design
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- **Summary**

Summary

- Multi-Level Signaling
- Spec Compliant AMI Model Builder
  - PCI Express 6.0, DDR5/LPDDR5, GDDR6x/7, USB4, Ethernet
- AMI Model Compliance Simulation
- Simulation to Measurement Correlation

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Thank you