Advanced SerDes & DDR AMI Modeling and Simulation

Chuanbao Li  Jiarui WU  Xiuguo Jiang
Keysight Technologies

Asian IBIS Summit (Shanghai)
November 10, 2023
Agenda

• Development Trends & Challenges in High-Speed Digital Design

• Modeling and Simulation Challenges

• AMI Modeling and Simulation Solutions

• Summary
Development Trends & Challenges in High-Speed Digital Design

Acceleration of Innovation

• Increased speed means increased complexity
• New design and measurement challenges are here
• No sign of slowing…

PCIe 1.0 (2.5 GT/s)
2003

PCIe 2.0 (5 GT/s)
2006

PCIe 3.0 (8 GT/s)
2010

PCIe 4.0 (16 GT/s)
2017

PCIe 5.0 (32 GT/s)
2019

PCIe 6.0 (64 GT/s)
2022

PCIe 7.0 (128 GT/s)
2024-2025

Advanced SerDes & DDR AMI Modeling and Simulation
Development Trends & Challenges in High-Speed Digital Design

PAM-n modulation

Multi-Level Signaling Methodologies: PAM-2(NRZ), PAM-3, PAM-4, PAM-8, PAM16

- PCIe6/PCle7
- Ethernet
- GDDR6X

- USB4 V2
- GDDR7

- MIPI A-PHY
PAM-n Signaling Benefits and Challenges

Benefits
• PAM-n improves transmission efficiency
• PAM-n could reduce bandwidth limitation

Challenges
• 1/3 reduction in amplitude (9 dB SNR degradation)
• ~ 33% UI timing loss due to level transitions

Sensitivity to noise (xtalk, reflection, and other noise sources) is a key challenge.

<table>
<thead>
<tr>
<th></th>
<th>Nyquist Frequency</th>
<th>Insertion Loss</th>
<th>Signal Mapping</th>
<th>Baud Rate</th>
<th>Bit Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>NRZ (PAM-2)</td>
<td>10 GHz</td>
<td>22.5 dB</td>
<td>1 bit to 1 symbol</td>
<td>20 Gbaud/s</td>
<td>20 Gbps</td>
</tr>
<tr>
<td>PAM-3</td>
<td>10 GHz</td>
<td>22.5 dB</td>
<td>3 bits to 2 symbols</td>
<td>20 Gbaud/s</td>
<td>30 Gbps</td>
</tr>
<tr>
<td>PAM-4</td>
<td>10 GHz</td>
<td>22.5 dB</td>
<td>2 bits per symbol</td>
<td>20 Gbaud/s</td>
<td>40 Gbps</td>
</tr>
<tr>
<td>PAM-8</td>
<td>10 GHz</td>
<td>22.5 dB</td>
<td>4 bits per symbol</td>
<td>20 Gbaud/s</td>
<td>80 Gbps</td>
</tr>
</tbody>
</table>
Agenda

• Development Trends & Challenges in High-Speed Digital Design

• Modeling and Simulation Challenges

• Modeling and Simulation Insights

• Summary
PAM-N Modeling Challenges

Transmitter Linearity, Noise and Distortions

• **RLM (Level Separation Mismatch Ratio)** \( R_{LM} \)
  - Identify **transmitter nonlinearity**.
  - Verify linear spacing of the PAM-N levels
  - Ideal PAM4: \{-0.5, -1/6, 1/6, 0.5\}
  - Assuming non-ideal mapping table is \{\(V_0\), \(V_1\), \(V_2\), \(V_3\)\}

\[
\begin{align*}
V_{\text{mid}} &= \frac{(V_0 + V_3)}{2} \\
ES_1 &= \frac{(V_1 - V_{\text{mid}})}{(V_0 - V_{\text{mid}})} \\
ES_2 &= \frac{(V_2 - V_{\text{mid}})}{(V_3 - V_{\text{mid}})} \\
R_{LM} &= \min((3*ES_1), (3*ES_2), (2 - 3*ES_1), (2 - 3*ES_2))
\end{align*}
\]

• **SNDR (Signal to Noise and Distortion Ratio)**
  - Distortion: Introduced by level mismatch.
  - Noise: Uncorrelated RMS amplitude noise of each symbol level

\[
SNDR = 10\log_{10}\left(\frac{P_{\text{max}}^2}{\sigma_e^2 + \sigma_n^2}\right)
\]
PAM-N Modeling Challenges

Receiver Non-linearity

• **Gain Compression**
  • Output/input relationship
  • Causes reduction of gain
  • Should be modeled for simulation accuracy

• **Automatic Gain Control**
  • Maintain a relatively flat output level
  • Should be included for simulation accuracy
Supporting Parallel, Single-Ended Signals with External Clocks

**DDR Modeling Challenges**

**Input to DRAM**

- 1.1V
- 0.55V

**After Gain & 4 Tap DFE**

- Single-Ended Signal
- Asymmetric Eye: Rise Time ≠ Fall Time

**DFE Clocked by DQS**:

- Correlated Jitter on DQ & DQS cancels out
- Uncorrelated Jitter on DQS is transferred to DQ

**Asymmetric Eye: Crossing Points are shifted in the Equalized Eye**
Agenda

• Development Trends & Challenges in High-Speed Digital Design

• Modeling and Simulation Challenges

• Modeling and Simulation Insights

• Summary
Designer Faced Questions?

- AMI Developer
- Chip Company
- SERDES Architecturer
- System Integration Company
- Physical System Designer

Customized High Accuracy AMI Models
Partial-Customized Low Accuracy Models
Standard Specific AMI Models

Fast
Slow
Model-Based AMI Modeling Platform – EDA Tool

Advanced SerDes & DDR AMI Modeling and Simulation
Wizard-Driven AMI Modeler – EDA Tool

For PAM-n Tx:
- RLM
- SNDR
Compliance Simulation for PCIe

• Pad-to-Pad loss and system routing length
• PAM4
• Reference clock jitter

<table>
<thead>
<tr>
<th>Loss Parameters</th>
<th>PCI 5.0 Rev 1.0 (dB)</th>
<th>PCI 6.0 Rev 1.0 (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pad-to-Pad Loss at 16Hz</td>
<td>-36</td>
<td>-32</td>
</tr>
<tr>
<td>Root Complex Pkg (RC)</td>
<td>-9.0</td>
<td>-8.0</td>
</tr>
<tr>
<td>Add-in-Card (AIC)</td>
<td>-9.5</td>
<td>-8.5</td>
</tr>
<tr>
<td>System Trace Loss (RC)</td>
<td>-17.5</td>
<td>-15.5</td>
</tr>
</tbody>
</table>
PCle Reference Channel
AIC,CBB/CLB, Connector, Package models

- Provides PCle Gen5/Gen6 reference channel models (Single-Lane and 6-Lane models)
- Add-In-Card, CBB/CLB, Connector, and Package models
- Visual aid for a model selection
- IBIS-AMI model maker
## USB Reference Channel

Host PCB, Cable, and Device PCB models

<table>
<thead>
<tr>
<th>Speed</th>
<th>Total Loss Budget (dB)</th>
<th>Host (dB)</th>
<th>Cable (dB)</th>
<th>Device (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>USB4</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 Gbps (Gen2)</td>
<td>23</td>
<td>5.5</td>
<td>12</td>
<td>5.5</td>
</tr>
<tr>
<td>20 Gbps (Gen3)</td>
<td>22.5</td>
<td>7.5</td>
<td>7.5</td>
<td>7.5</td>
</tr>
<tr>
<td><strong>USB3.2</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 Gbps</td>
<td>23</td>
<td>8.5</td>
<td>6</td>
<td>8.5</td>
</tr>
<tr>
<td>5 Gbps (Type C-C connector)</td>
<td>20</td>
<td>6.5</td>
<td>7</td>
<td>6.5</td>
</tr>
</tbody>
</table>

Advanced SerDes & DDR AMI Modeling and Simulation
Example: PCIe 6.0 End to End Simulation
Example: PCIe 6.0 Simulation vs. Measurement Correlation

- PCIe 6.0 Simulation
Example: PCIe 6.0 Simulation vs. Measurement Correlation

EDA Tool

Silicon Eye

Synopsys DesignWare® PCIe 6.0 PHY IP
Support Rx_Use_Clock_Input for PAM-n

Previously, GetWave2, Keysight Proprietary IP

- AMI was developed for SerDes, for embedded clocking
- Memory systems use clock forwarding with a separate clock signal DQS, RDQS, or WCK
- BIRD 209 (2021) was accepted and ratified in IBIS 7.1 to support the clock-forwarding technology with Rx_Use_Clock_Input
- Previously GetWave2, the true support of clock forwarding, only supported NRZ modulation
- Rx_Use_Clock_Input for any modulations, PAM3, PAM4, PAM6, PAM8, PAM16, etc.
Example: Comparison of model simulation results generated by 2 methods

CTLE + DFE

Wizard-Driven Modeling Tool

Model-Based Modeling Tool
Other Modulation Levels

- Channel Simulator supports Various Multi-Level Signaling Methodologies
  - PAM-2 (NRZ)
  - PAM-3
  - PAM-4
  - PAM-6
  - PAM-8
  - PAM-16
Agenda

• Development Trends & Challenges in High-Speed Digital Design

• Modeling and Simulation Challenges

• Modeling and Simulation Insights

• Summary
Summary

- Multi-Level Signaling

- Spec Compliant AMI Model Builder
  - PCI Express 6.0, DDR5/LPDDR5, GDDR6x/7, USB4, Ethernet

- AMI Model Compliance Simulation

- Simulation to Measurement Correlation
Thank you