Hardware and AI/ML: Applications of SIPI & IBIS

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Agenda

- Hardware Plays Critical Roles in AI/ML
- Human vs Silicon Evolutions
- SIPI Demands & Challenges
- AI/ML and Hardware Can Help Each Other
- SIPI AI/ML Case Studies
  - Placement optimization of decoupling capacitors
  - PDN Impedance Prediction (CNN-GA)
  - Eye-diagram-metrics prediction with DNN
  - Eye-diagram generation with RNN
- IBIS AI/ML Usage Cases
  - IBIS + AI/ML for SIPI design and simulations
    - IBIS keywords are very useful as AI/ML parameters
  - Use AI/ML to generate more accurate IBIS models
Hardware Plays Critical Roles in AI/ML

AI/ML Algorithm

Hardware

Software

Physical World

Sensors/ Eye/Ear..

Data

CPU/ Brain

AI/ML Algorithms

Actuators/ Hands..

Data
Human Evolution Over Millions Years

3X increase over 6 million years

Reference: How Could Language Have Evolved?DOI:10.1371/journal.pbio.1001934
Silicon Evolution in 42 Years


Figure 20  Tradeoffs in MPU performance after the power limit was reached.

10^7 X increase over 42 years!
Machine vs Living Creatures

Multi-GPU convolutional neural network (2012)


Early back-propagation network (1986)

Perception (1958)

Neural Network Size Grows with Hardware Advancement

Silicon/Hardware is evolving much faster, but still fall behind Human

Ivan Goodfellow et al.
Signal Integrity Demands & Challenges

Relentless Advancement – Switch Silicon Bandwidth

12 Years
7 Switch Generations (80x)
4 SerDes Speeds (10x)
4 Switch Radix Increases (8x)

Switch Silicon BW
640G
1.28T
3.2T
6.4T
12.8T
25.6T
102.4T?

SerDes Speed
10G
28G
56G
112G

# SerDes
x64
x128
x256
x512

Optics
QSFP+
QSFP28
QSFPDD56
QSFPDD800

Figure 3 Relentless advancement – switch silicon bandwidth

Reference: OIF Next Generation CEI-224G Framework
Power Integrity Demands & Challenges

Figure 4 Relentless advancement – 80x BW over 12 years

Reference: OIF Next Generation CEI-224G Framework
Advanced HW AI/ML copilots are expected to significantly improve the hardware design. This will enable a positive feedback loop between Hardware Design and AI/ML applications.
More Advanced Hardware for AI/ML

Current Silicon/Hardware cannot meet exponential growth of AI/ML! nVidia is a $T dollar company now. We need more advanced hardware!
More Powerful AI/ML for Hardware Design

Mark Hayter, Plenary Talk, 2018 IEEE EMC Symposium, Singapore
Case Study: Optimization for Decap Placement (ANN-GA)

Input: decaps value and location

Output: PDN impedance

- The final architecture consists on 3 hidden layer (width of 2, 30 and 2, respectively)
- The output layer has size of 361: the values of $Z_{in}(f)$ at the 361 frequency points of the spectrum
Results of the Optimization

<table>
<thead>
<tr>
<th>Elementary capacitors</th>
<th>C (nF)</th>
<th>ESL (pH)</th>
<th>ESR (mΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C₁</td>
<td>100</td>
<td>222</td>
<td>8.9</td>
</tr>
<tr>
<td>C₂</td>
<td>47</td>
<td>154</td>
<td>21.4</td>
</tr>
<tr>
<td>C₃</td>
<td>22</td>
<td>142</td>
<td>25.2</td>
</tr>
</tbody>
</table>

Pop: 10 chrom  
# gen: 10  
fₘₐₓ: 1 GHz  
iter: 10

![Graphs showing impedance comparison with mask, optimization, and no Decap]
Lab Validations

Decap locations in the real board

$Z_{in}$ at Port 3:
- from ANN-GA
- from measurement
- from simulation
Deep learning to optimize Decap placement given any: board shape, stack-up, IC location, and # of decaps

Two step approach: trained network + fine tune (GA)
Use the predicted solution by the DRL as a seeded solution of the GA
Case Study: PDN Impedance Prediction

Convolutional neural network (CNN) structure:

- Training: 1.3M board
- Testing: 10K board
- Training time: 80 hours (1 NVIDIA Tesla K80 GPU)
Case Study: PDN Impedance Prediction

![Graph showing impedance vs frequency with BEM and DNN methods]

**Table 2: Time comparison**

<table>
<thead>
<tr>
<th>Methods</th>
<th>Case 1</th>
<th>Case 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full-wave simulation</td>
<td>35 min</td>
<td>40 min</td>
</tr>
<tr>
<td>Boundary element</td>
<td>10 s</td>
<td>30 s</td>
</tr>
<tr>
<td>network</td>
<td>0.1 s</td>
<td>0.1 s</td>
</tr>
</tbody>
</table>
Case Study: ML in High-Speed Channel Modeling

 Serializer -> Tx -> Channel -> Rx ->Deserializer

 Clk Generation (PLL) -> Tx

 Clk Recovery -> Rx

 Eye Height

 Eye Width

 Bit Period
Case Study: Eye-diagram-metrics Prediction with DNN

- **Generator** creates a set of input parameters for a high-speed channel, stored in \( \{x\} \).
- **Supervisor** returns eye height or width \( y \) based on \( \{x\} \).
- The learning process is essentially the selection of the right regression function \( f(\{x\}, \{\theta\}) \) where \( \{\theta\} \) contains the parameters to be learned, such that the prediction made by \( f(\{x\}, \{\theta\}) \) approximates the value returned by the supervisor uniformly over all possible input \( \{x\} \).
- **Regression method** in this work includes linear, support vector, and DNN regressions.
Case Study: Eye-diagram-metrics Prediction with RNN

RNN Unit

\{h^{t-1}\} \rightarrow \{h^t\} \rightarrow \{x^t\}

LSTM Unit

\{c^{t-1}\} \rightarrow \{c^t\} \rightarrow \{x^t\} \rightarrow \{h^{t-1}\} \rightarrow \{h^t\}

Start

1. Transient Iterations
2. Newton-Raphson Iterations
3. Solving Linear System

- Nonlinear Convergence
  - Yes
  - All Time Steps
    - Yes
    - End
  - No

- Yes

- No
Eye Diagram Generation with a PAM4 Example

Circuit Simulator

LSTM Network

IBIS + AI/ML for SIPI Design and Simulations

• **IBIS keywords** are very useful as AI/ML input parameters

• This is an active research field and here are some publications:

  • Comparison of Machine Learning Techniques for Predictive Modeling of High-Speed Links, Hanzhi Ma; Er-Ping Li; Andreas C. Cangellaris; Xu Chen, 2019 IEEE 28th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)
  • Self-Evolution Cascade Deep Learning Model for High-Speed Receiver Adaptation, Bowen Li; Brandon Jiao; Chih-Hsun Chou; Romi Mayder; Paul Franzon, IEEE Transactions on Components, Packaging and Manufacturing Technology, Year: 2020 | Volume: 10, Issue: 6
Use AI/ML to generate more accurate IBIS models

- This is a relatively new research field, and it belongs to generative AI.

- Presentation from Prof Huang at the Hybrid IBIS Summit at 2023 IEEE Symposium on EMC+SIPI

**USB3.0 IBIS-AMI Model Construction based on Measurement and Neural Network**

Jiahuan Huang (Missouri S&T EMC Lab, USA)
Junho Joo (Missouri S&T EMC Lab, USA)
Hank Lin (ASUS, Taiwan)
Bin-Chyi Tseng (ASUS, Taiwan)
Will Chan (ASUS, Taiwan)
Chulsoon Hwang (Missouri S&T EMC Lab, USA)

[Presented by Jiahuan Huang]
THANK YOU!
&
QUESTIONS?

Please contact me at
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Abbreviations

- GA: Genetic Algorithm
- ANN: Artificial Neural Network
- CNN: Convolutional Neural Network
- RNN: Recurrent Neural Network
- DNN: Deep Neural Networks
- LSTM: Long Short-Term Memory
Publications

[A] Stefano Piersanti, Riccardo Cecchetti, Carlo Olivieri; Francesco de Paulis; Antonio Orlandi; Markus Bueker, **Decoupling Capacitors Placement at Board Level Adopting a Nature-Inspired Algorithm**, in Electronics 2019, Volume 8, Issue 7, October 2019, available online: [https://www.mdpi.com/2079-9292/8/7/737/pdf](https://www.mdpi.com/2079-9292/8/7/737/pdf)

[B] Francesco de Paulis; Riccardo Cecchetti; Carlo Olivieri; Stefano Piersanti; Antonio Orlandi; Markus Bueker, **Efficient Iterative Process based on an Improved Genetic Algorithm for Decoupling Capacitor Placement at Board Level**, in Electronics 2019, Volume 8, Issue 11, available online: [https://www.mdpi.com/2079-9292/8/11/1219/pdf](https://www.mdpi.com/2079-9292/8/11/1219/pdf)


