Efficient time-domain noise analysis method

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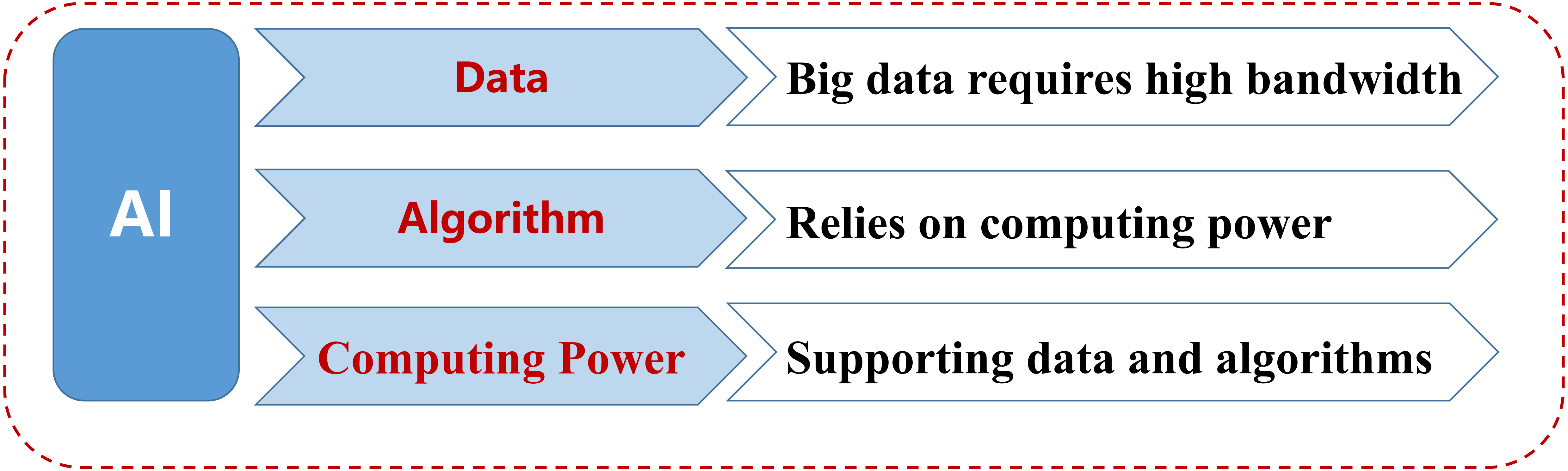
Outline

1. **PI Challenges in High-Power Computing Scenarios**
2. **Efficient time-domain noise analysis method**

- **Analytical calculation for the standard deviation of voltage noise**
- **The method of calculating of the worst-case voltage noise**
- **The method of calculating the statistical distribution of voltage noise**

1. PI Challenges in High-Power Computing Scenarios

In the 4th industrial revolution, AI is the core driving force.



AI

- **Data** → Big data requires high bandwidth
- **Algorithm** → Relies on computing power
- **Computing Power** → Supporting data and algorithms

Driven by Moore's Law, the improvement in AI hardware computing power is the most crucial factor for the development of artificial intelligence!

1. PI Challenges in High-Power Computing Scenarios

- What is the core issue that needs to be addressed during the process of enhancing computing power?

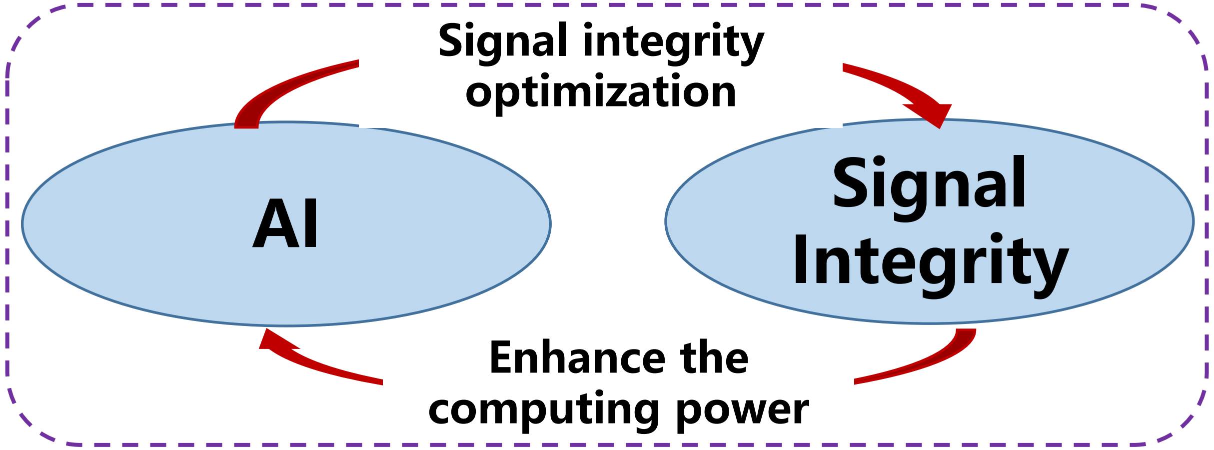
The data transmission between nodes is the bottleneck that restricts computing power.

↓

High-quality high-speed interconnection

↓

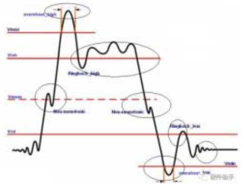
Signal Integrity



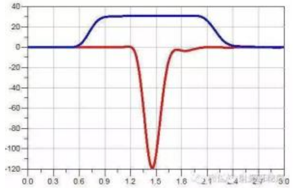
1. PI Challenges in High-Power Computing Scenarios

High-Power Computing Scenarios

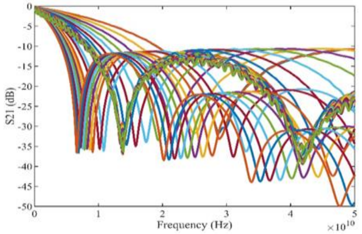
SI



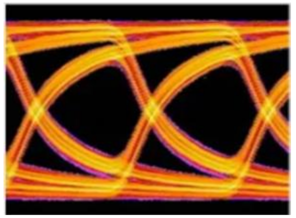
Reflection



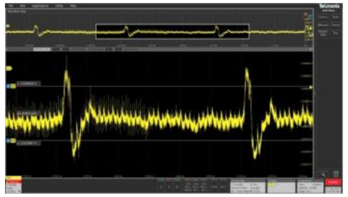
Crosstalk



Loss

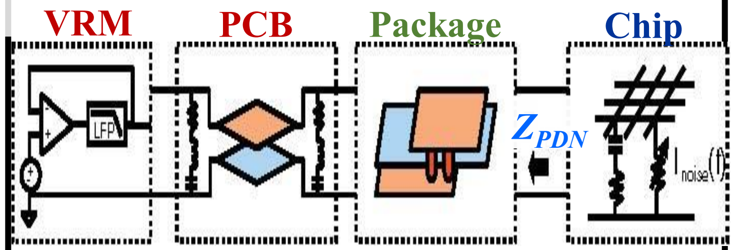


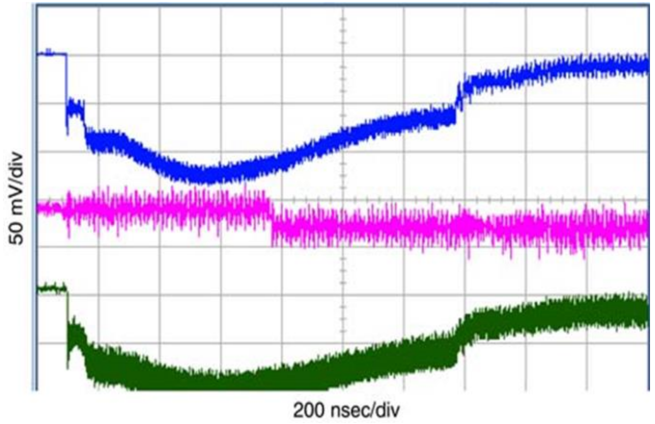
Jitter



Noise

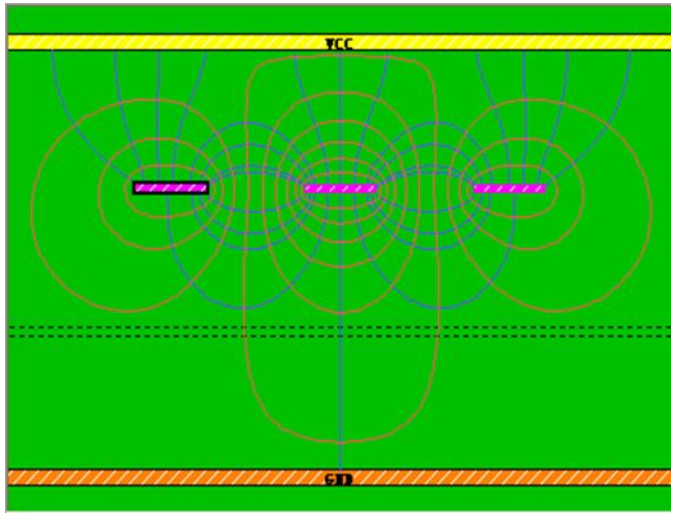
PI





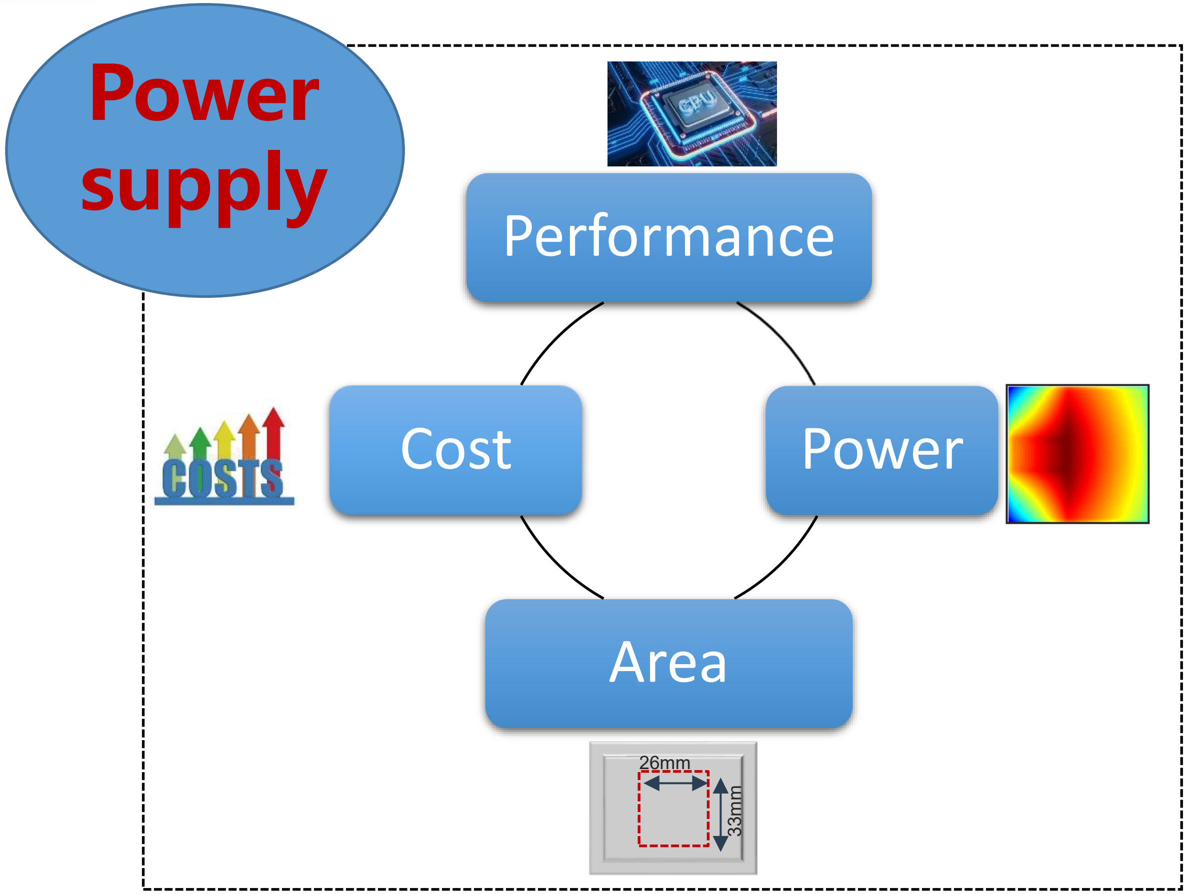
Rail collapse **Ripple**

EMI



EMC **EMI**

1. PI Challenges in High-Power Computing Scenarios



Power supply

Performance

Cost

Power

Area

Signal integrity

Heat dissipation

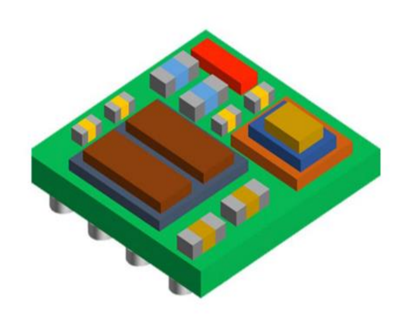
Warping

PDN quality

- **The power distribution network (PDN) is the largest and most complex interconnection structure in a chip (About for 40% - 60%).**

1. PI Challenges in High-Power Computing Scenarios

AI chips



High computational power--》 High power consumption

High integration level--》 Not enough area for decoupling

Complex operating modes--》 Current imbalance

More power rails--》 Complex coupling

Induce numerous difficulties in the power integrity design process.

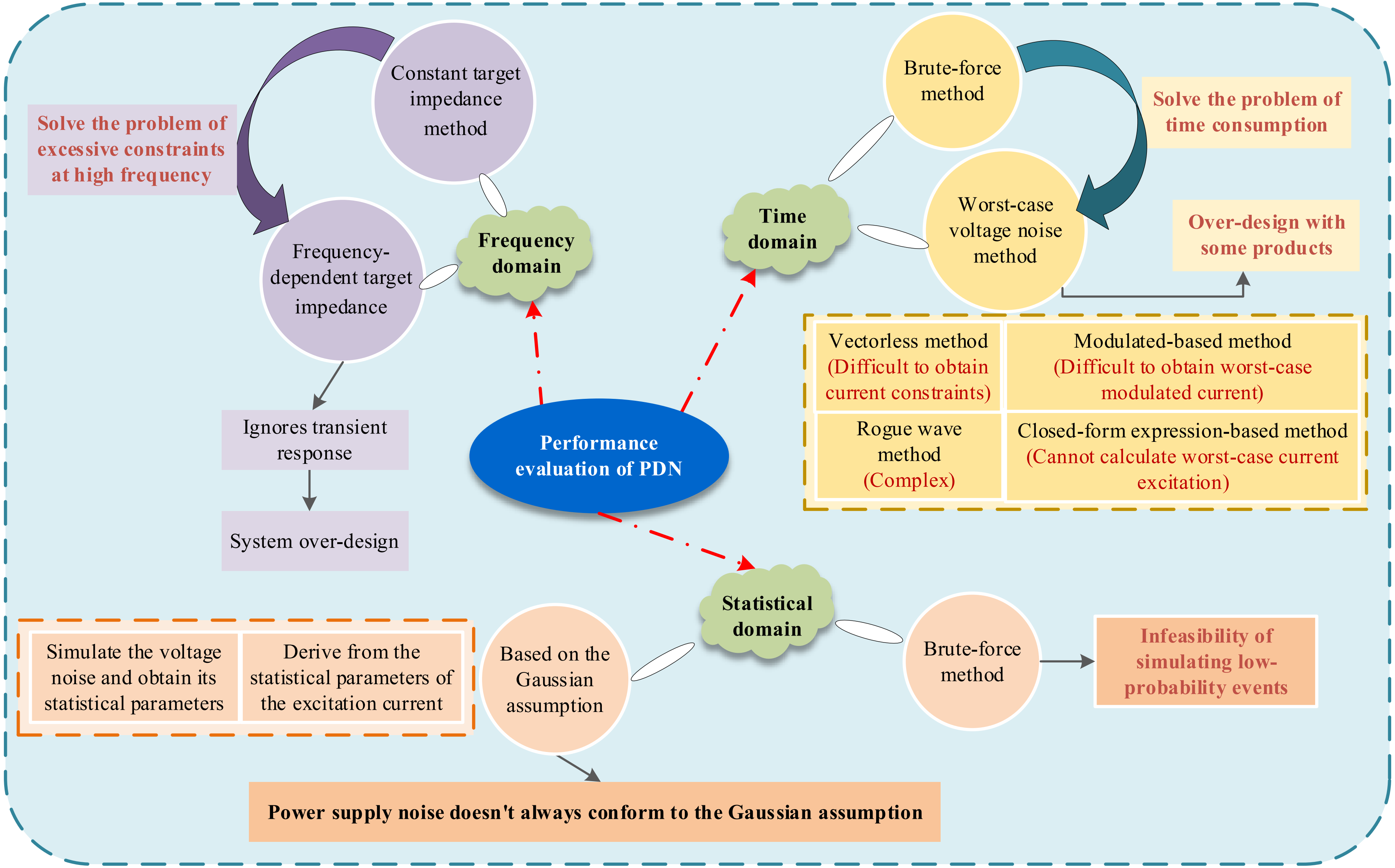
More design ingenuity is required!

1. PI Challenges in High-Power Computing Scenarios

The performance evaluation of PDN is an important part of its design optimization process.

Existing methods:

- ☐ Frequency domain
- ☐ Time domain
- ☐ Statistical domain



Performance evaluation of PDN

Frequency domain

Constant target impedance method

Solve the problem of excessive constraints at high frequency

Frequency-dependent target impedance

Ignores transient response

System over-design

Time domain

Brute-force method

Solve the problem of time consumption

Worst-case voltage noise method

Over-design with some products

Vectorless method (Difficult to obtain current constraints)	Modulated-based method (Difficult to obtain worst-case modulated current)
Rogue wave method (Complex)	Closed-form expression-based method (Cannot calculate worst-case current excitation)

Statistical domain

Brute-force method

Infeasibility of simulating low-probability events

Based on the Gaussian assumption

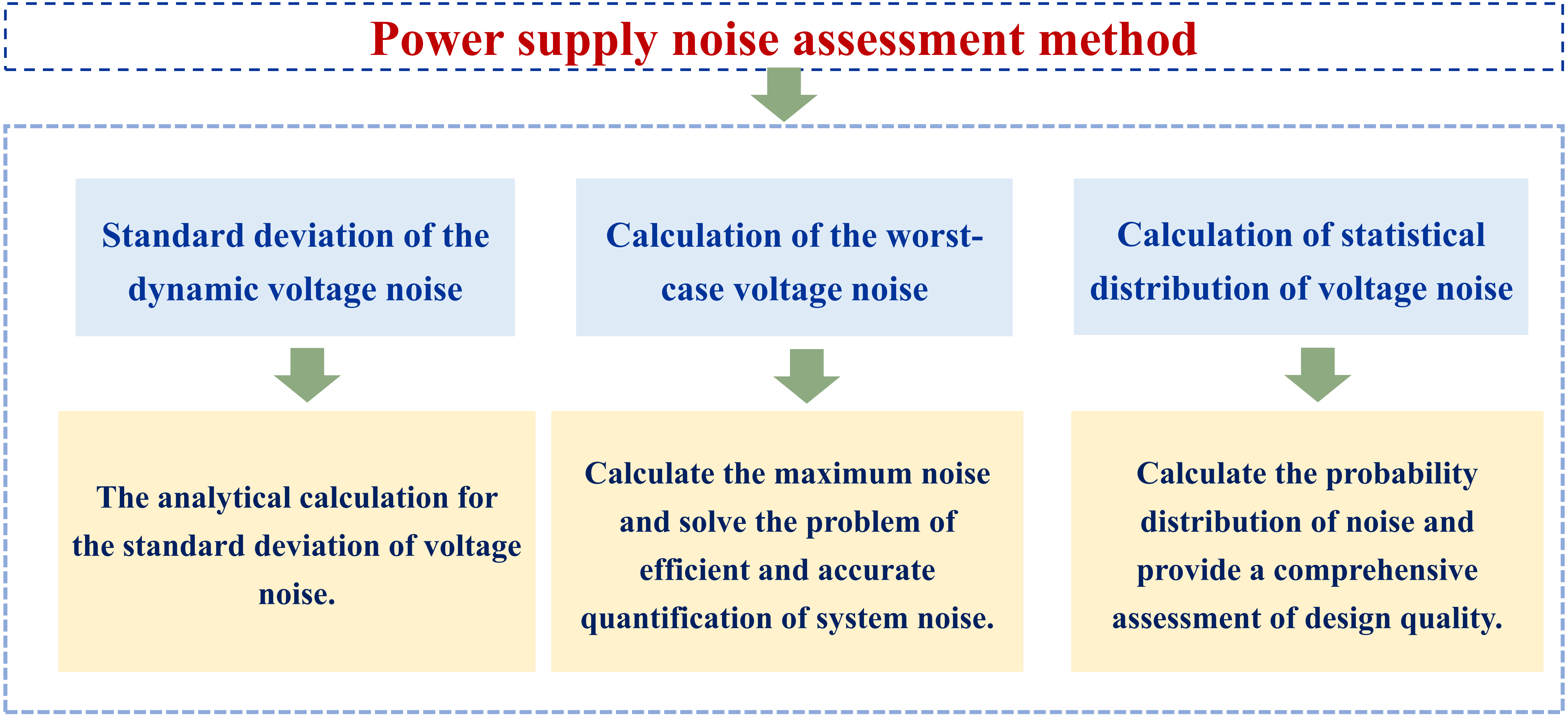
Simulate the voltage noise and obtain its statistical parameters	Derive from the statistical parameters of the excitation current

Power supply noise doesn't always conform to the Gaussian assumption

Outline

1. **PI Challenges in High-Power Computing Scenarios**
2. **Efficient time-domain noise analysis method**
    - **Analytical calculation for the standard deviation of voltage noise**
    - **The method of calculating of the worst-case voltage noise**
    - **The method of calculating the statistical distribution of voltage noise**

Power supply noise assessment method



Power supply noise assessment method

Standard deviation of the dynamic voltage noise

The analytical calculation for the standard deviation of voltage noise.

Calculation of the worst-case voltage noise

Calculate the maximum noise and solve the problem of efficient and accurate quantification of system noise.

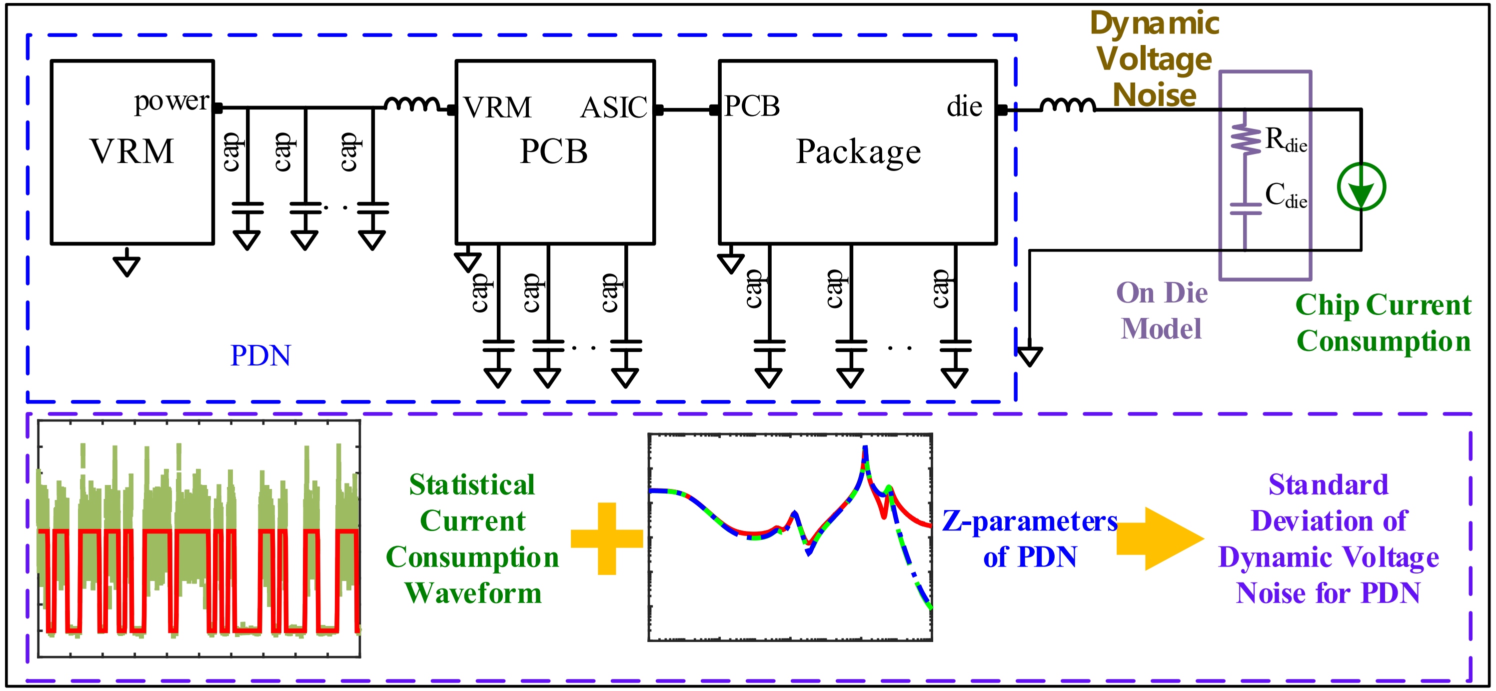
Calculation of statistical distribution of voltage noise

Calculate the probability distribution of noise and provide a comprehensive assessment of design quality.

1. The method of analytical calculation for the standard deviation of voltage noise

Proposed Method

Current acting upon the PDN impedance will cause voltage Noise



$$I \times Z = U$$

In **frequency** and **power spectral** domain, **current** multiplied by **impedance** equals to **voltage**.

Parseval's theorem

Obtain the standard deviation of the dynamic voltage noise.

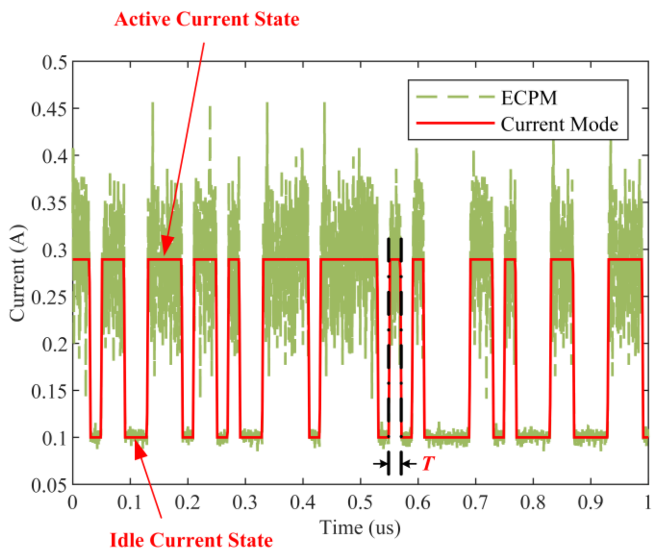
A Method for Calculating the Standard Deviation of Dynamic Voltage Noise by PSD (power spectral density) and Z-parameter.

Proposed Method

Calculation of the Power Spectral Density (PSD)

Plight

- ➢ **Current consumption behavior exhibits randomness.**
- ➢ **Current consumption behavior subject to logical constraints.**

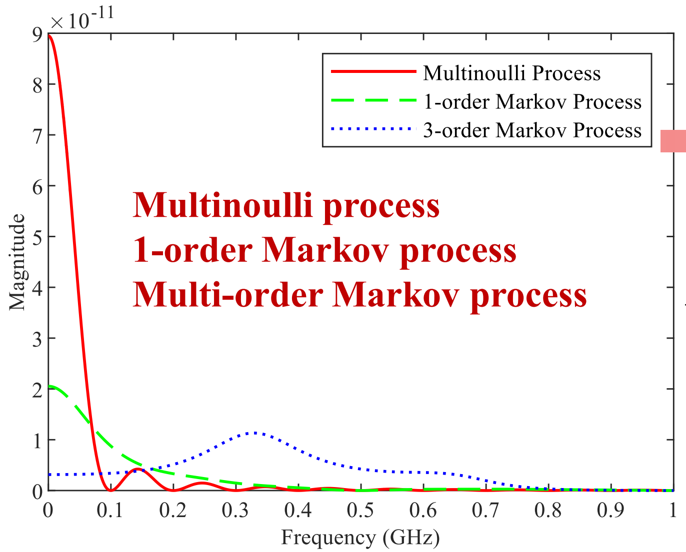


Current Consumption model

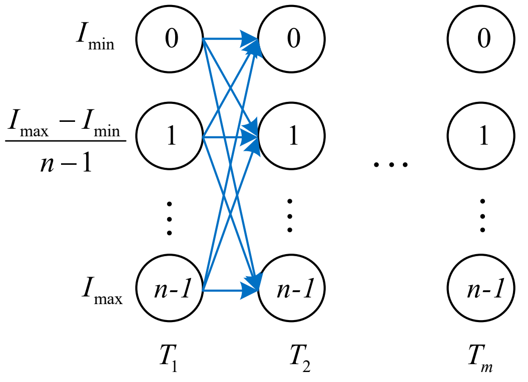
Tools for describing **randomness**

Auto-correlation

Wiener-Khinchi



The amplitude of current consumption in each cycle is a random variable.



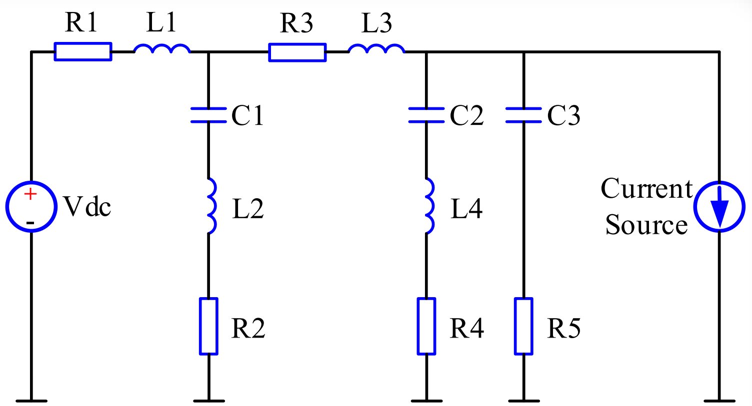
$$\mathbf{T}_1 = \begin{bmatrix} p_{11} & \cdots & p_{1I} & \cdots & p_{1M} \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ p_{K1} & \cdots & p_{KI} & \cdots & p_{KM} \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ p_{M1} & \cdots & p_{MI} & \cdots & p_{MM} \end{bmatrix}$$

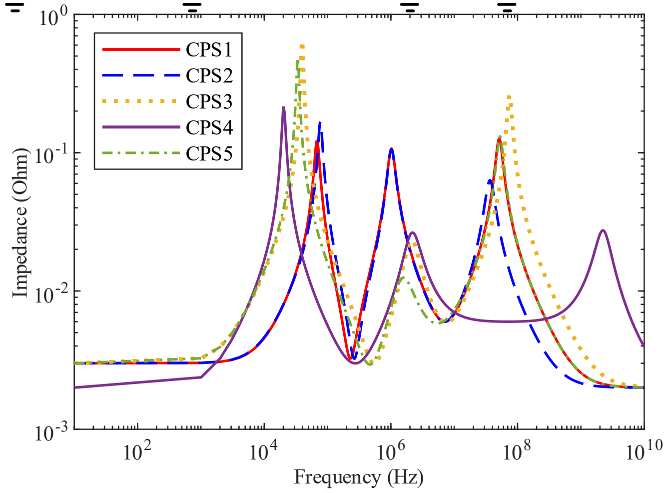
$$\begin{bmatrix} \mathbf{S}_1 \\ \mathbf{P} \end{bmatrix} = \begin{bmatrix} S_1 & \cdots & S_I & \cdots & S_M \\ p_1 & \cdots & p_I & \cdots & p_M \end{bmatrix}$$

Proposed method can calculate the PSD for various current consumption

Results

Result（Single Chip）



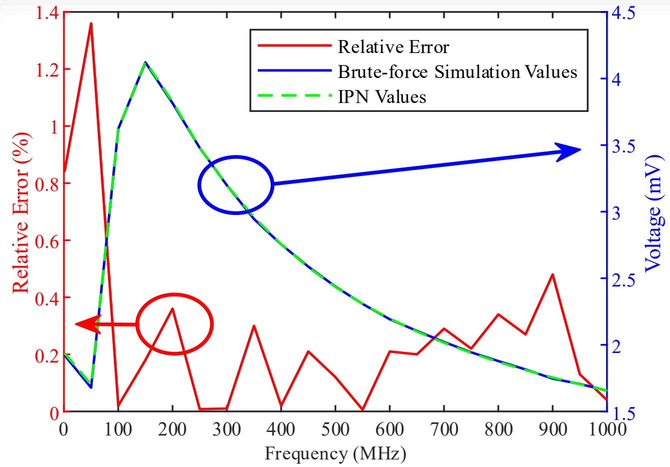


Only Modify the R, L, C

Comparison of the standard deviation of the dynamic voltage noise

CPS	1	2	3	4	5
Methods	Results（mV）				
The proposed method	3.25	1.69	6.43	0.67	3.30
Transient simulation	3.25	1.69	6.45	0.67	3.30

The results of the proposed method is accurate

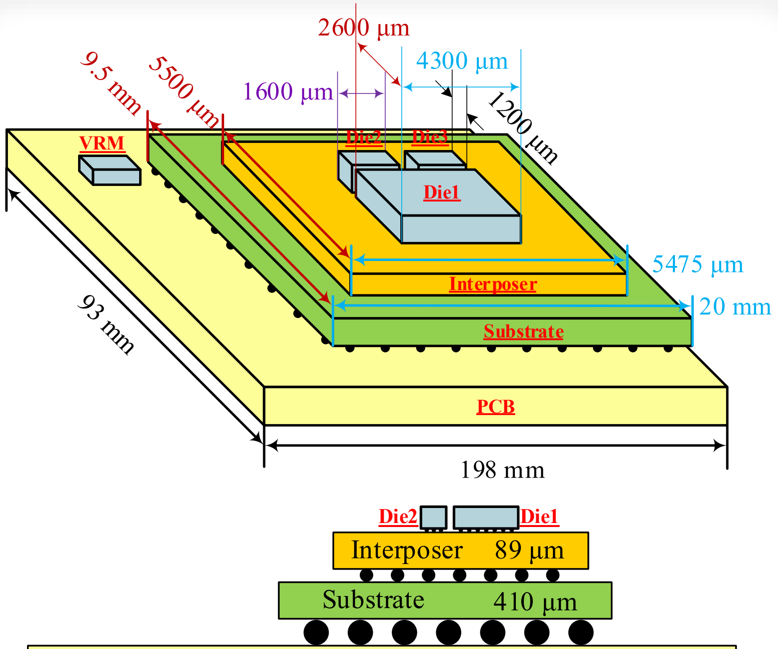


Verify robustness

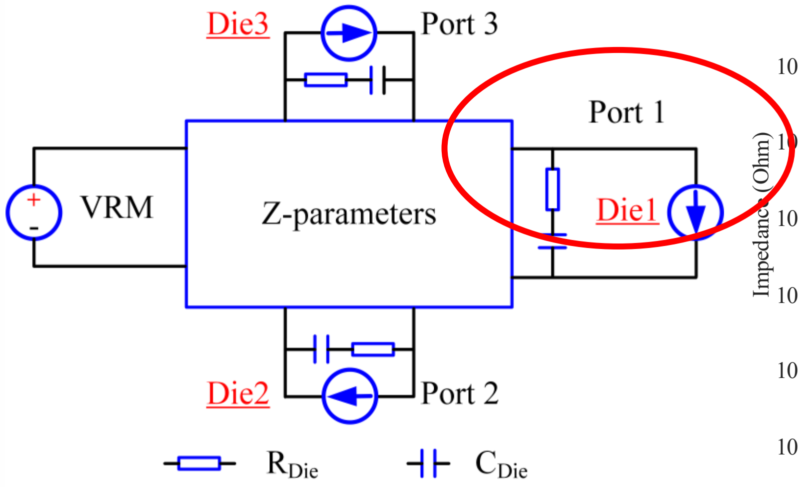
- **Fit well !**
- **Relative Error less than 2 %**
- **Time consumed in 1 second.**

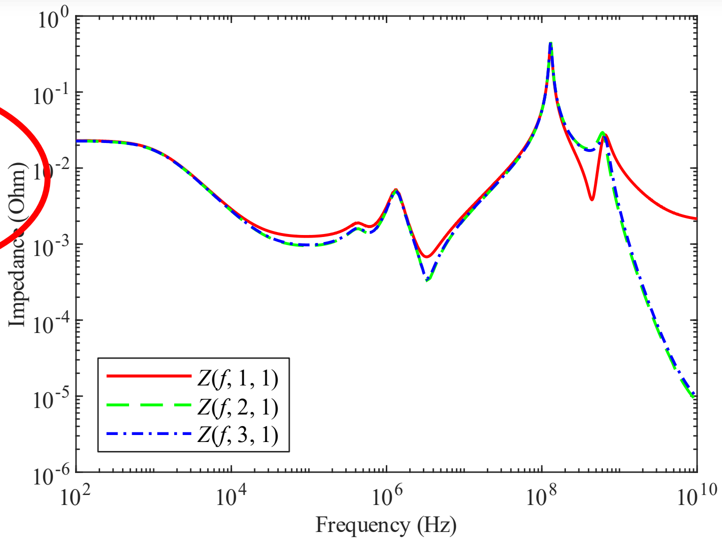
Results

Result（Multiple Chips）



Top	35 µm	Copper
Dielectric	200 µm	FR4
VCC	17 µm	Copper
Dielectric	1200 µm	FR4
GND	17 µm	Copper
Dielectric	200 µm	FR4
Bottom	35 µm	Copper



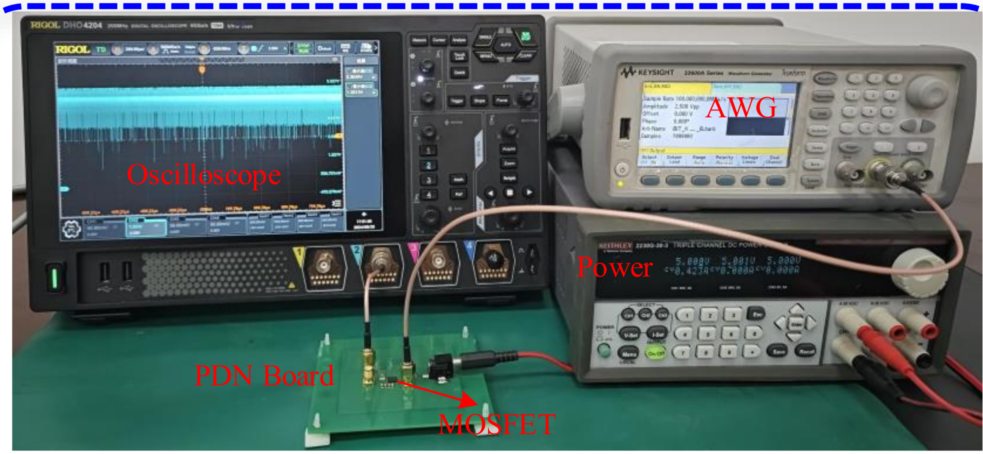


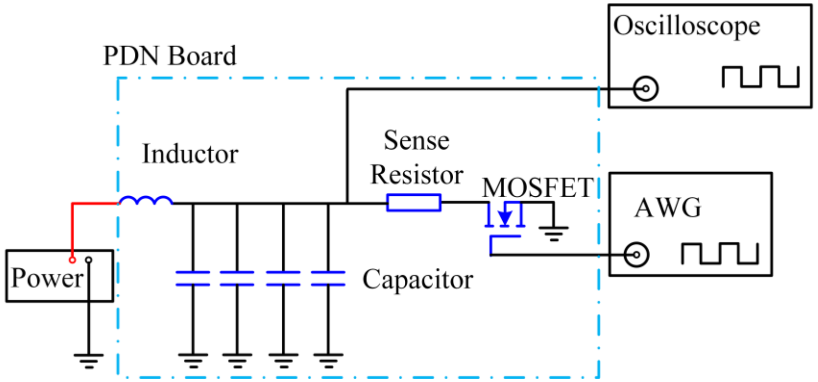
Calculate the voltage noise at Port 1

Random Process	Proposed Method (mV)	Transient Simulation (mV)	Relative Error (%)
Multinoulli Process	7.148	7.120	0.394
One-Order Markov Process	8.732	8.702	0.339
Two-Order Markov Process	9.859	9.840	0.198
Different Random Process for each Chip	8.196	8.238	0.517

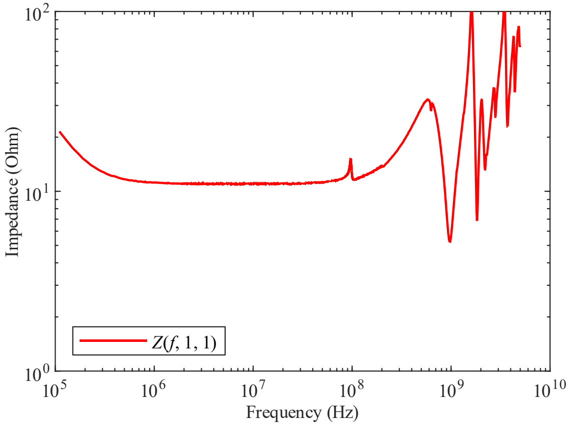
Results

Result（Measurement）

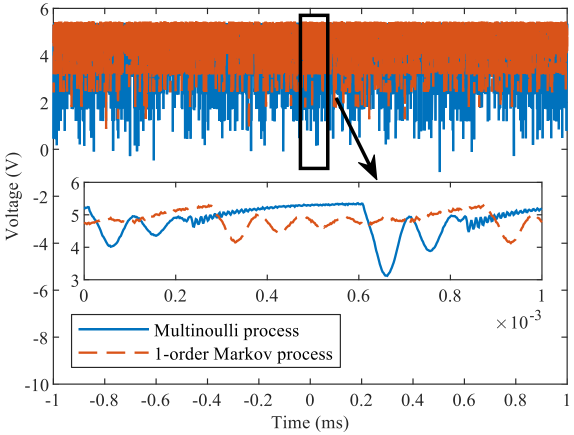




Topology of the Measurement Platform



Measured Impedance Curve



Measured Voltage Noise

Accurate !

Random Process	Proposed Method (mV)	Measurement (mV)	Relative Error(%)
Multinoulli Process	0.5739	0.5456	4.92 %
One-Order Markov Process	0.3999	0.3857	3.54 %
Three-Order Markov Process	0.4002	0.4167	4.11 %

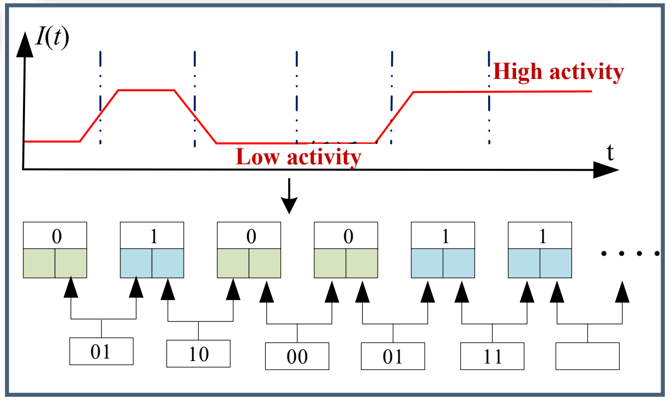
2. The method of calculating of the worst-case voltage noise

Power supply noise assessment method

01. Calculation of the Worst-Case Voltage Noise Based on Ramp Current

Load Current Modeling

Encode the current state



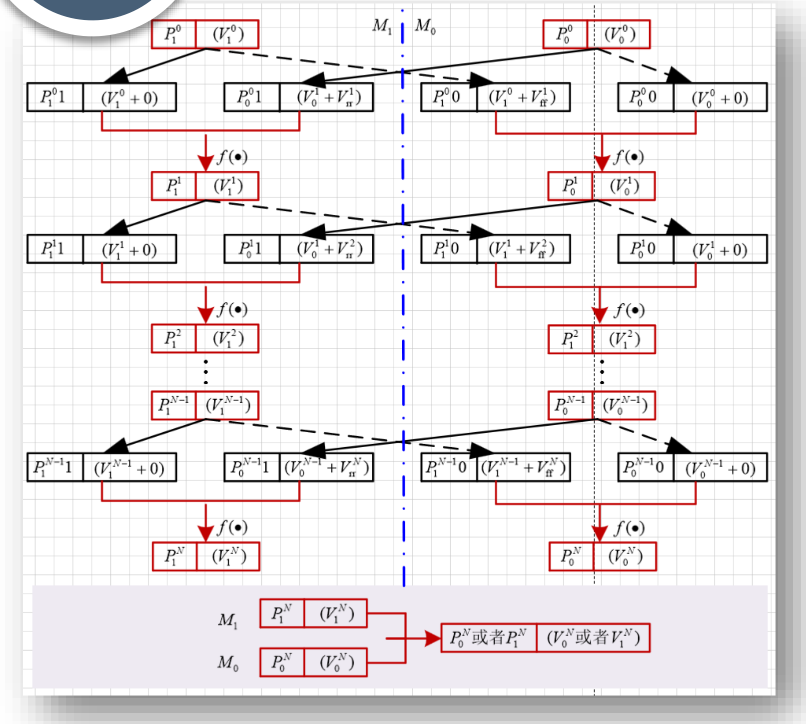
- **“01”: The ramp current from low to high;**
- **“10”: The ramp current from high to low;**
- **“00”: constant low-activity current;**
- **“11”: constant high-activity current.**

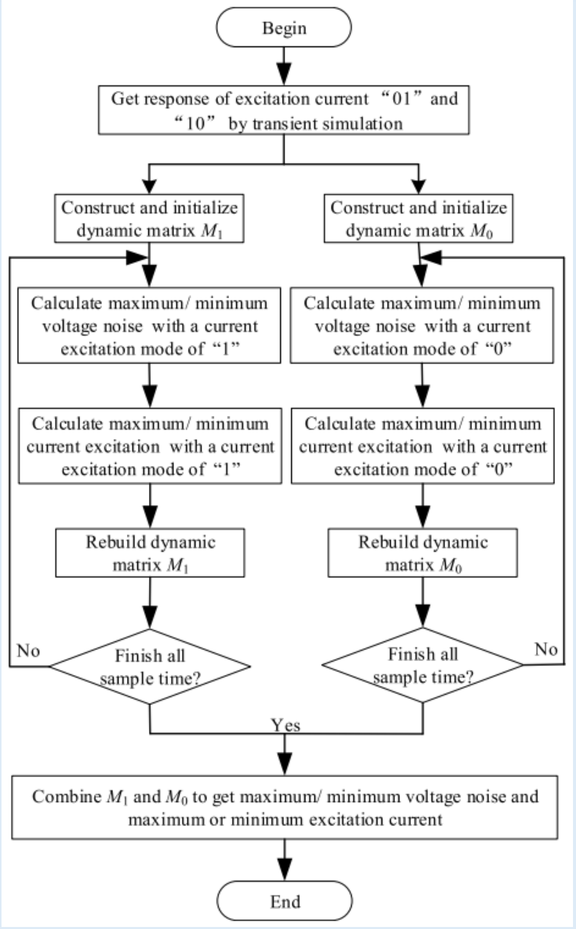
The ideal current of “01” and “10”

$$I_{\mathrm{r}}(t)=\begin{cases}\dfrac{I_{\max}}{2}, & t>0\\ 0, & t\le 0\end{cases}\qquad I_{\mathrm{f}}(t)=\begin{cases}0, & t>0\\ \dfrac{I_{\max}}{2}, & t\le 0\end{cases}$$

Calculate the Voltage Noise

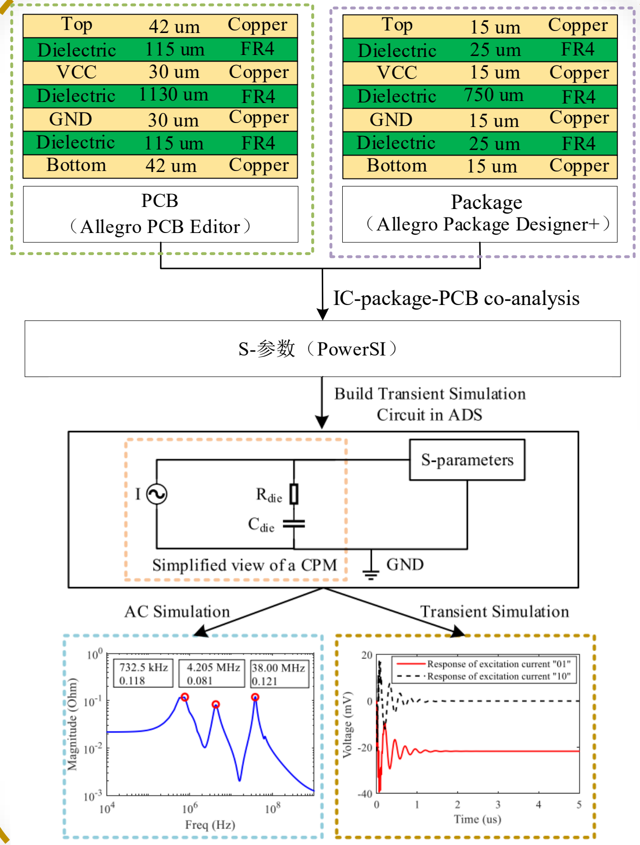
- **Calculate the worst-case voltage noise and the worst-case current excitation**





01. Calculation of the Worst-Case Voltage Noise Based on Ramp Current

Comparison With the Modulate-Based Method



Top	42 um	Copper
Dielectric	115 um	FR4
VCC	30 um	Copper
Dielectric	1130 um	FR4
GND	30 um	Copper
Dielectric	115 um	FR4
Bottom	42 um	Copper

PCB
（Allegro PCB Editor）

Top	15 um	Copper
Dielectric	25 um	FR4
VCC	15 um	Copper
Dielectric	750 um	FR4
GND	15 um	Copper
Dielectric	25 um	FR4
Bottom	15 um	Copper

Package
（Allegro Package Designer+）

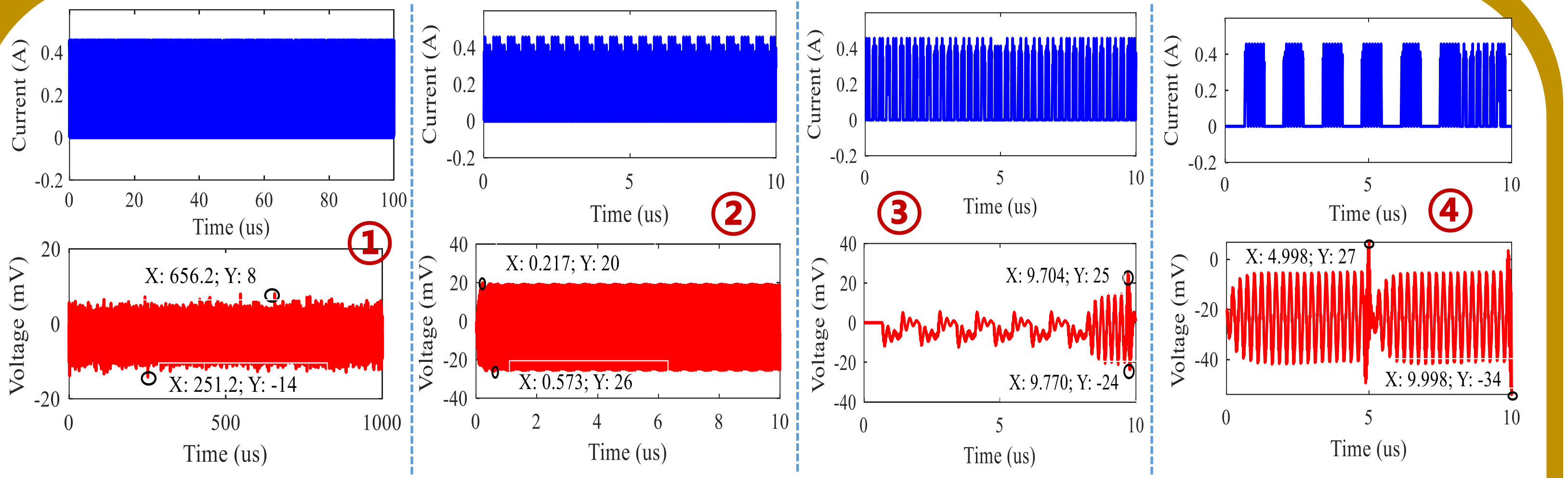
IC-package-PCB co-analysis

S-参数（PowerSI）

Build Transient Simulation Circuit in ADS

AC Simulation

Transient Simulation



	最坏电源噪声	误差	耗时
①：PRBS current modulated by clock gating current sequence of 38.0 MHz	50 mV	--	10.3 s
②：PWL current modulated by clock gating current sequence of 38.0 MHz	46 mV	-8%	10.2 s
③：PWL current modulated by three gating current sequences	49 mV	-2%	10.9 s
④：Proposed method	61 mV	22%	12.3 s

The proposed method obtains more accurate results.

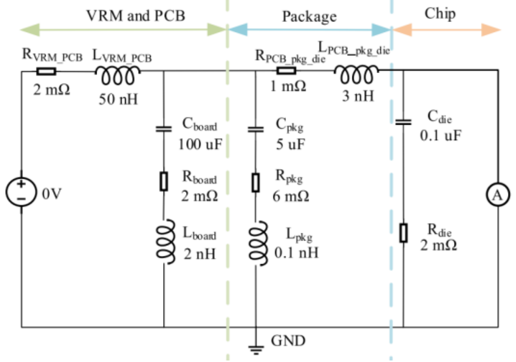
Power supply noise assessment method

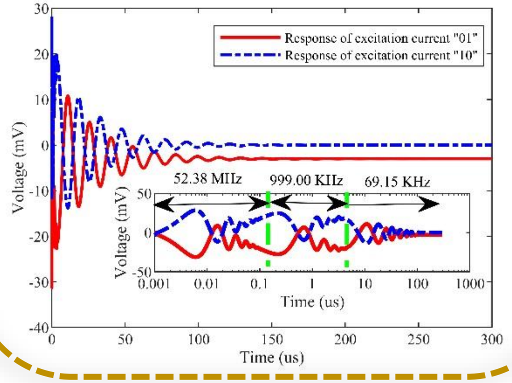
01. Calculation of the Worst-Case Voltage Noise Based on Ramp Current

Compared With the Rogue Wave Method

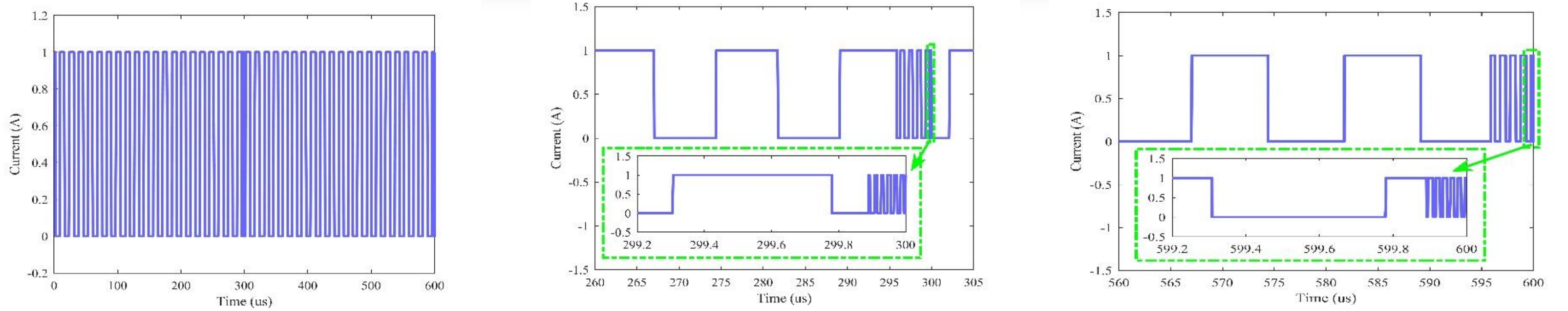
The proposed method obtains more accurate results.

A 3rd-order PDN circuit model used in comparison

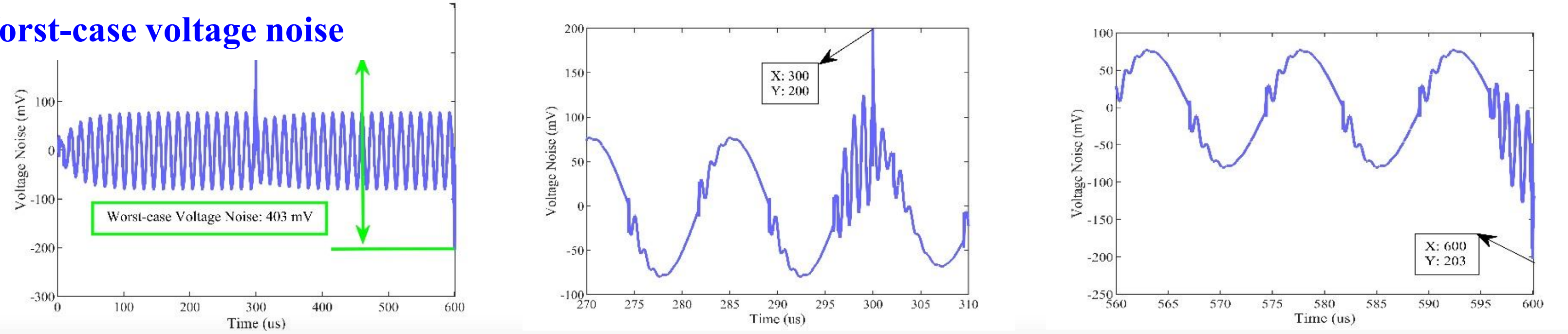




Worst-case current excitation



Worst-case voltage noise

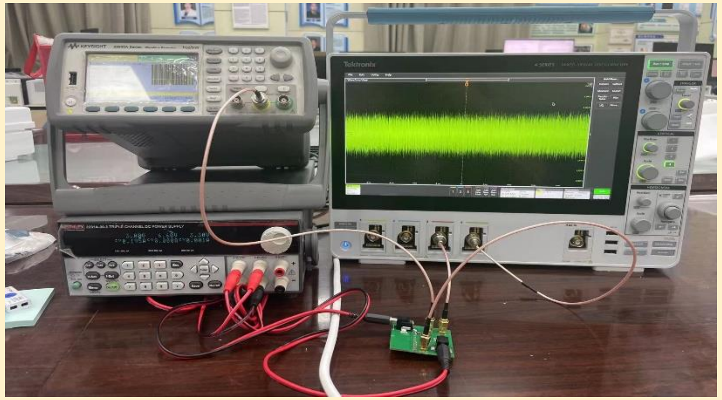


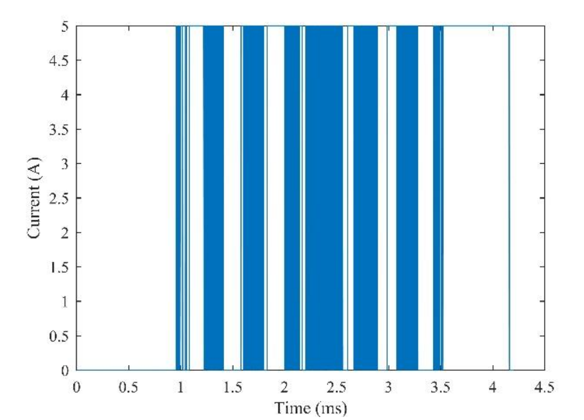
	Proposed	Simulated result based on proposed worst-case current excitation	Rouge wave
Voltage noise（mV）	403	403	375

Power supply noise assessment method

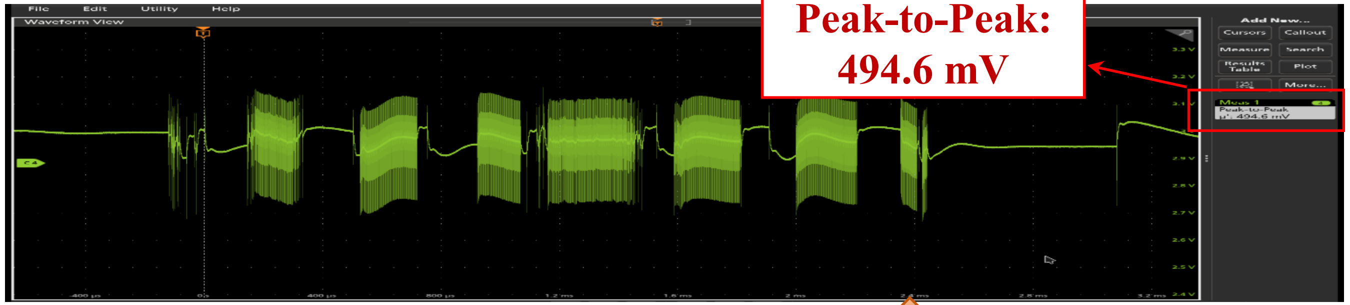
01. Calculation of the Worst-Case Voltage Noise Based on Ramp Current

Measurement





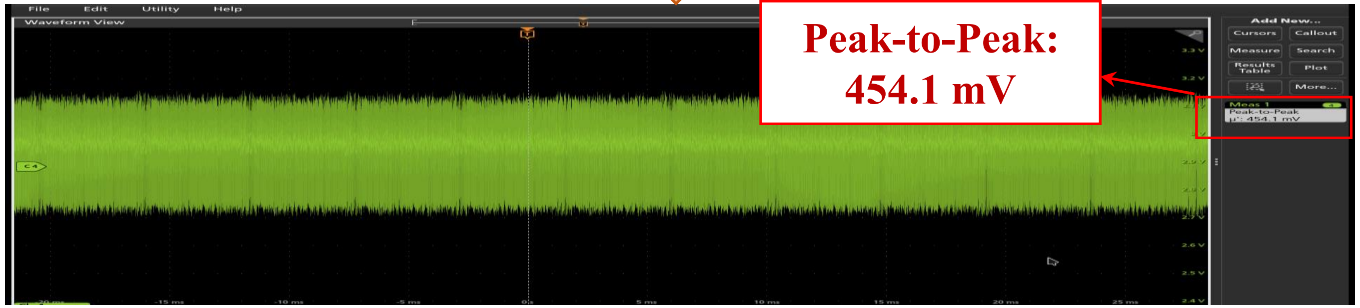
Worst-case current excitation calculated by responses of the ramp currents



Peak-to-Peak: 494.6 mV

Voltage noise for worst-case excitation

Voltage noise for arbitrary excitation



Peak-to-Peak: 454.1 mV

The proposed method is more efficient.

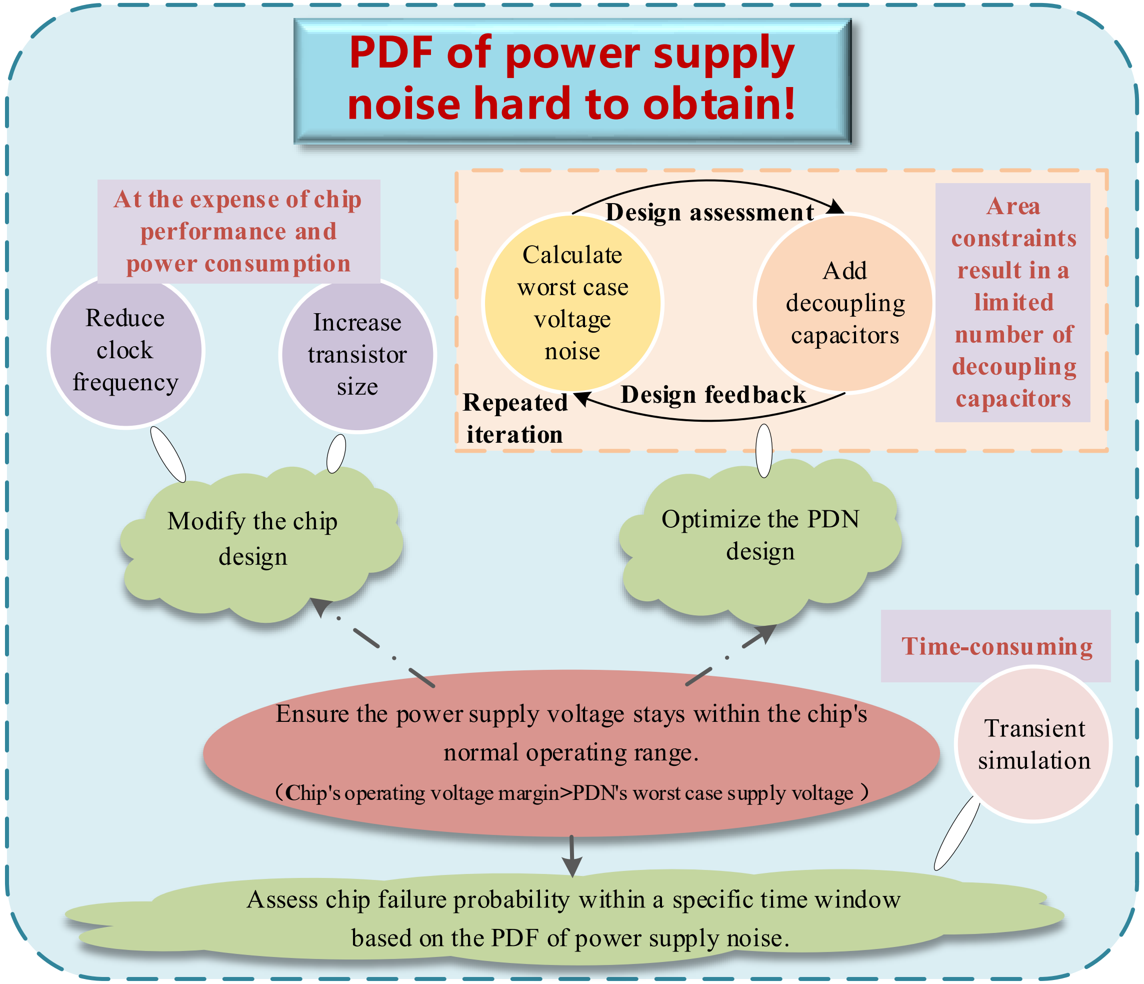
Power supply noise assessment method

3. The method of calculating the statistical distribution of voltage noise

Power supply noise assessment method

02. Calculation of Statistical Distribution of Power Supply Noise

Voltage noise statistical distribution analysis based on multiple pulse currents



PDF of power supply noise hard to obtain!

At the expense of chip performance and power consumption

Reduce clock frequency

Increase transistor size

Design assessment

Calculate worst case voltage noise

Add decoupling capacitors

Design feedback

Repeated iteration

Area constraints result in a limited number of decoupling capacitors

Modify the chip design

Optimize the PDN design

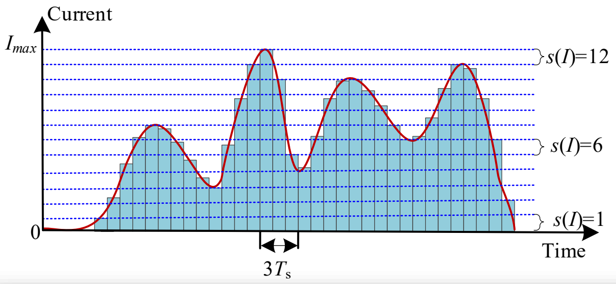
Time-consuming

Ensure the power supply voltage stays within the chip's normal operating range.
（Chip's operating voltage margin>PDN's worst case supply voltage ）

Transient simulation

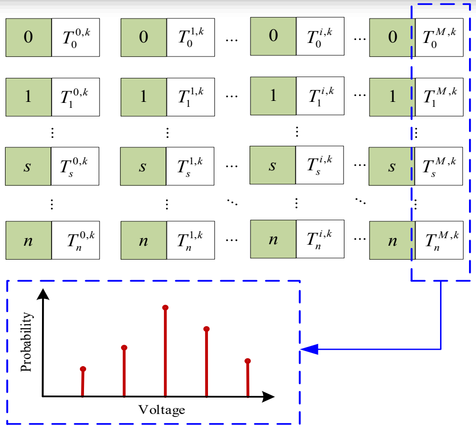
Assess chip failure probability within a specific time window based on the PDF of power supply noise.

Current feature extraction & current encoding



$$s(I)=\begin{cases}0, & I=0\\ 1, & I\in(0,\frac{I_{\max}}{n}\cdot 1]\\ \vdots & \vdots\\ i, & I\in(\frac{I_{\max}}{n}\cdot(i-1),\frac{I_{\max}}{n}\cdot i]\\ \vdots & \vdots\\ n, & I\in(\frac{I_{\max}}{n}\cdot(n-1),\frac{I_{\max}}{n}\cdot n]\end{cases}$$

Calculate the Statistical Distribution of Noise



The voltage and corresponding probability in the sth matrix at the kth sampling point in the ith period:

$$V_s^{i,k}=\left[V_0^{i-1,k}+v_s^{i,k},V_1^{i-1,k}+v_s^{i,k},\cdots,V_n^{i-1,k}+v_s^{i,k}\right]$$

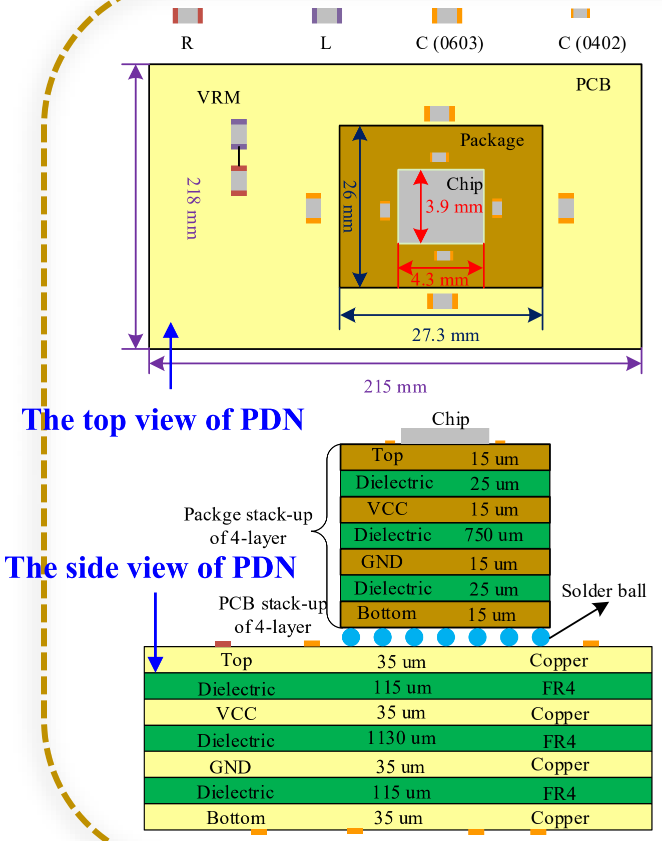
$$P_s^{i,k}=\left[P_0^{i-1,k}\cdot\frac{1}{n+1},P_1^{i-1,k}\cdot\frac{1}{n+1},\cdots,P_n^{i-1,k}\cdot\frac{1}{n+1}\right]$$

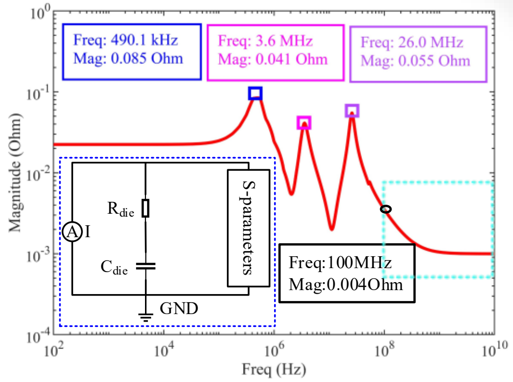
$$T_s^{i,k}=\begin{bmatrix}V_s^{i,k}\\ P_s^{i,k}\end{bmatrix}$$

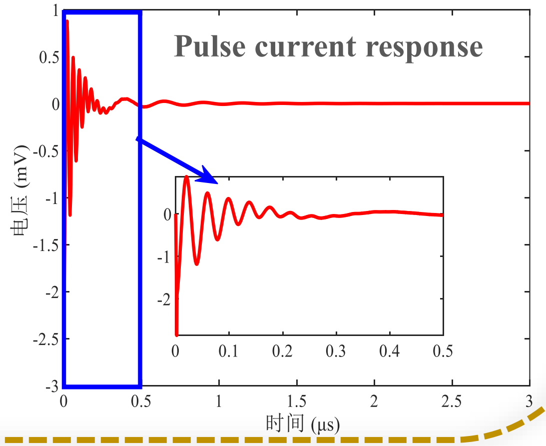
$$T^k=\begin{bmatrix}T_0^{M,k} & T_1^{M,k} & \cdots & T_n^{M,k}\end{bmatrix}=\begin{bmatrix}V_0^{M,k} & V_1^{M,k} & \cdots & V_n^{M,k}\\ P_0^{M,k} & P_1^{M,k} & \cdots & P_n^{M,k}\end{bmatrix}$$

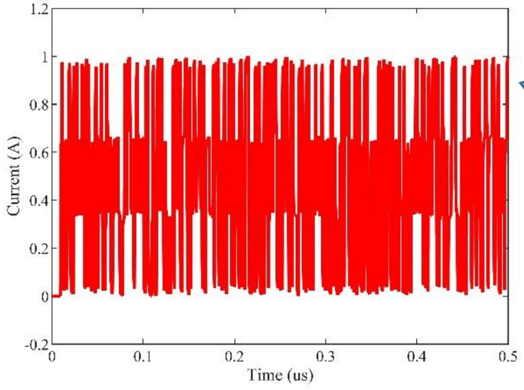
02. Calculation of Statistical Distribution of Power Supply Noise

Comparison of voltage noises obtained by the transient simulation and the proposed method



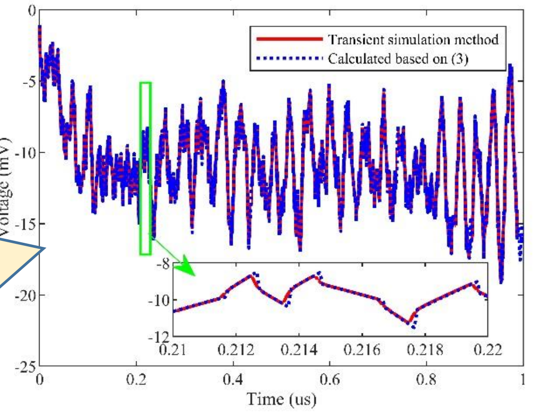






- Ip-p of the load is 1A
- Rise/fall time is 0.1 ns
- Pulse width is 1 ns
- 20 samples in one period

$$V(t)\big|_{t=t_0} = R^s(t_0) + \sum_{j=1}^{m}\left(\left(\frac{s'}{n}\right)\cdot R(t_0 - jT) - V_{steady}\right)$$

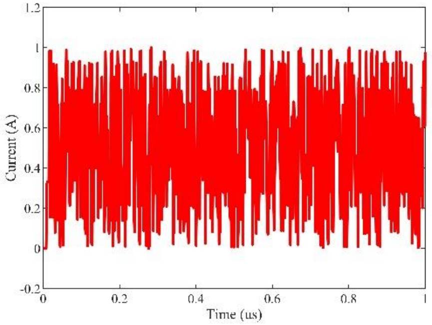


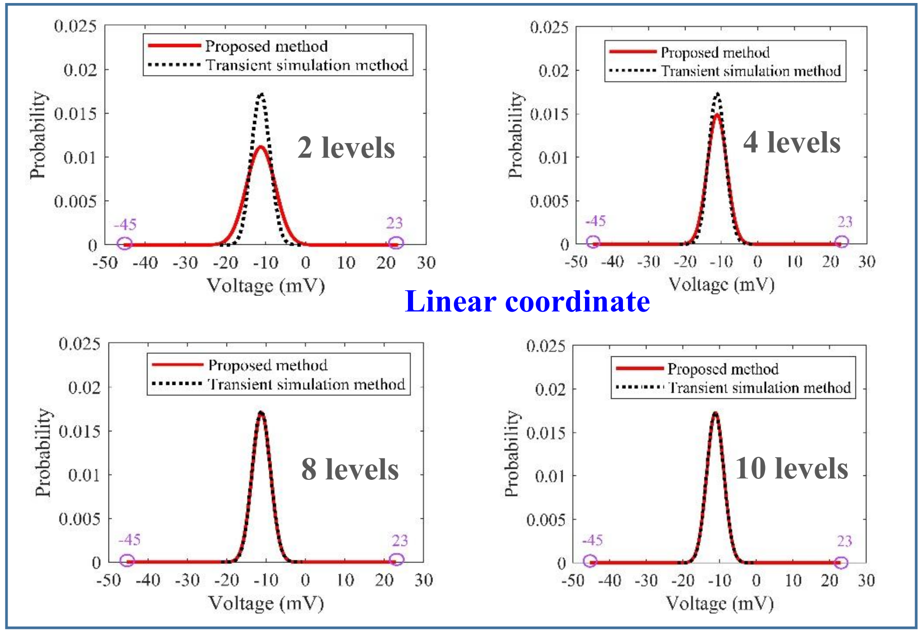
- 4 current levels
- transient simulation & proposed method
- The fit goodness for two curves is 0.9979

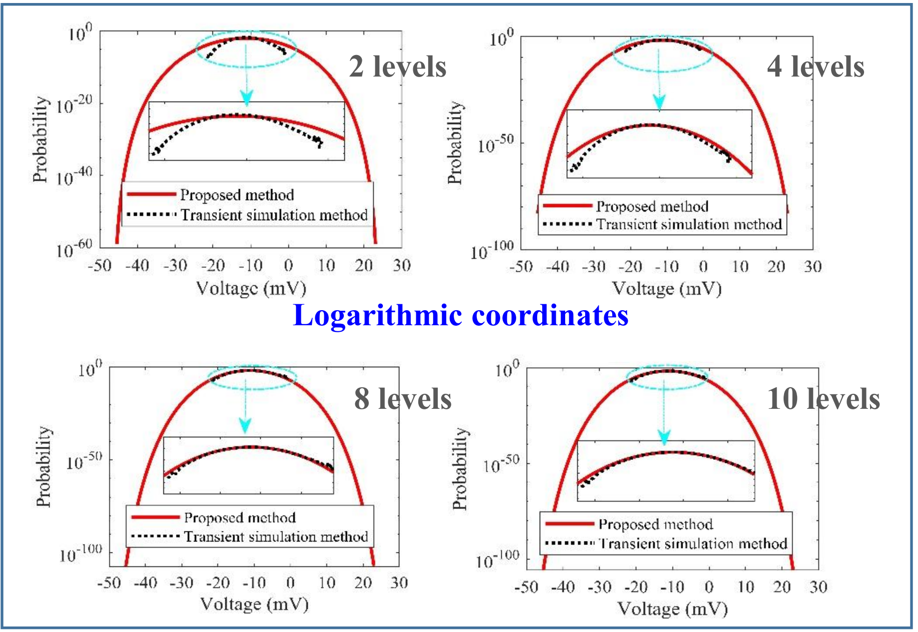
02. Calculation of Statistical Distribution of Power Supply Noise

Comparison of PDFs of noise obtained by the transient simulation and the proposed method

- **The amplitude of the load current was categorized into 2 levels, 4 levels, 8 levels, and 10 levels, respectively;**
- **Utilizing the proposed method in conjunction with current pulse responses of varying amplitudes to calculate the voltage noise PDF.**







	2 levels		4 levels		8 levels		10 levels	
	Mean (mV)	Standard deviation (mV)	Mean (mV)	Standard deviation (mV)	Mean (mV)	Standard deviation (mV)	Mean (mV)	Standard deviation (mV)
Transient simulation	-11.191	0.073	-11.191	0.073	-11.191	0.073	-11.191	0.073
Proposed method	-11.191	0.035	-11.191	0.084	-11.191	0.072	-11.191	0.073
Relative error (%)	0.000	52.055	0.000	15.068	0.000	1.370	0.000	0.00

Thanks