

Conquer MIPI C-PHY Simulation Challenge

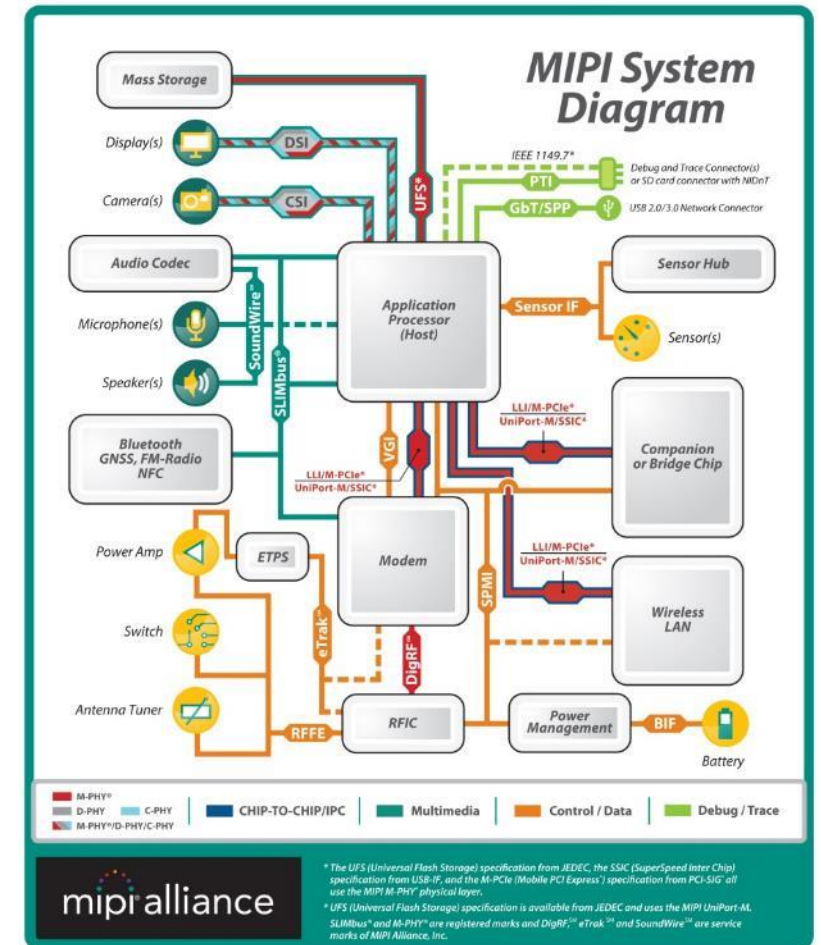
Xiuguo Jiang

Keysight EDA SE Manager

2025.11.07

Agenda

- MIPI and C-PHY Background
- C-PHY Simulation Challenge
- C-PHY Simulation Traditional Solution
- Innovative Simulation for C-PHY and Case Study
- Summary



Background

MIPI C-PHY leads Camera interface

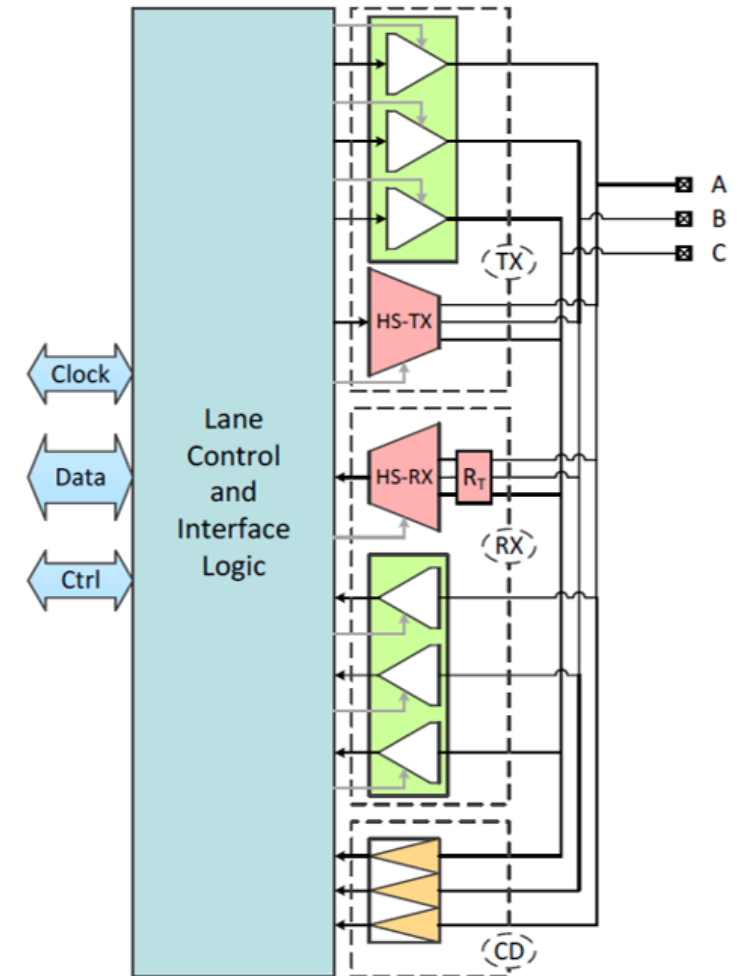
- More cameras have been integrated into mobile devices, including VR/AR headsets
- High-speed data transmission is essential for ADAS, autonomous vehicles, and in-vehicle infotainment systems
- Adopting more MIPI C-PHY reduces harness weight and enables the transmission of more high-speed data



Image source: tesla.com

MIPI C-PHY Introduction

- Lane consisting of 3 wires, A, B, C
- TXs and RXs: Bidirectional
- Contention detection (LP only)
- Two set's of TXs / RXs (HS & LP)
- LP-mode:
 - Large amplitude ($\sim 1V$), unterminated
 - Data format: "RZ"
 - Signaling: non-differential
- HS-mode:
 - Small amplitude ($\sim 200mV,pp$)
 - Termination 50 Ω - "star-type" (encircled)
 - Data format: 3-phase / 3-level
 - Signaling: 3 single ended wires forming a HS-lane,
 - Encoding: 16 bits to 7 symbols with 5 values (0,1,2,3,4) => coding gain 2.28



MIPI C-PHY Simulation Challenges

C-PHY sources need to model true silicon behaviors

However,

- The generic C-PHY model has limitations due to its linear behavior
- The simulation results show discrepancies from actual measurements
- Designers have begun to seek an accurate simulation method down to the silicon level.



“There are differences between simulations vs. real silicon measurements.”

“Designers want to simulate C-PHY with true silicon-level chip behaviors.
How can we provide this model?”

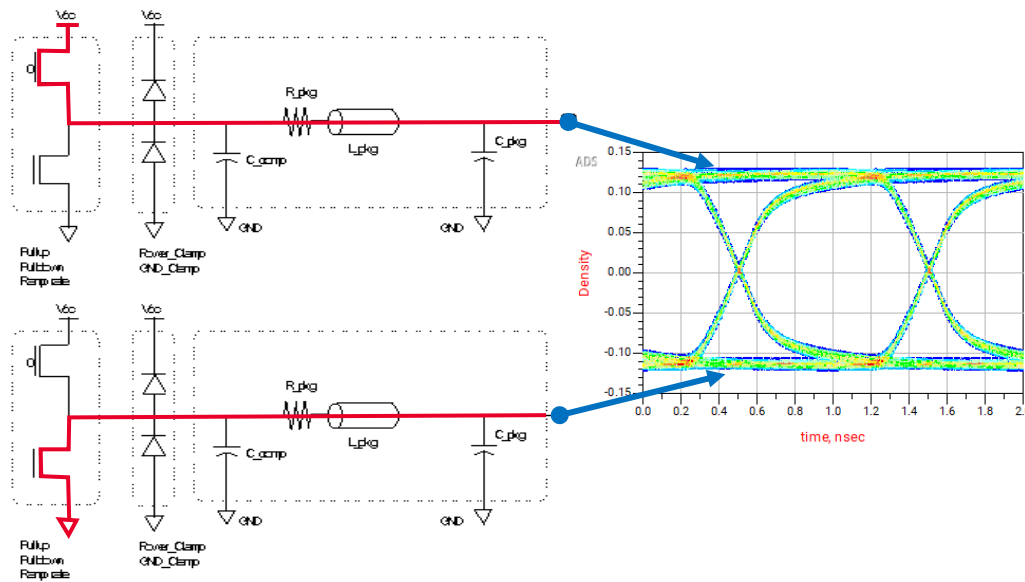


How to simulate MIPI C-PHY with true silicon level behaviors?

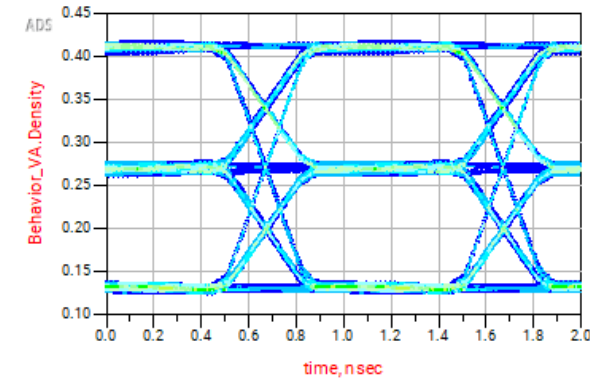
MIPI C-PHY Simulation Challenges I

Limitation with conventional IBIS models

- IBIS (Input/Output buffer information specification) model



The IBIS model is defined for two level transitions (Pull-up and Pull-down)

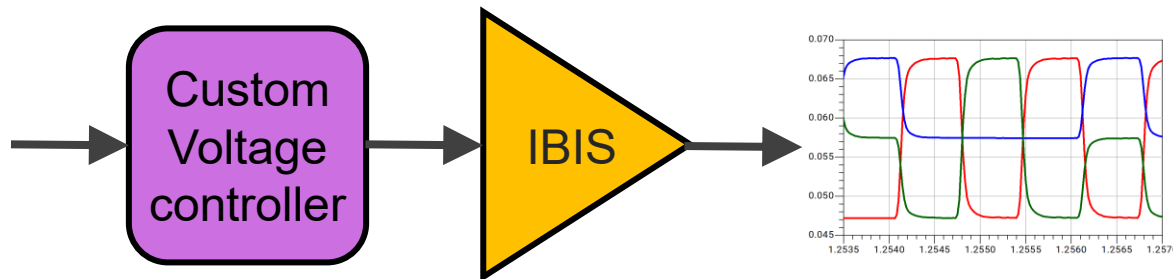


However, C-PHY uses PAM3-like signaling.

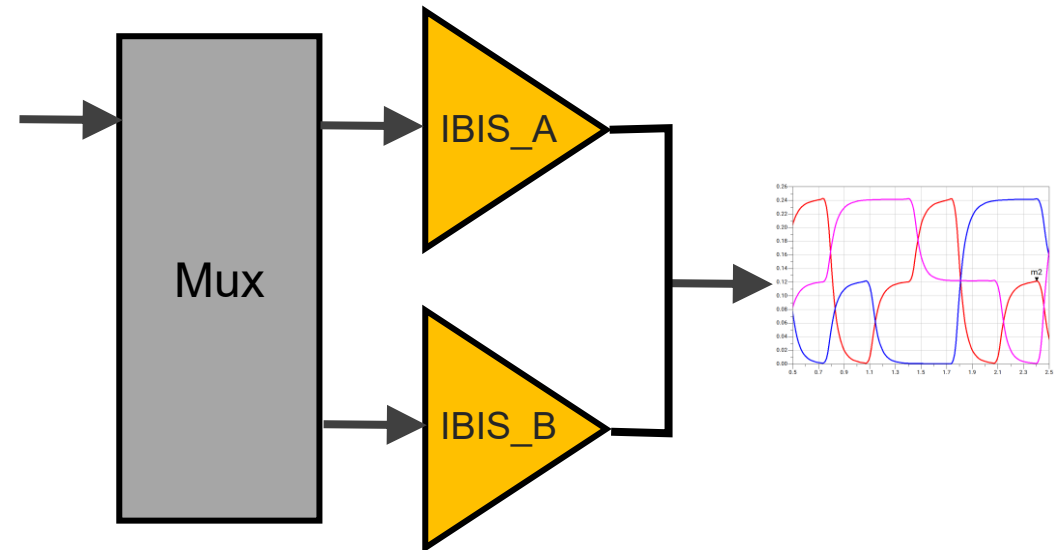
MIPI C-PHY Simulation Challenges II

Why conventional IBIS model can't deliver the right signaling?

- Modified IBIS model



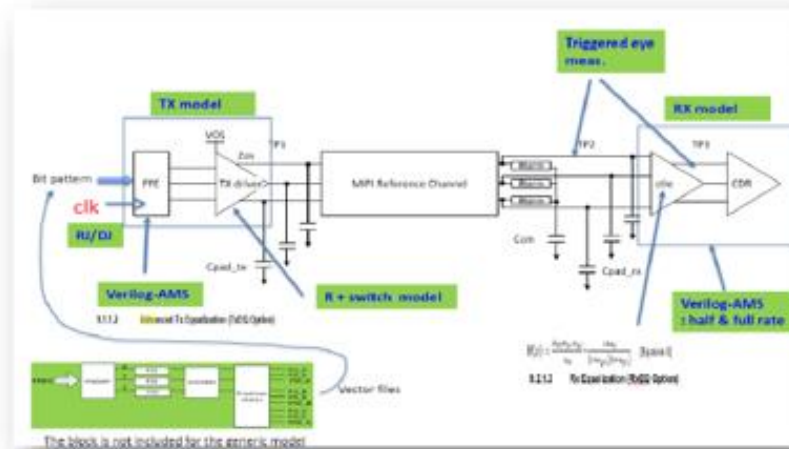
- 3 state level is not real chip behavior
- All rise/fall time has the same slew rate



- Mid-state level might be wrong due to impedance difference between IBIS files
- Low to High rise/fall time is not represented

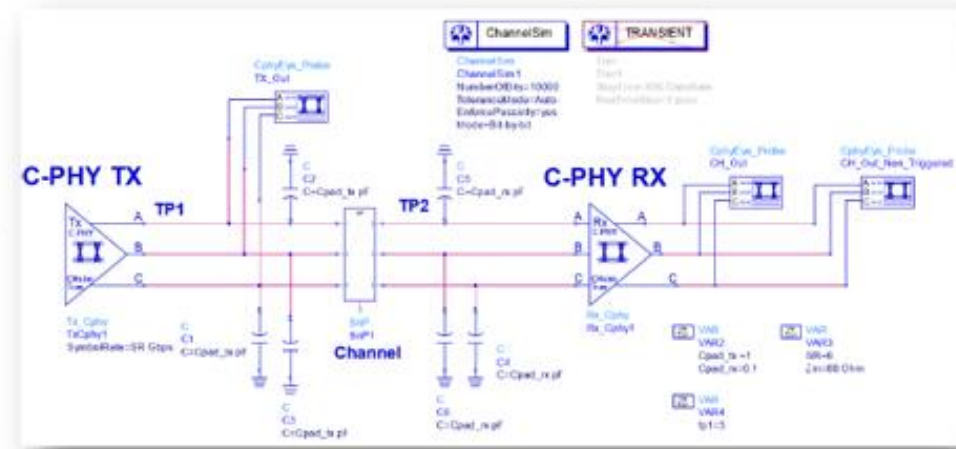
C-PHY Simulation Traditional Solution

- Special C-PHY Transmitter, Receiver and Trigger Eye-Probe
- Support Transient and Statistical simulation technology
- Support Tx/Rx equalization and RJ, PJ, DCD, and so on jitter model.



Note: Courtesy of Qualcomm

Today



EDA Tool

EDA Tool Challenges

Ensuring EDA Tool Compatibility

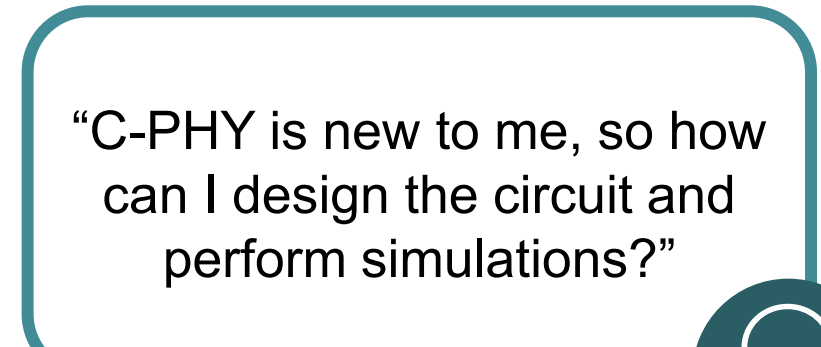
- High-speed data transmission is essential for ADAS, autonomous vehicles, and in-vehicle infotainment systems
- Adopting more MIPI C-PHY reduces harness weight and enables the transmission of more high-speed data

However,

- C-PHY is new to the automotive industry
- There is no clear direction on which tools to use.
- Existing simulation tools are commonly utilized.



“What criteria should be used to choose a MIPI C-PHY simulation tool?”



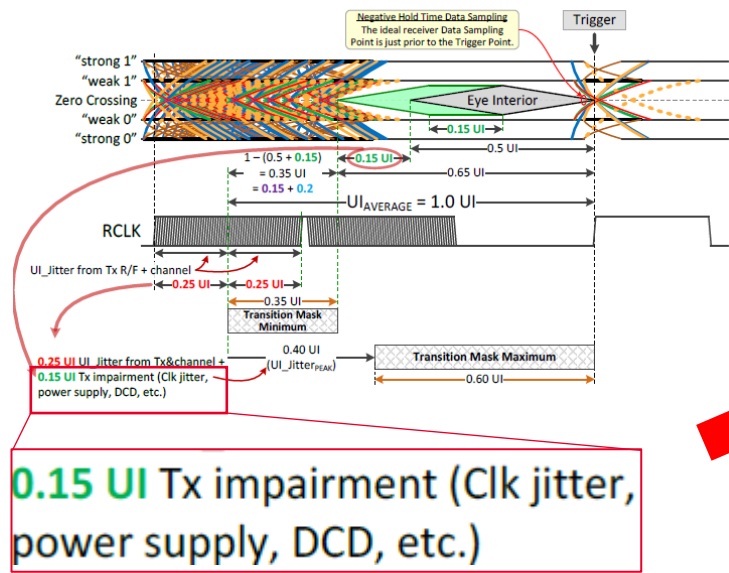
“C-PHY is new to me, so how can I design the circuit and perform simulations?”

How do I know my EDA tool complies with the C-PHY specification?

MIPI C-PHY Jitter Requirements

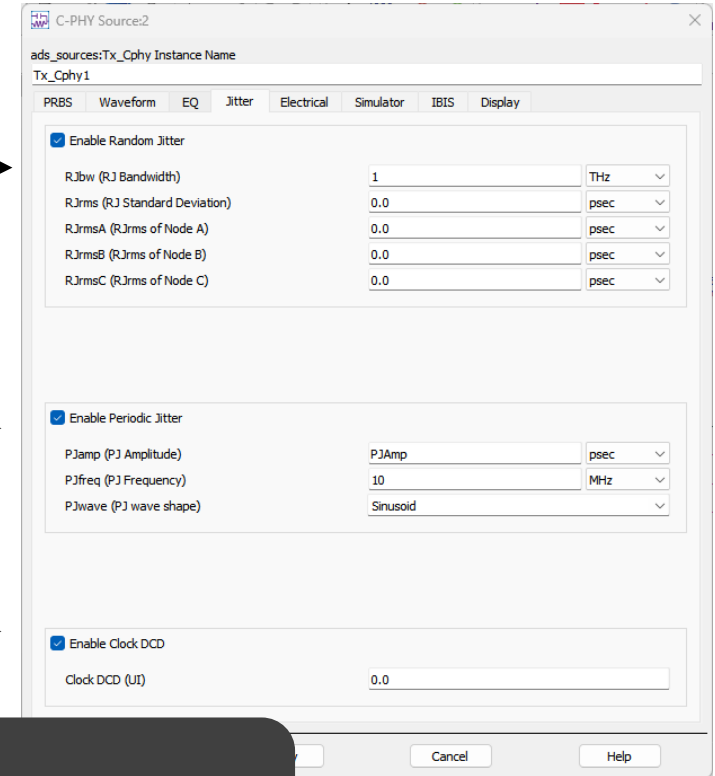
Ensure Accurate Jitter Simulation

MIPI C-PHY Jitter definition



Possible Tx jitter

- Power supply \rightarrow RJ
- Clk_Jitter \rightarrow Periodic
- DCD \rightarrow Clock DCD



C-PHY source must support Tx jitter, ClockDCD, RJ, PJ

Complexity of C-PHY Signals

Mapping and Encoding the data

0x7290 =
0001110001111010

16 bits
word

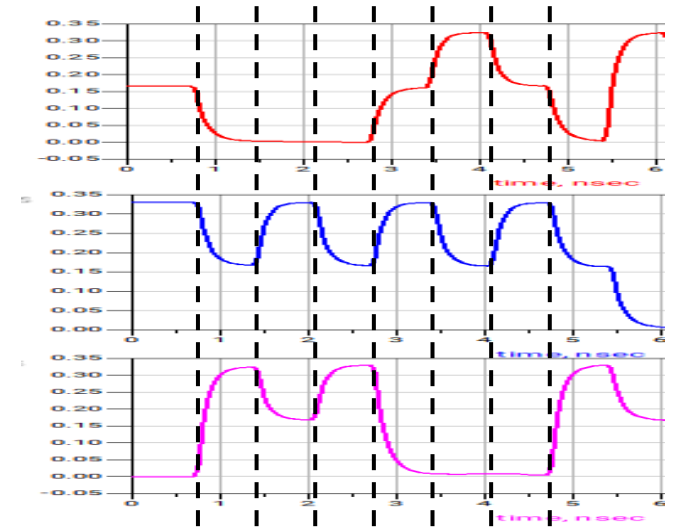
Symbols

- 010
- 010
- 011
- 001
- 000
- 011
- 001

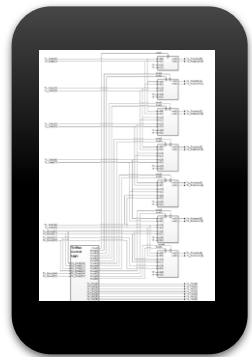
{1301322}

Wire state name

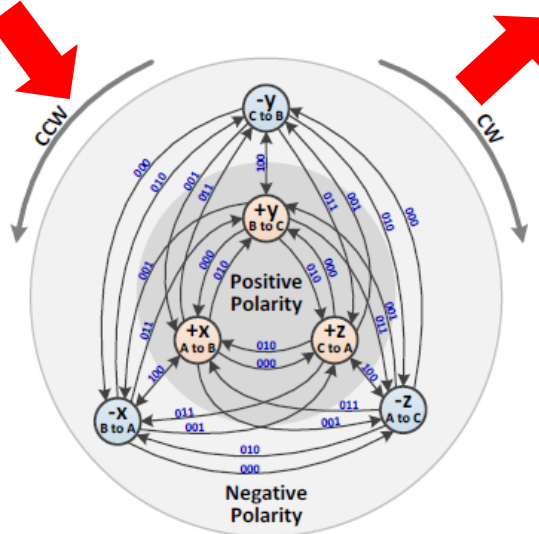
- +x
- +y
- +z
- x
- +z
- +y
- z
- +y



+y | +z | -x | +z | +y | -z | +y



Mapping



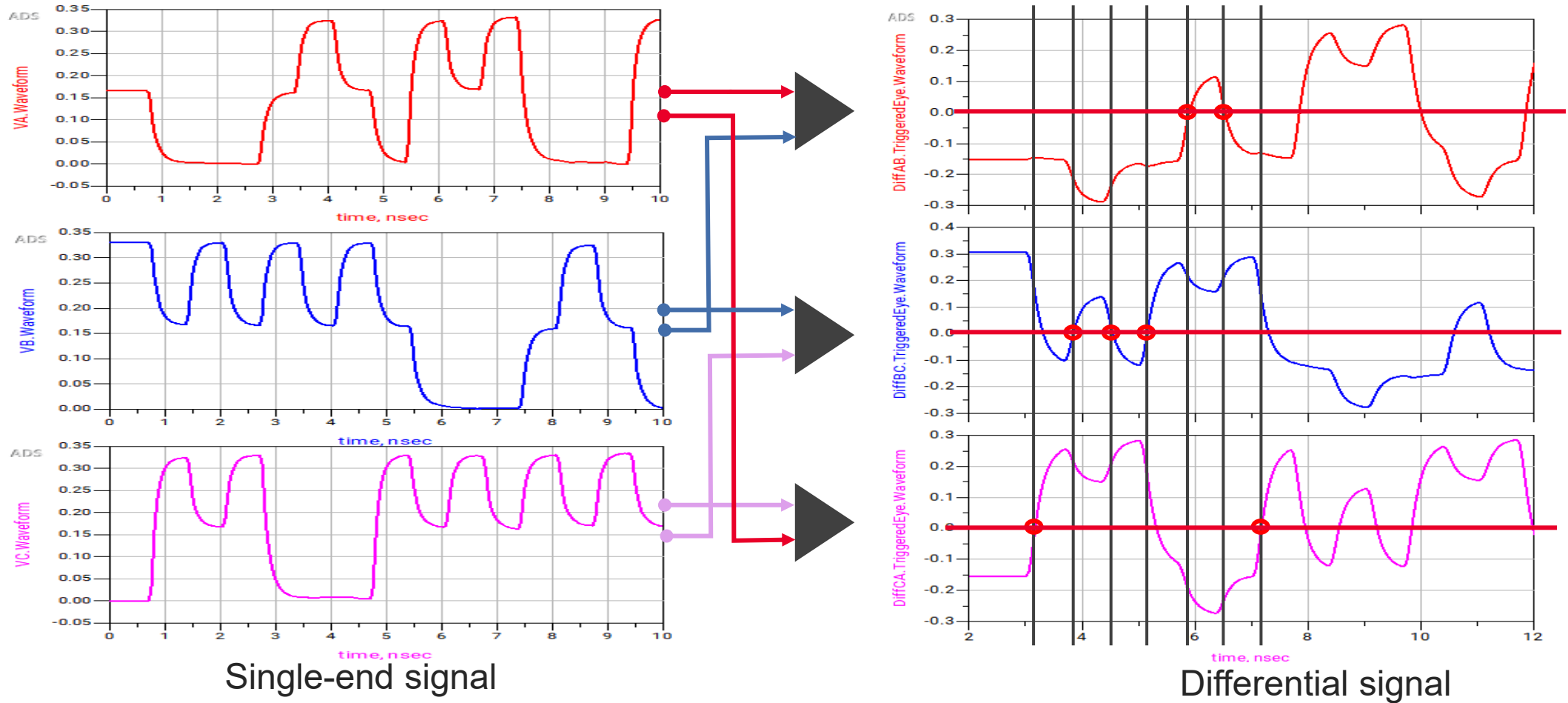
Encoding

Wire State	VA	VB	VC
+x	3/4 V	1/4 V	1/2 V
-x	1/4 V	3/4 V	1/2 V
+y	1/2 V	3/4 V	1/4 V
-y	1/2 V	1/4 V	3/4 V
+z	1/4 V	1/2 V	3/4 V
-z	3/4 V	1/2 V	1/4 V

Wire State

Correct C-PHY Encoding

Coding ensures every UI has at least ONE 0V crossing for clock recovery

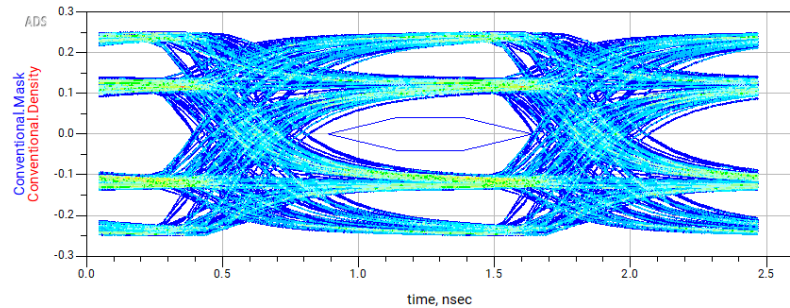
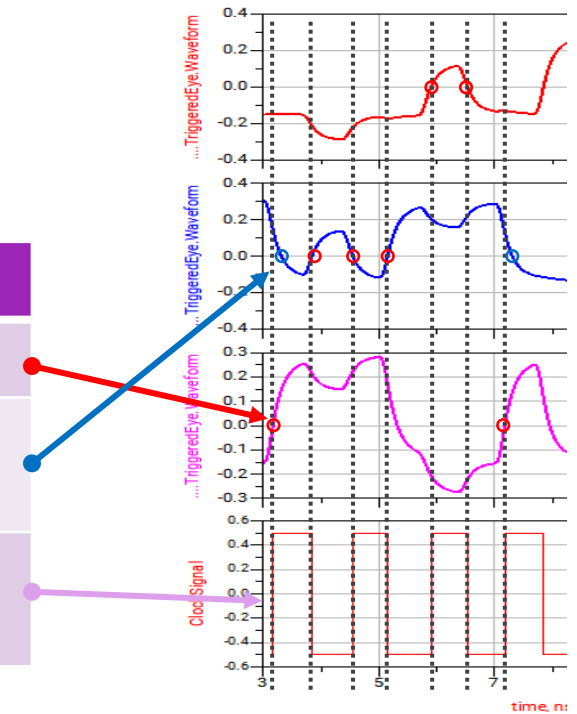


C-PHY source must have mapping and encoding

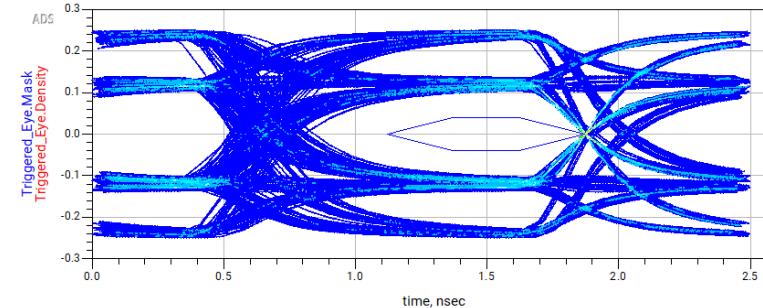
C-PHY Signal Quality Check with Eye Diagram

Non-triggered vs Triggered Eye

	Non-triggered	Triggered eye
Clock edge	Center of eye	At the first zero-crossing
Clock source	Single waveform	3 waveforms, ignore subsequent edges in the same UI
Data sample point	Center of eye	Prior to the trigger point



Non-triggered Eye



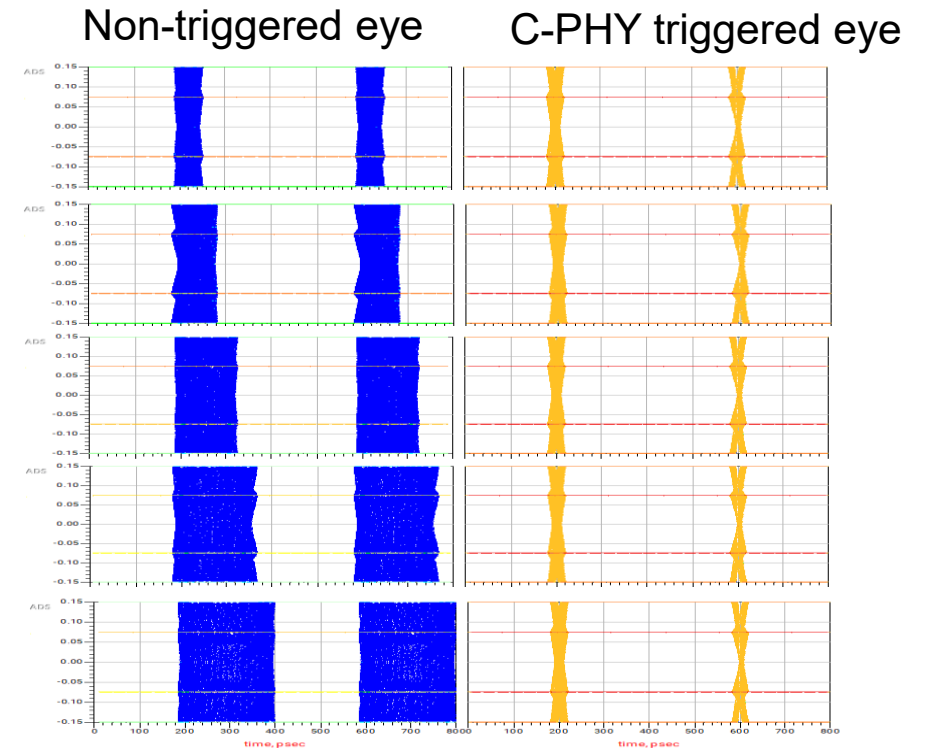
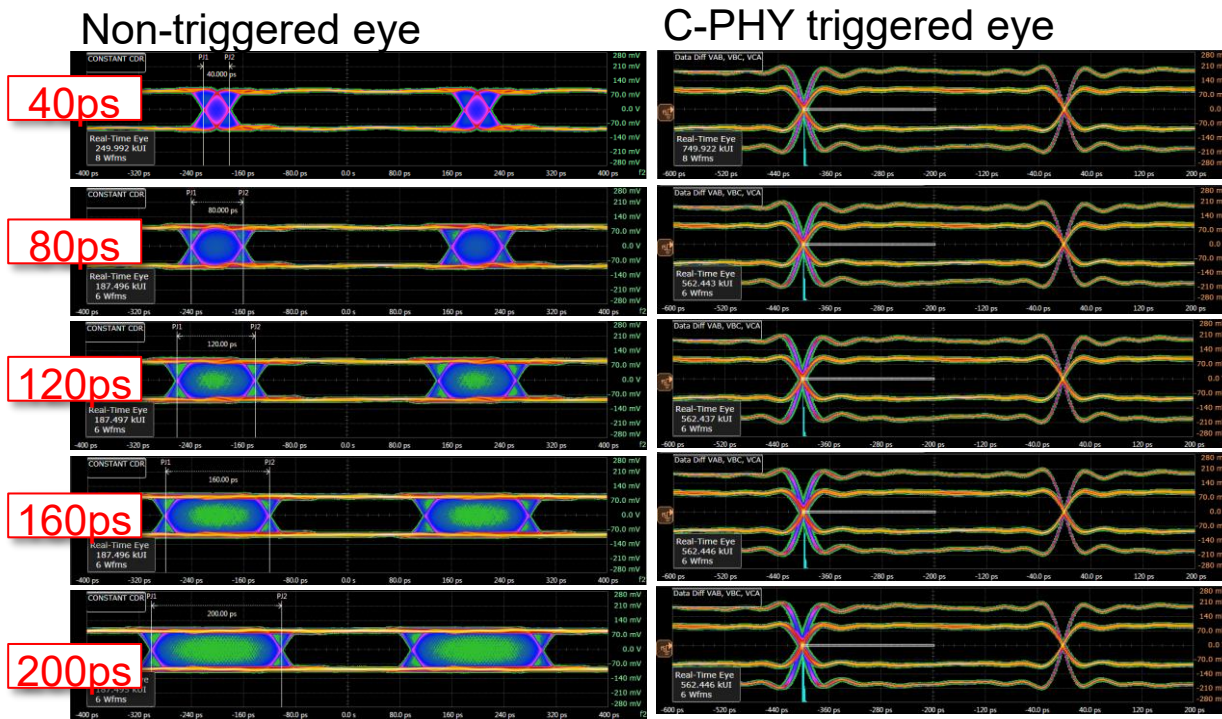
Triggered Eye

2Gsps, 100mUI, 100MHz PJ

Impact of Jitter on C-PHY Eye Diagrams

C-PHY's Jitter Resilience

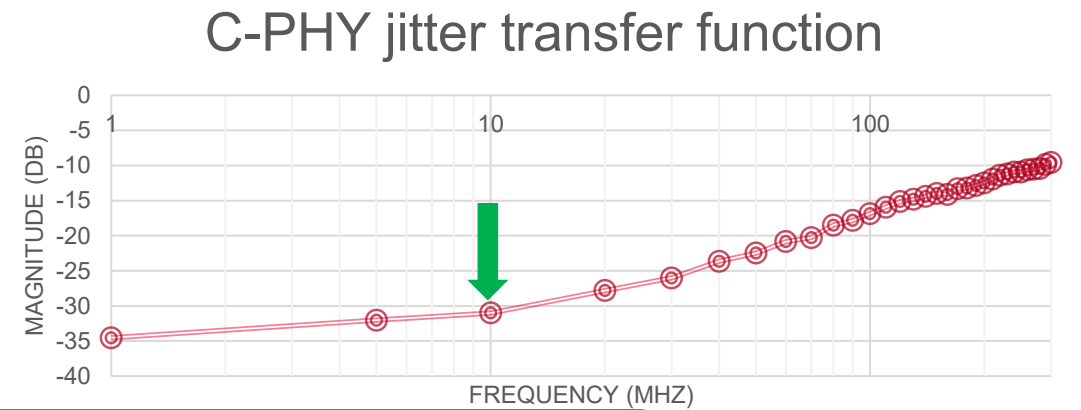
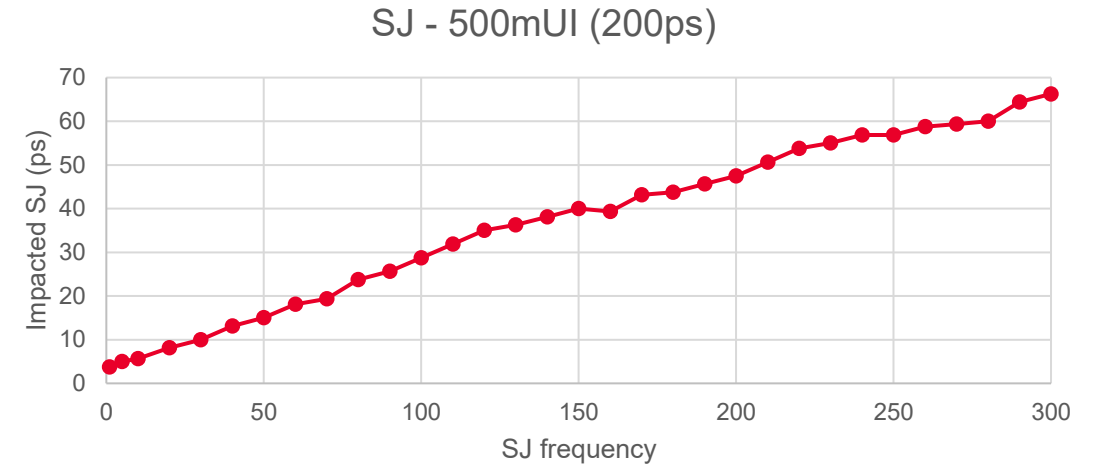
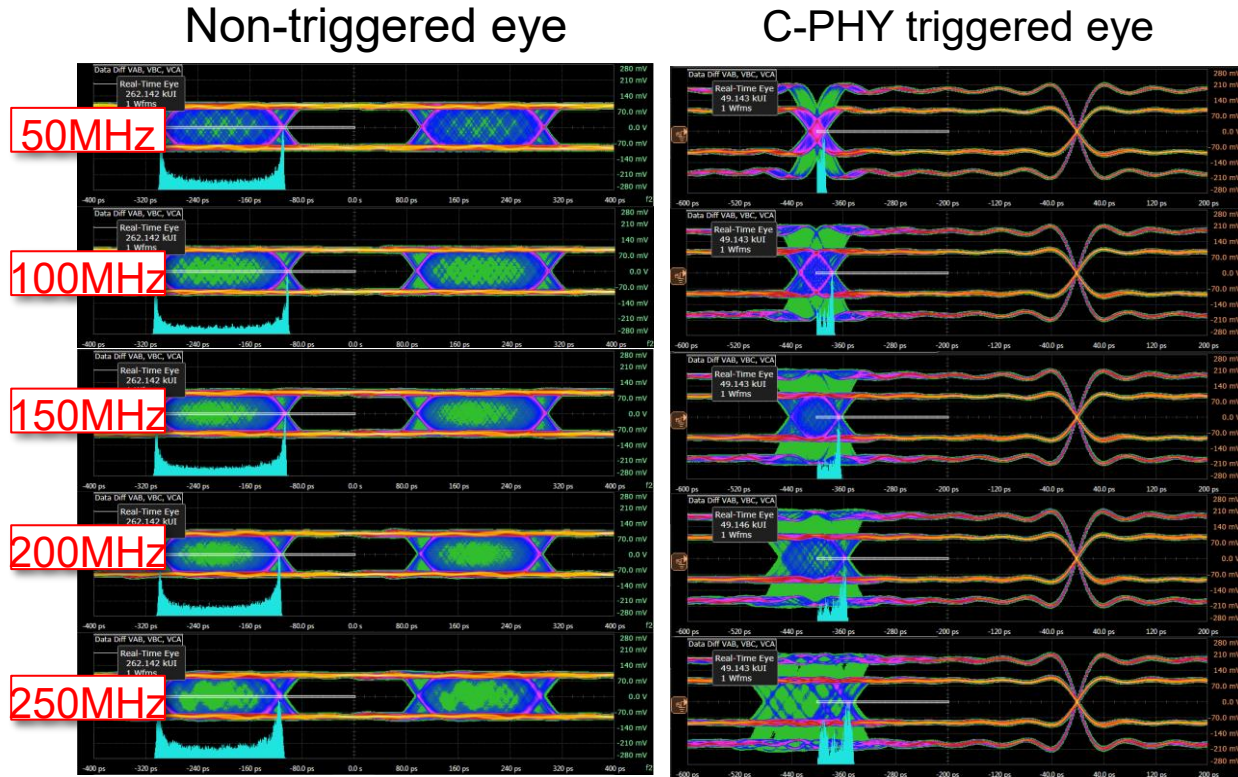
- A triggered eye is resistant to jitter



2.5Gps, 10MHz PJ

Importance of C-PHY Triggered Eye Support

Only triggered eye shows the right behavior of the C-PHY eye diagram



C-PHY measurement must have Triggered eye

Utilization of C-PHY Equalization

Verifying CTLE Support in C-PHY Receivers

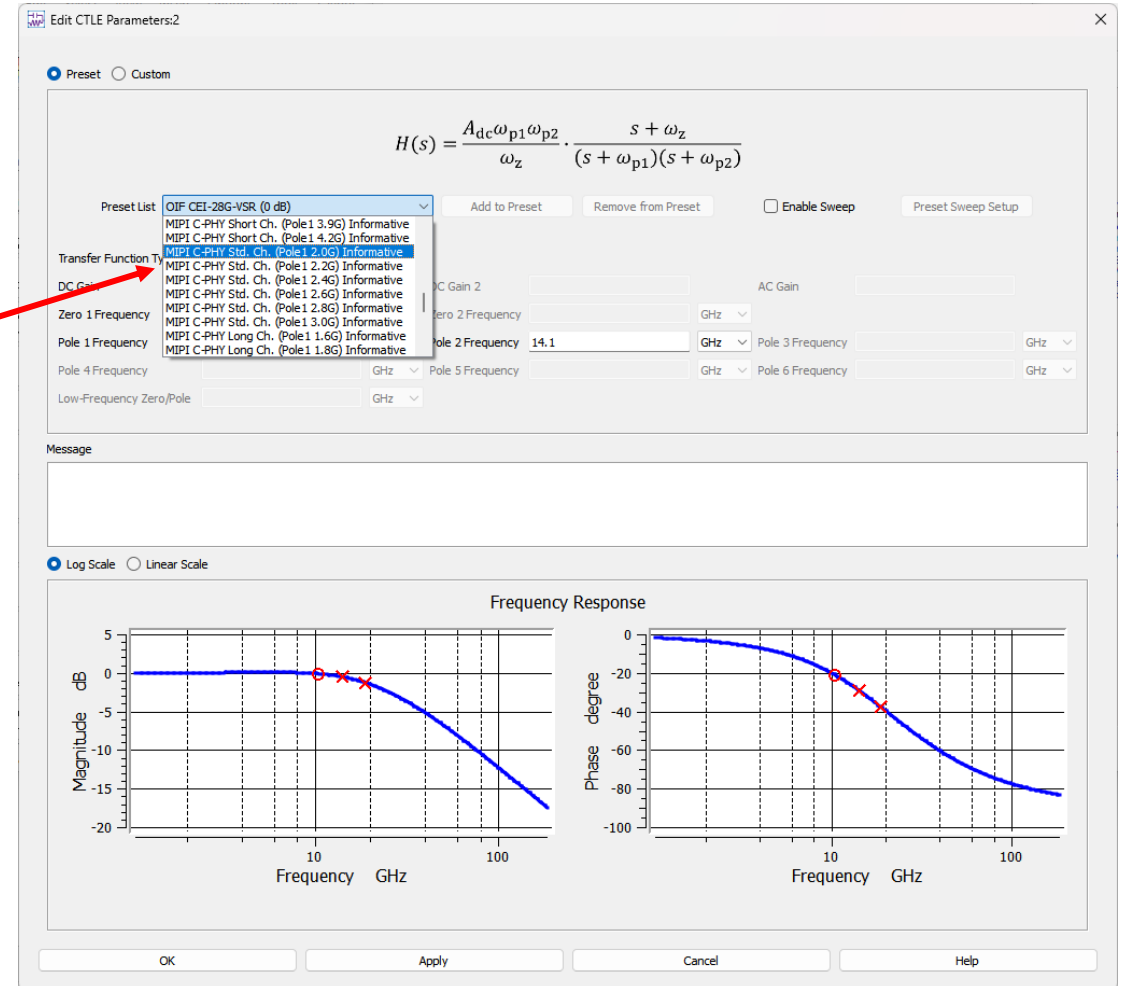
- From C-PHY v2.0 and on, Rx CTLE (Continuous Time Linear Equalization) is required.

fz (GHz)	fp1 (GHz)	fp1 / fz	fp2 (GHz)
1.0	2.0	2.0	10
1.0	2.2	2.2	10
1.0	2.4	2.4	10
1.0	2.6	2.6	10
1.0	2.8	2.8	10
1.0	3.0	3.0	10

Reference CTLE for standard channel

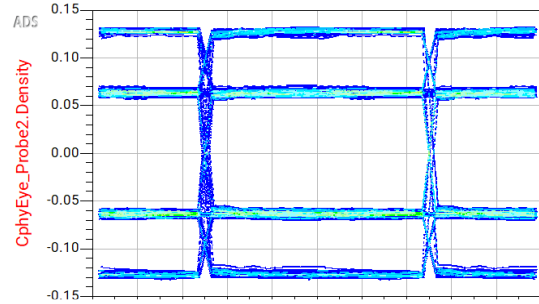
$$H(s) = \frac{A_{DC}\omega_{P1}\omega_{P2}}{\omega_z} \cdot \frac{s + \omega_z}{(s + \omega_{P1})(s + \omega_{P2})} \quad [\text{Equation 1}]$$

Where: A_{DC} is the DC gain,
 $\omega_{P1} = 2\pi f_{P1}$ f_{P1} is the first pole frequency
 $\omega_{P2} = 2\pi f_{P2}$ f_{P2} is the second pole frequency
 $\omega_z = 2\pi f_z$ f_z is the zero frequency

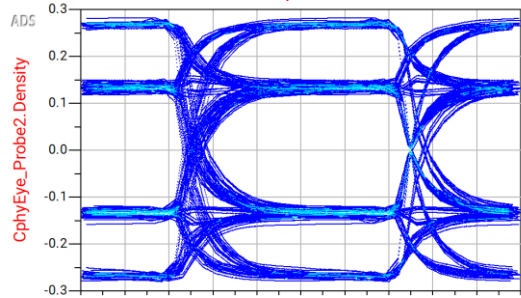


C-PHY receiver must support Equalization

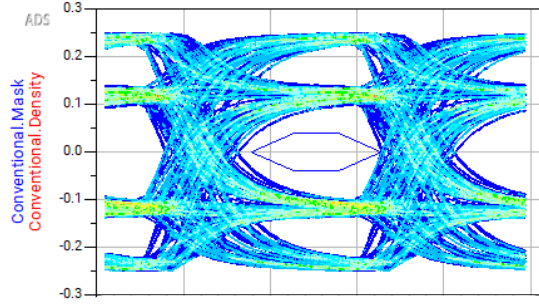
Summary



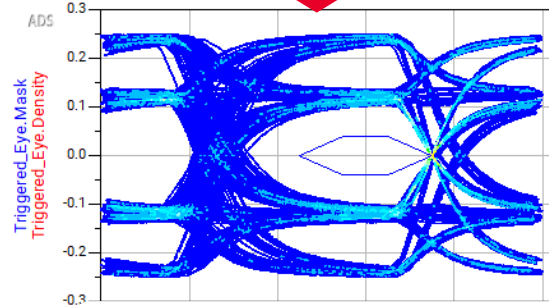
Behavior model



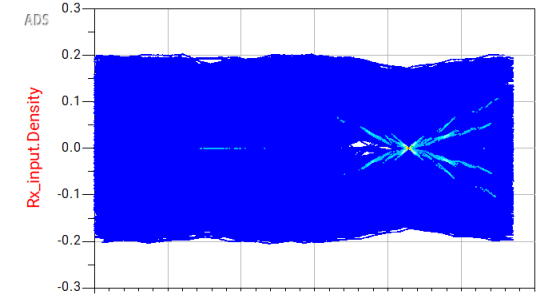
C-PHY Waveform source



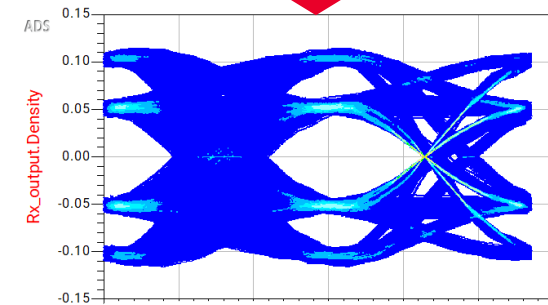
Non-triggered Eye



Triggered Eye



No Equalization



Receiver CTLE

Deliver Accurate Results

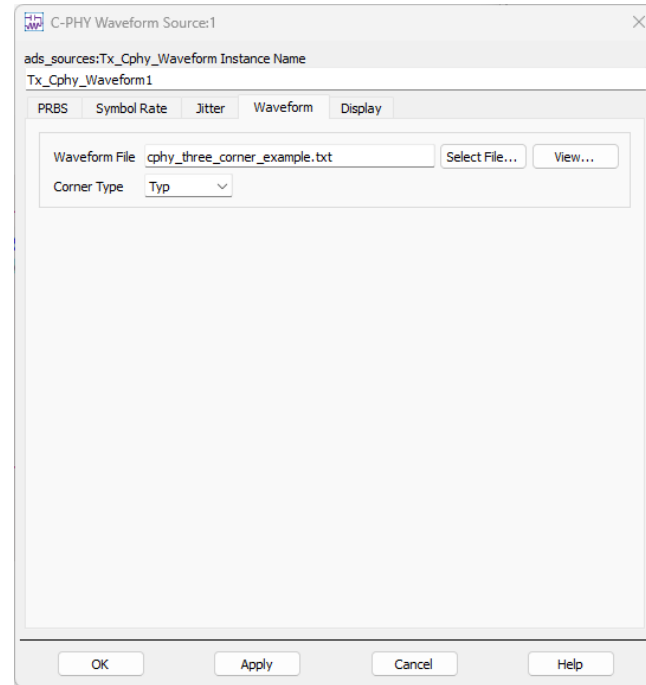
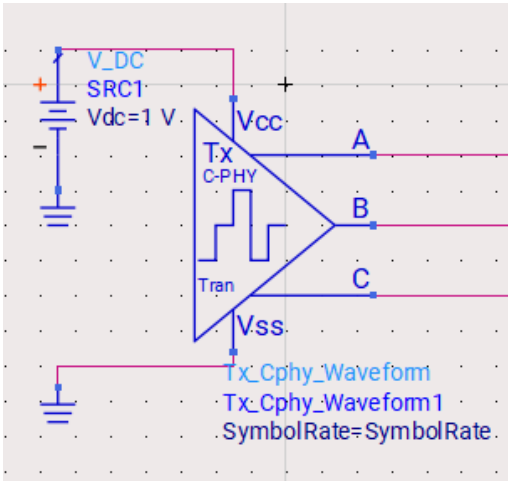
Comply with the Specification

Ensure Rx Accuracy

Innovative C-PHY Waveform Source

New, Innovative C-PHY Waveform Source

Beyond the limits of IBIS



Highlights:

- Industry-unique solution
- Measured waveform-based model
- 3 different corner cases: Typical, Min, Max

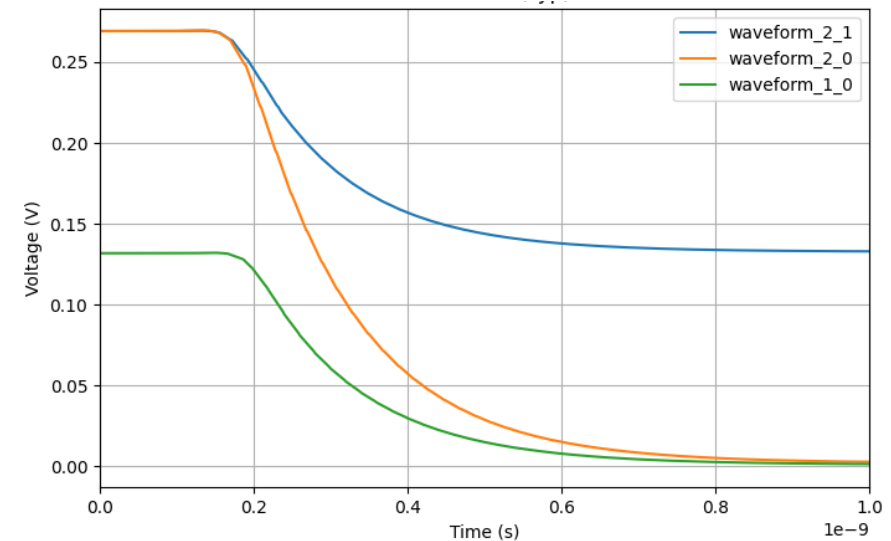
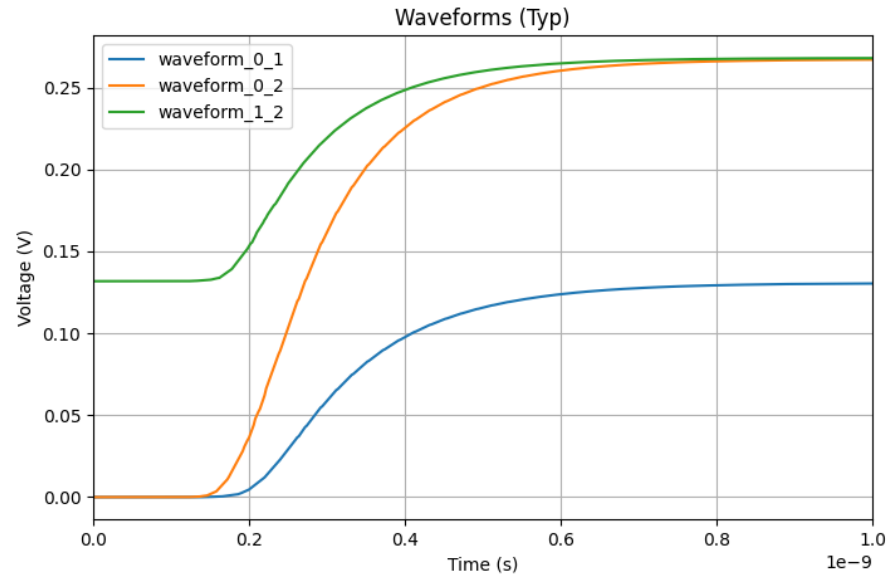
Advantage I with New C-PHY Waveform Source

Accurate silicon behavior from measured waveform

```
[Waveform_1_0]
R_fixture=50
V_fixture=0.0
|time      V(typ)
|
0.0000E+00
2.0000E-11
4.0000E-11
6.0000E-11
1.0000E-10
1.2000E-10
1.4000E-10
1.6000E-10
1.8000E-10
2.0000E-10
2.2000E-10
2.4000E-10
2.6000E-10
2.8000E-10
3.0000E-10

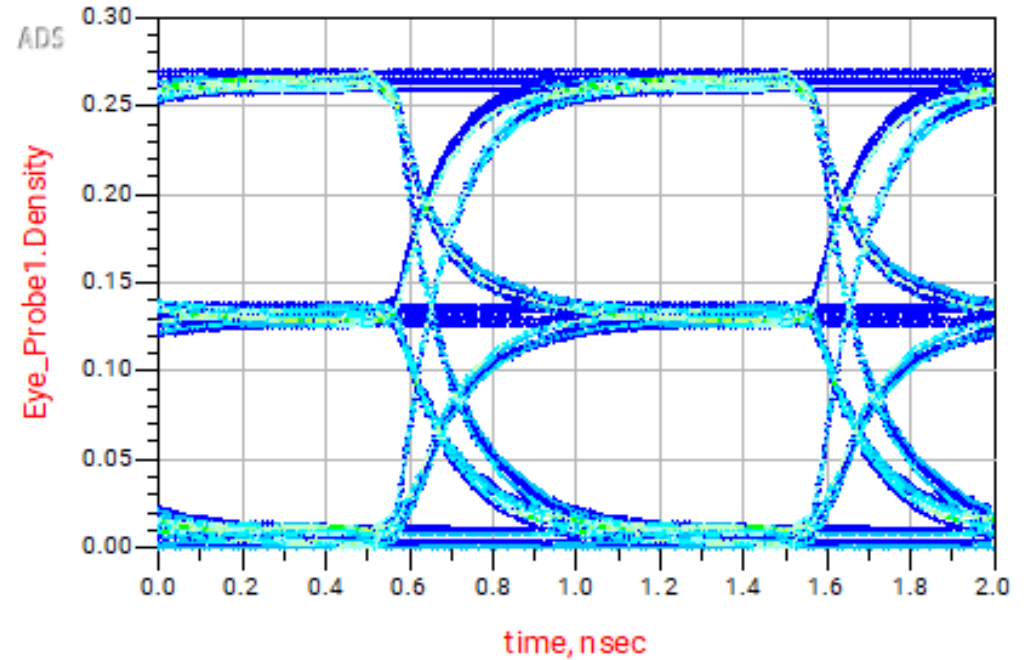
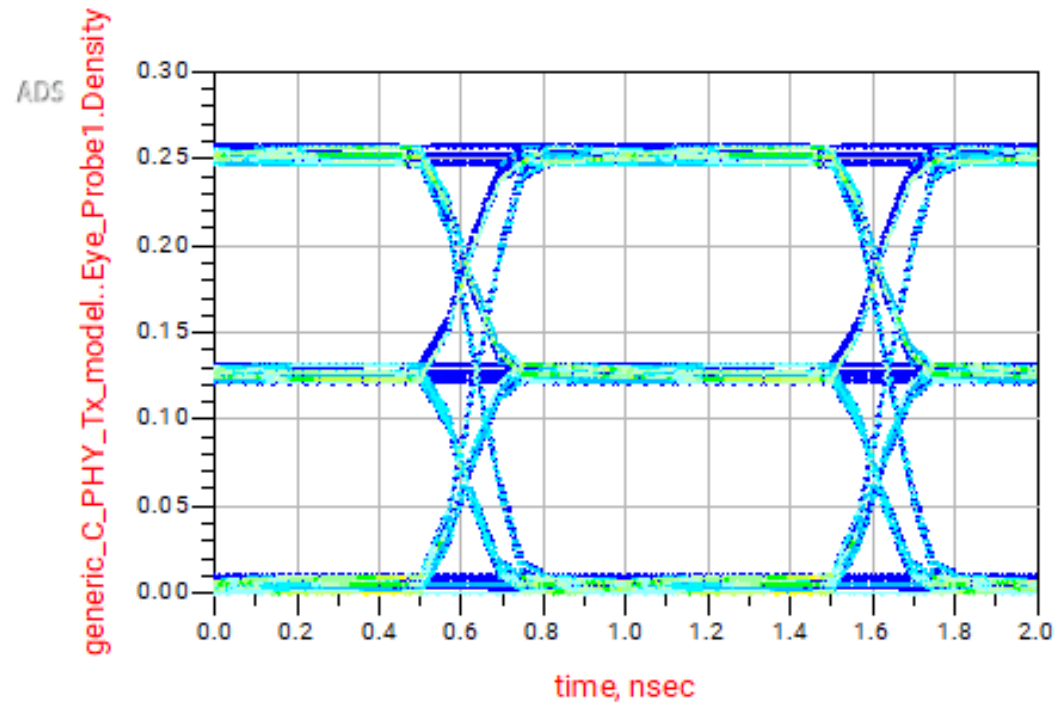
[Waveform_2_0]
R_fixture=50
V_fixture=0.0
|time      V(typ)
|
0.0000E+00
2.0000E-12
4.0000E-12
6.0000E-12
1.0000E-11
1.2000E-11
1.4000E-11
1.6000E-11
1.8000E-11
2.0000E-11
2.2000E-11
2.4000E-11
2.6000E-11
2.8000E-11
3.0000E-11

[Waveform_2_1]
R_fixture=50
V_fixture=0.0
|time      V(typ)
|
0.0000E+00      2.6920E-01
2.0000E-12      2.6920E-01
4.0000E-12      2.6920E-01
6.0000E-12      2.6920E-01
1.0000E-11      2.6920E-01
1.2000E-11      2.6920E-01
1.4000E-11      2.6920E-01
1.6000E-11      2.6920E-01
1.8000E-11      2.6920E-01
2.0000E-11      2.6920E-01
2.2000E-11      2.6920E-01
2.4000E-11      2.6920E-01
2.6000E-11      2.6920E-01
2.8000E-11      2.6920E-01
3.0000E-11      2.6920E-01
3.2000E-11      2.6920E-01
```



Advantage I with New C-PHY Waveform Source, cont...

Accurate Eye Diagram prediction

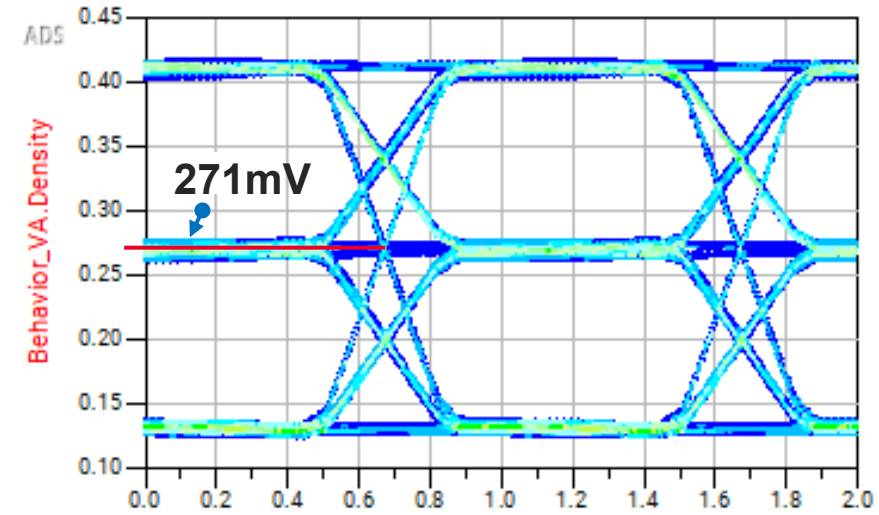
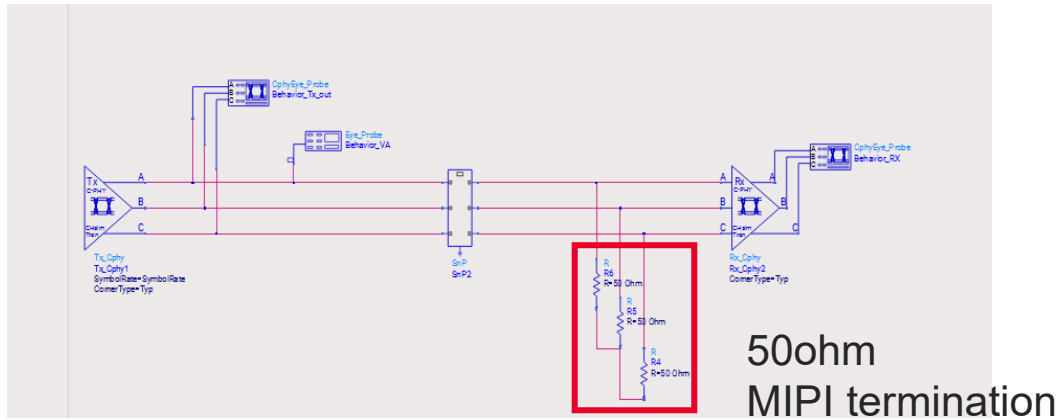


Represents true C-PHY transition behavior

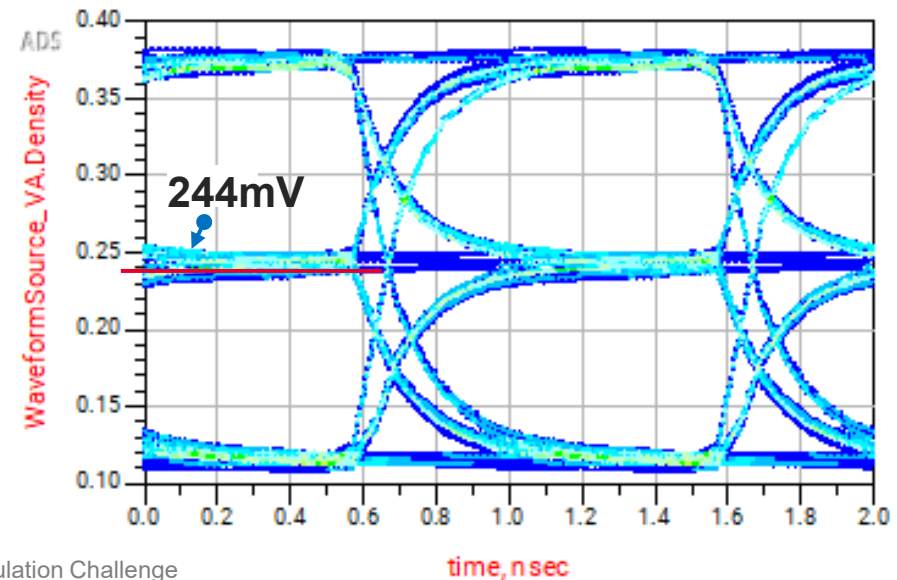
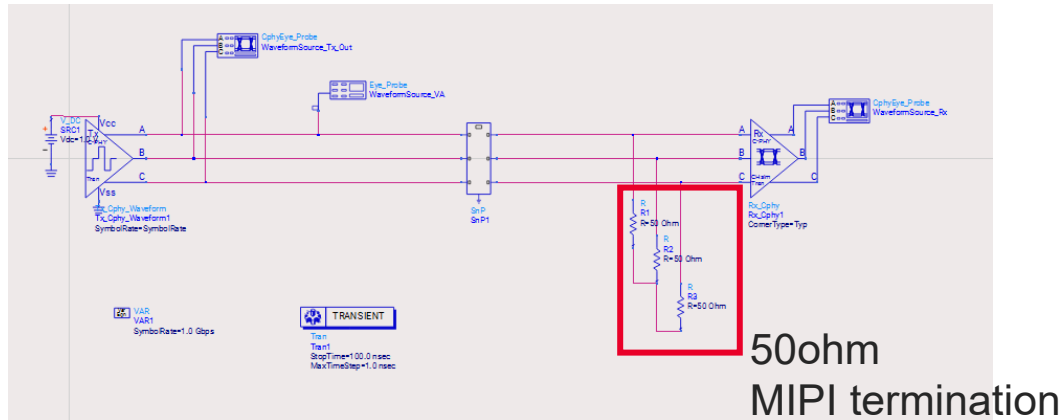
Advantage II with New C-PHY Waveform Source

Accurate non-linear DC offset behavior modeling

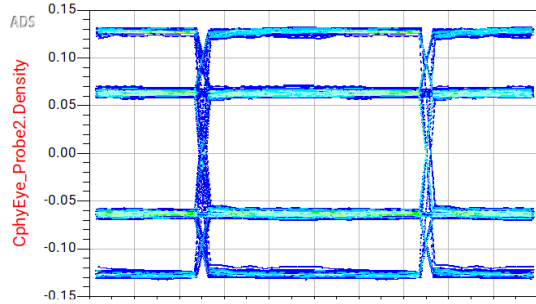
Behavior model



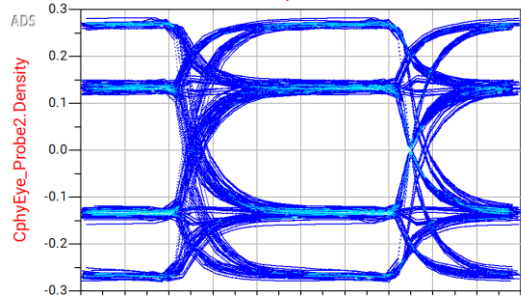
Waveform source



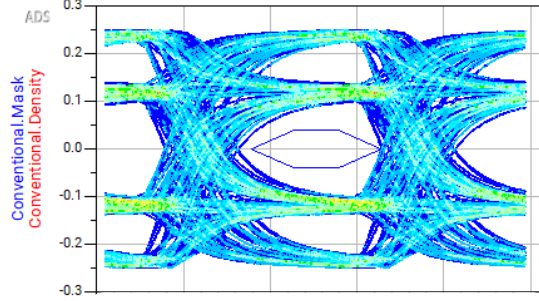
Summary



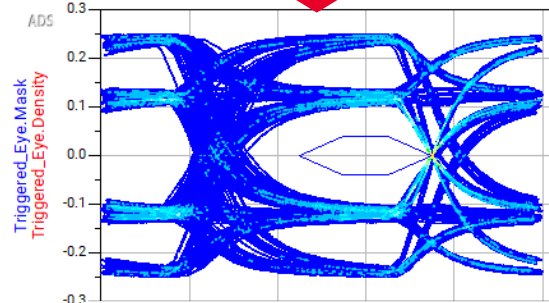
Behavior model



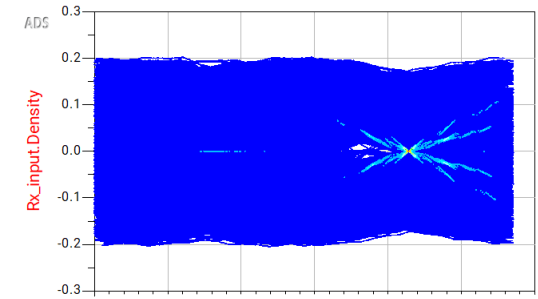
C-PHY Waveform source



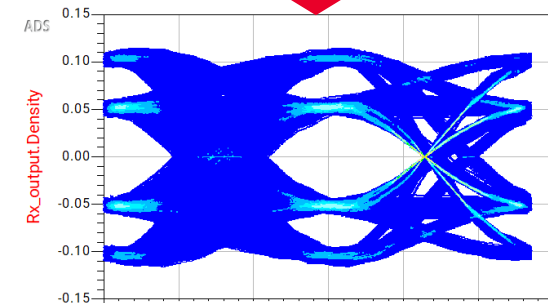
Non-triggered Eye



Triggered Eye



No Equalization



Receiver CTLE

Deliver Accurate Results

Comply with the Specification

Ensure Rx Accuracy

