IBIS Power Integrity Introduction

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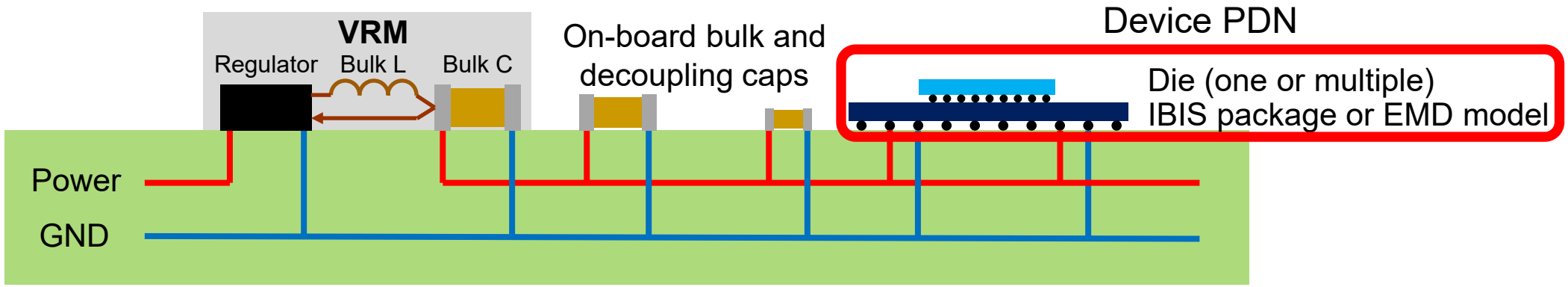
Overview

- Introduction
- Terminology definitions
- Load Models and Device PDN Models of package and die
- Device PDN Model
- Load Model
- Examples of analysis that can be done with these models
- Examples of [Device PDN Model] and [Load Model]
- Discussion Points, Next Steps

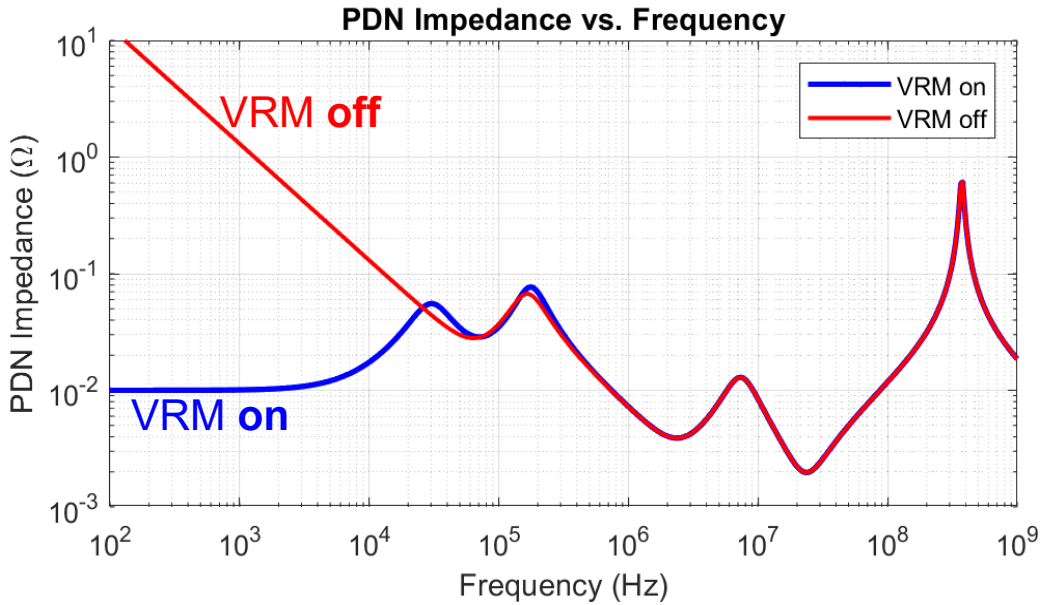
Introduction: Background

- BIRD 223.1 proposed SPIM (Streamlined Power Integrity Model) for IBIS to support power integrity simulations
  - The BIRD was approved in November 2023, but a few problems were discovered later
- The proposal in this presentation attempts to resolve those problems without eliminating or restricting any of the features in BIRD 223.1
- This proposal includes a few additional features and capabilities which were not present in BIRD 223.1
  - Most notable is the separation of the information into two distinct areas:
    - [Device PDN Model] – contains the definition of the package and on-die interconnect SPICE subcircuit or Touchstone S-parameter model, including decoupling capacitors if present
    - [Load Model] – contains the definition of current sources (loads) and probes (target impedance, IR drop, etc.)

Introduction: VRM and PDN



Power Delivery Network on PCB (Board PDN)



PDN impedance: with vs. without VRM

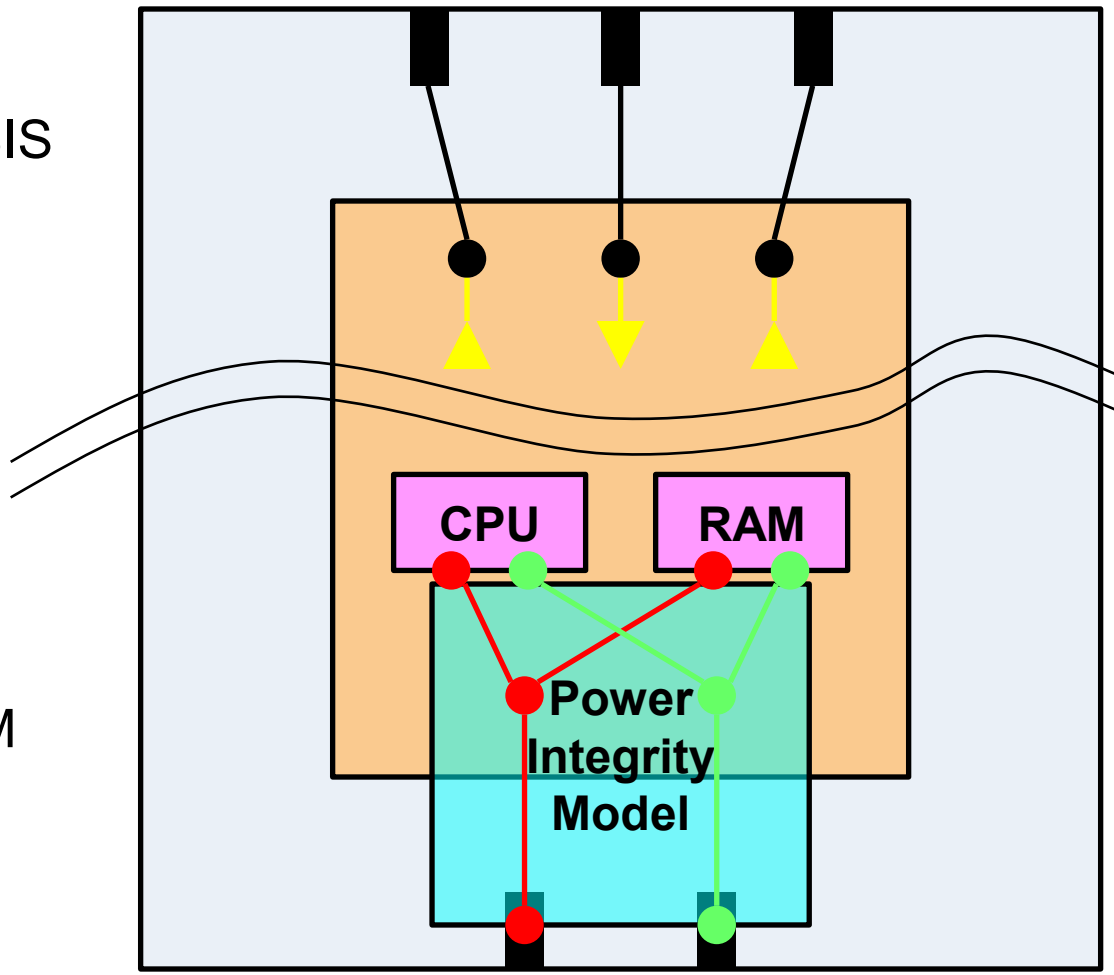
VRM plays an important role in the PDN, especially at low frequencies

Adapted from: *Behavioral Modeling and Parameter Extraction of VRMs for Power Integrity Analysis,* Hybrid IBIS Summit at IEEE EMC+SIPI 2025

PIM with IBIS

Normal IBIS

IBIS-PIM



IBIS “pins”

IBIS package

IBIS “pads”

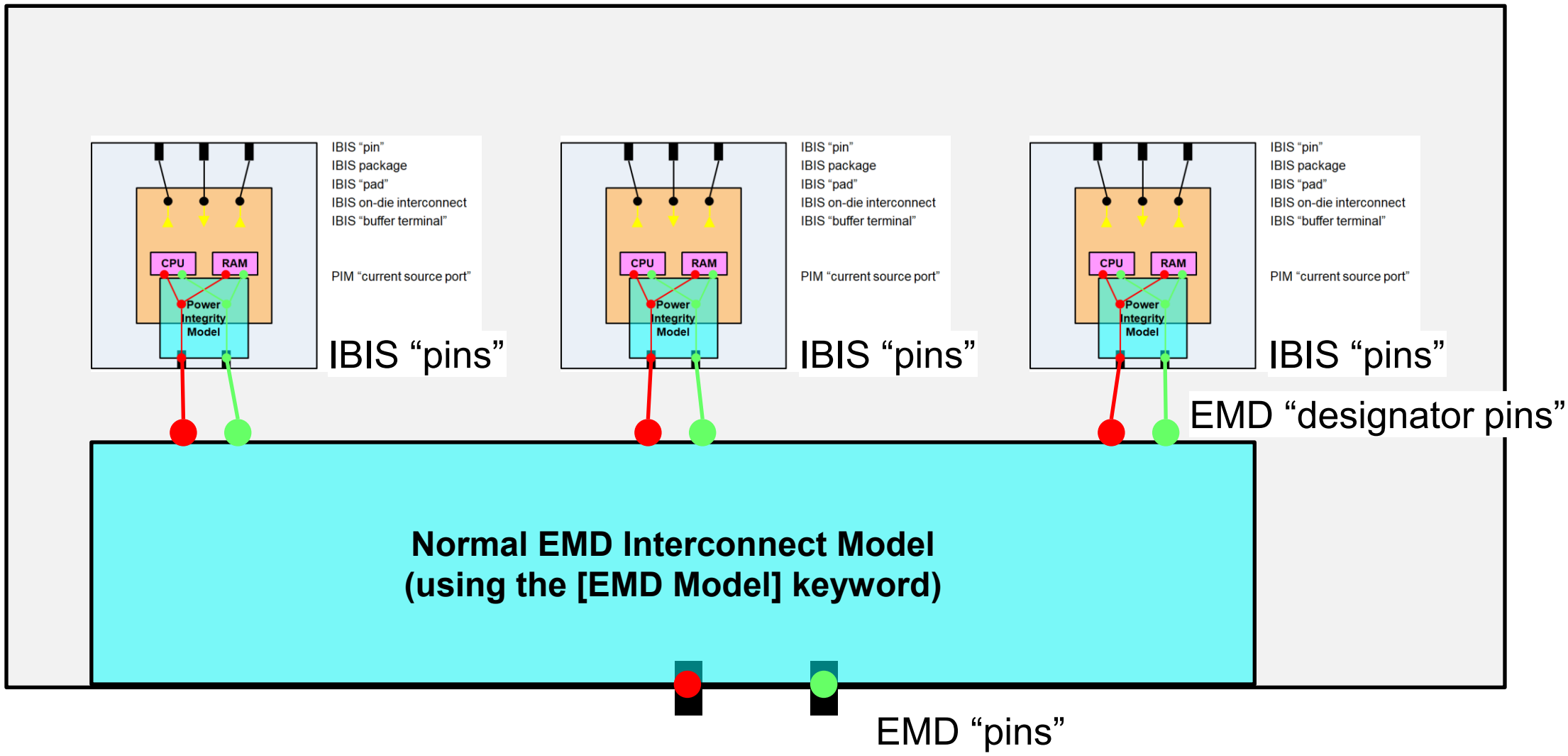
IBIS on-die interconnect

IBIS “buffer terminals”

PIM “current source ports”

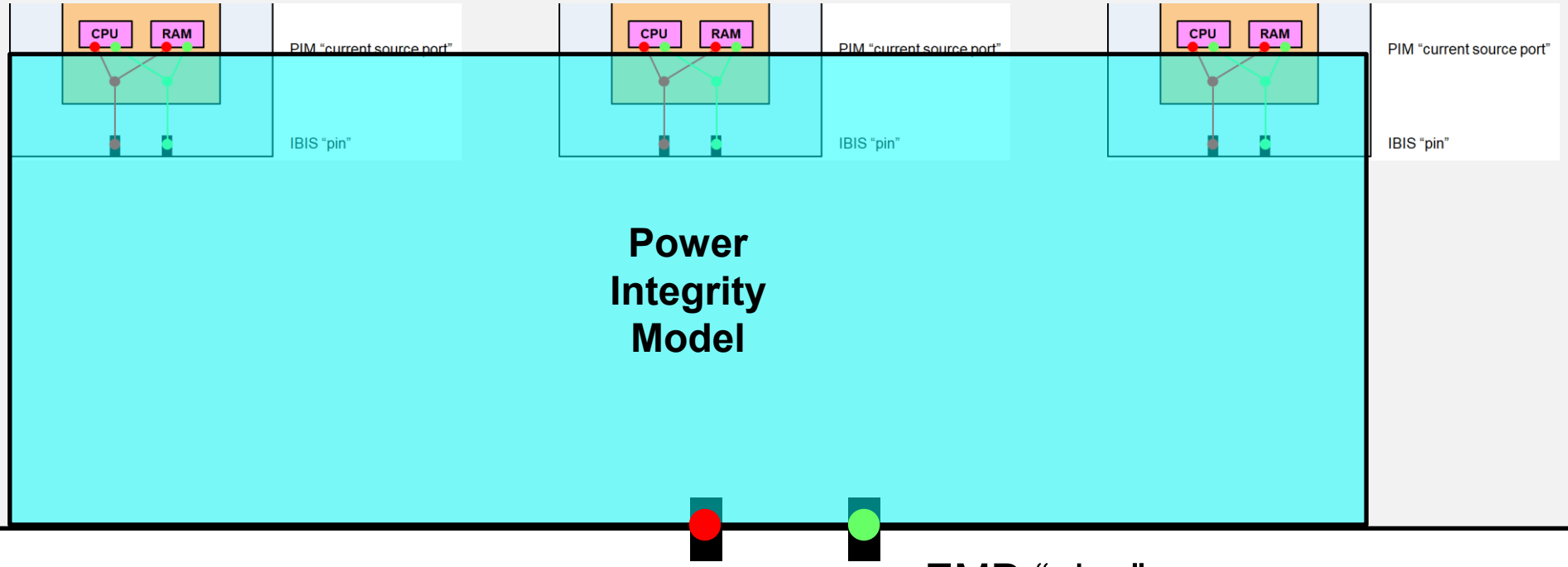
IBIS “pin” = PIM “pin ports”

PIM with EMD (with normal [EMD Model] in EMD and PIM in IBIS)



PIM with EMD (with one PIM for EMD and IBIS)

No IBIS models (from [EMD Parts] / [EMD Designator List]) are instantiated, PIM current sources and probes are defined instead. This boils down to the same as a "normal" PIM with IBIS. The only difference is that instead of IBIS [Pin], it references [EMD Pin List] and the names of current sources and probes might include the die number/name.



Standalone PIM or PIM invoked from IBIS or EMD

- A PIM may be used standalone, without depending on any other files
  - In this case the .pim file relies on a pin list defined by its own pin list keyword
- A PIM may be invoked from a .ibs file
  - In this case the .pim file relies on the pin list located in the [Pin] keyword of the .ibs file
  - The .ibs file will need a new keyword to invoke PIM in the .pim file, similar to how the [Package Model] keyword can point to a .pkg file
- A PIM may be invoked from an .emd file
  - In this case the .pim file relies on the pin list located in the [EMD Pin List] keyword of the .emd file
  - The .emd file will need a new keyword to invoke PIM in the .pim file

Terminology used in this Presentation - basics

- **Die pad** refers to the connection point between the integrated circuit die and its package. The term includes wire bond pads, bump pads, and any other 2D and 3D chip connection methodologies.
- **Device pin** refers to the connection point between a package and a printed circuit board. The term includes devices with physical pins (DIP, SOIC, etc.), balls (BGA), flat no-lead packages (DFN, QFN, etc.) and any other device connection methodologies.
- An **IBIS file** (*.ibs) represents one or more devices (using the [Component] keyword), describing the behavior of I/O buffers on the die and the interconnect between the terminals of the I/O buffers and die pads (on-die interconnect) and between the die pads and device pins (package).
- An **EMD file** (*.emd) describes an electrical module, which may be a printed circuit board (PCB), or a substrate that carries multiple devices or other modules, or a multi-chip module (MCM), or a stacked die device, or an interposer, etc. An EMD file has two main interfaces. One of these interfaces defines the connections to the PCB (or another module) through a set of user-visible **EMD pins**. The other interface defines the connections to the devices (or other EMD modules) using a set of **device pins**. The PCB, MCM, stacked die device, interposer, etc. models in EMD files are called **EMD interconnect model**.
- A **Device PDN Model** is a behavioral representation of the entire power delivery network (PDN) between the device (or EMD) pin interface and one or more power consuming locations on the die which may represent computational units, memory, peripheral interfaces, etc.

Terminology used in this Presentation – terminals and ports

- Device PDN Models reference either an IBIS-ISS (SPICE) subcircuit or a Touchstone file. Connections to SPICE subcircuits are made through "**terminals**" and connections to Touchstone files are made through "**ports**".
- Each Touchstone port has two "terminals". In simulation netlists the second terminal (reference) of a port may be connected to A_gnd (aka node 0) or any other SPICE node.
  - IBIS-ISS (SPICE) supports three different port referencing syntaxes for instantiating a Touchstone model with the S-element. E.g., for an .s2p model:
    - N Sxyz n1 n2 model=ModelName
    - N+1 Sxyz n1 n2 <ref> model=ModelName
    - 2N Sxyz n1 <ref1> n2 <ref2> model=ModelName
  - where <ref>, <ref1>, <ref2> may be "0" (for global ground) or any other SPICE node.
- The EDA tool may decide which S-element syntax to use, but **the fundamental requirement is that:**
  - **ports connected together must use the same reference node**
  - **ports connected to SPICE subcircuit terminals must use the same reference node**

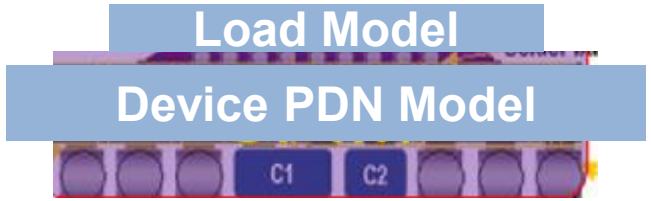
Terminology used in this Presentation – PIM specifics

- A **current source** represents a power consuming unit on the die which may be a computational unit, memory, peripheral interface, etc., on the die or device. It is up to the model maker to decide how many current sources are needed to adequately describe the power consumption characteristics of the die or device.
  - Current sources may be attached only to dedicated SPICE current source terminals or Touchstone current source ports.
- A **probe** represents a measurement location (or observation point). A probe definition contains the properties and rules of the probe against which the EDA tool can evaluate the simulation results.
  - Probes may be attached to dedicated probe terminals or ports, current source terminals or ports, or pin terminals or ports.
- If current sources or probes are connected to ports, their “+” and “-” terminals are connected to the “+” and “-” terminals of the port, respectively.
- If current sources or probes are connected to terminals, their reference terminal may be explicitly connected to another terminal or may be implicitly connected to A_gnd (aka node 0).

Load Models and Device PDN Models of package and die

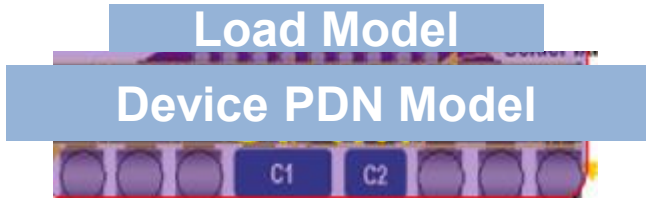
- Power Integrity Analysis tools require models that describe the current requirements on the die and describe the interconnect model between the device pins and the power consuming units on the die
- Load Model - describes the current requirements on the die
  - DC Load(s) for DC and AC analysis
  - PWL (Current vs. time waveforms)
  - Probe definitions with targets and rules
- Device PDN Model - describes the interconnect model between the device pins and the power consuming units on the die
  - Current Source Ports may have individual or grouped current sources
    - Grouping may be used to limit the complexity of the model and protect IP
  - Device Pin Ports or terminals
    - Grouping may be used to limit complexity of the model
  - Probe Ports
    - Provides dedicated observation points
  - Device PDN Models can be in the form of
    - Touchstone file
    - IBIS-ISS SPICE subcircuit (RLC or resistor matrix)

Load Model



- Pairs with “Device PDN Model”
- Defines one or more Current Sources
  - Current sources are connected to Device PDN Model current source ports
  - Each Current Source can change Current Levels independently
  - Multiple Current Sources may be connected to a single Device PDN Model current source port
  - DC current levels
  - Rise and fall time from one DC level to another DC level
  - PWL current vs. time waveforms
    - IC Vendor can supply waveforms as a stress test
    - User can generate their own PWL waveforms to emulate current sources changing levels (in-line or external file)
- Defines one or more Probes
  - Can be associated with any port (Current Source Port, Pin Port, dedicated Probe Port)
  - Rules
    - Voltage range rule
    - Impedance target table / mask rule (in-line or external file)
    - Maximum Device Pin current rule

Device PDN Model



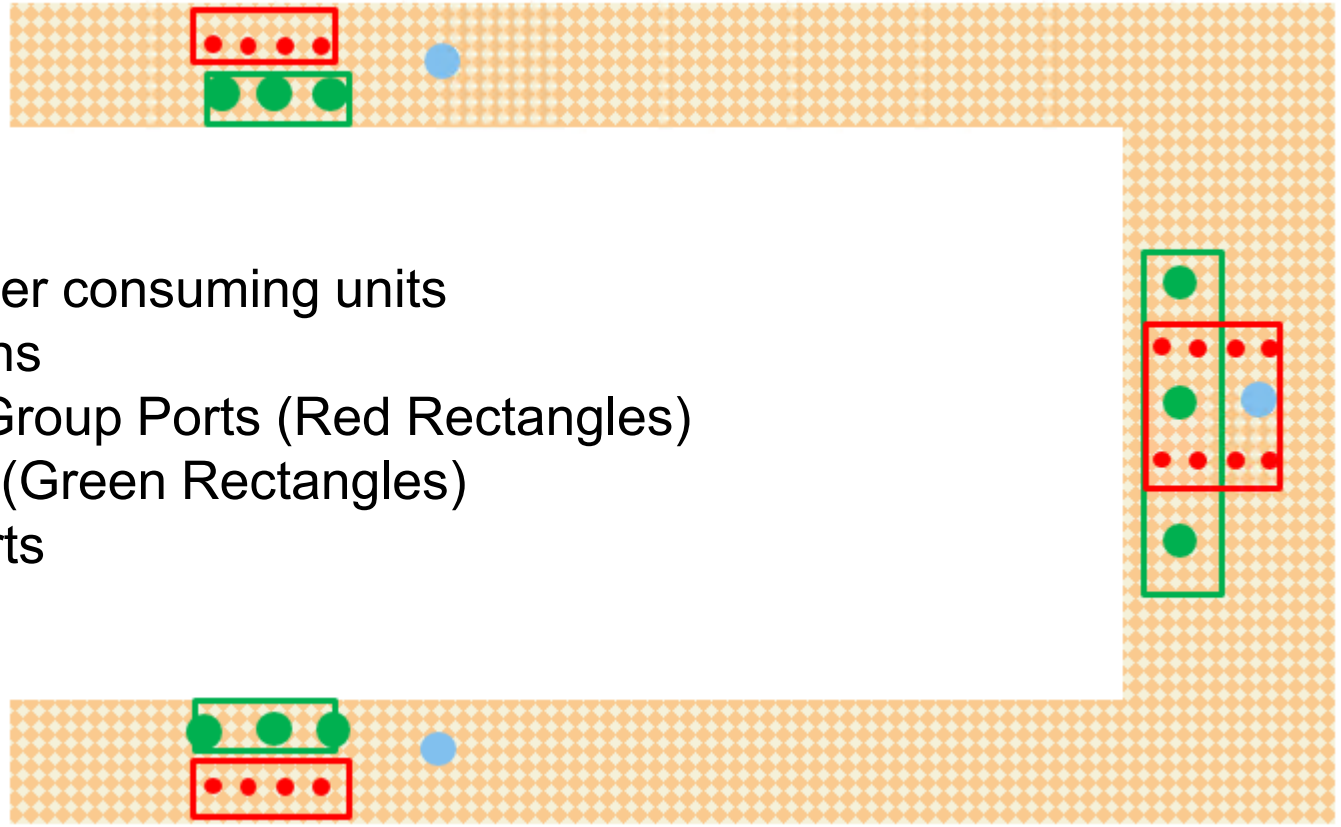
- Describes the package and on-die interconnect, including decoupling capacitors if present
- SPICE subcircuit or a Touchstone S-parameter file
- Device pins may be grouped into one or more “Device Pin Groups”
  - It is the responsibility of the EDA tool to mate the “Device Pin Groups” of the Device PDN Model to the Board PDN model
  - Can expose sense points for the VRM
- Die pads are **not defined** since Device PDN Models do not have “Die Pad Ports”
- Instead, Device PDN Models have “Current Source Ports” to which current sources, representing individual or grouped on-die power consuming units are connected
- In addition to “Device Pin” and “Current Source Ports”, Device PDN Models may have dedicated “Probe Ports”

Examples of Analysis That Can Be Done With These Models

- DC analysis
  - IR Drop
  - Thermal Hot Spots
- AC (Frequency Analysis)
  - Determine the impedance profile of PDN at Device Pins or on the die
- TD (Time Domain Transient analysis)
  - Vendor supplied current vs. time PWL table
  - User created current vs. time PWL table
  - Determine voltage droop

Tradeoff Product Cost, Design Cost, Power, Efficiency, Margins (Reliability)

A Modern Package Interconnect for one Rail Net Size ~2”x2”



- Red dots are ports at power consuming units
- Green dots are Device Pins
- 3 Power consuming unit Group Ports (Red Rectangles)
- 3 Device pin Group Ports (Green Rectangles)
- Blue dots are 3 Probe Ports

The Device Pins (green dots) are connected to the PCB and have Pin Numbers to mate to the board
The power consuming unit Group Ports (red rectangles) are connected to current sources (Load), and their XY coordinates on the die are hidden from the user

Simple DC Example

```
[Device PDN Model]      PImodelName_1
   File_IBIS-ISS        Vdd_DC.iss   SubcktName
   Analysis_type        DC
   Number_of_terminals = 2
      1  Pin_Signal_Name   Vdd
      2  Current_Source
[End Device PDN Model]
```

```
[Rail Signal Name]      Vdd_1p8
   [Load Model]         LoadModelName_1
      Analysis_type     DC   PImodelName_1

      [Current Source]  CurrentSourceName_1
         Terminal       2
         |              Idle      Thermal  Turbo
         Current        1         5        10
      [End Current Source]

      [Probe]           ProbeName_1
         Voltage_target       1.8      1.7      1.9
         DC_max_pinCurrent    0.2
      [End Probe]

      [Probe List]      Port/Terminal
         ProbeName_1    1
         ProbeName_1    2
      [End Probe List]
   [End Load Model]
[End Rail Signal Name]
```

Simple DC Example

```
[Device PDN Model]      PImodelName_1
   File_IBIS-ISS        Vdd_DC.iss    SubcktName
   Analysis_type        DC
   Number_of_terminals = 2
      1  Pin_Signal_Name   Vdd
      2  Pin_Signal_Name   Vss
      3  Current_Source
      4  Current_Source
      5  Current_Source
[End Device PDN Model]
```

```
[Rail Signal Name]      Vdd_1p8
   [Load Model]         LoadModelName_1
      Analysis_type     DC   PImodelName_1

      [Current Source]  CurrentSourceName_1
         Terminal       3   5
         |              Idle      Thermal   Turbo
         Current        1         5         10
      [End Current Source]

      [Current Source]  CurrentSourceName_2
         Terminal       4   5
         |              Idle      Thermal   Turbo
         Current        1         5         10
      [End Current Source]

      [Probe]           ProbeName_1
         Voltage_target 1.8       1.7       1.9
         DC_max_pinCurrent  0.2
      [End Probe]

      [Probe List]      Port/Terminal
         ProbeName_1    1   2
         ProbeName_1    3   5
      [End Probe List]
   [End Load Model]
[End Rail Signal Name]
```

Simple TD Example

With Implicit Node 0 Reference

```
[Device PDN Model]      PImodelName_2a
   File_TS              Vdd.s2p
   Analysis_type        AC   TD
   Number_of_ports = 2
      1  Pin_Signal_Name   Vdd
      2  Current_Source
[End Device PDN Model]
```

With Explicit Reference

```
[Device PDN Model]      PImodelName_2b
   File_TS              Vdd.s2p
   Analysis_type        AC   TD
   Number_of_ports = 2
      1  Pin_Signal_Name   Vdd  Pin_Signal_Name   Vss
      2  Current_Source
[End Device PDN Model]
```

```
[Rail Signal Name]      Vdd_1p8
   [Load Model]         LoadModelName_1
      Analysis_type     TD   PImodelName_2a

      [Current Source]  CurrentSourceName_1
         Port           2
         |              Standby    Turbo
         Current        2          10
         Risetime       1.0e-10
         Current_waveform_file   FileName_1   WfmName_1
      [End Current Source]

      [Probe]           ProbeName_1
         Voltage_target 1.8        1.7        1.9
      [End Probe]

      [Probe List]      Port/Terminal
         ProbeName_1    1
         ProbeName_1    2
      [End Probe List]
   [End Load Model]
[End Rail Signal Name]
```

Simple AC Example

With Implicit Node 0 Reference

```
[Device PDN Model]      PImodelName_2a
   File_TS              Vdd.s2p
   Analysis_type        AC   TD
   Number_of_ports = 2
      1  Pin_Signal_Name   Vdd
      2  Current_Source
[End Device PDN Model]
```

With Explicit Reference

```
[Device PDN Model]      PImodelName_2b
   File_TS              Vdd.s2p
   Analysis_type        AC   TD
   Number_of_ports = 2
      1  Pin_Signal_Name   Vdd  Pin_Signal_Name   Vss
      2  Current_Source
[End Device PDN Model]
```

```
[Rail Signal Name]      Vdd_1p8
   [Load Model]         LoadModelName_1
      Analysis_type     AC   PImodelName_2b

      [Current Source]  CurrentSourceName_1
         Port           2
         Weight         1          | or Current
      [End Current Source]

      [Probe]           ProbeName_1
         Impedance_target_file   FileName1    TargetName1
      [End Probe]

      [Probe List]      Port/Terminal
         ProbeName_1    1
         ProbeName_1    2
      [End Probe List]
   [End Load Model]
[End Rail Signal Name]
```

Discussion Points, Next Steps

- Are we missing anything?
- Can/will IC Vendors supply this data?
- Need to handle return paths correctly!
- Can you use these models to do the analysis/simulation that you want/need to do?

- Next steps
  - Resolve any issues raised by this presentation
  - Review proposed BIRD
    - Names of keywords, parameters and rules
    - Does it meet the requirements specified above?

Thank you!