WAI 2026 · HANGZHOU

Hybrid IBIS Summit at IEEE WAI 2026

ML for Practical PCB PDN Design

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Missouri S&T

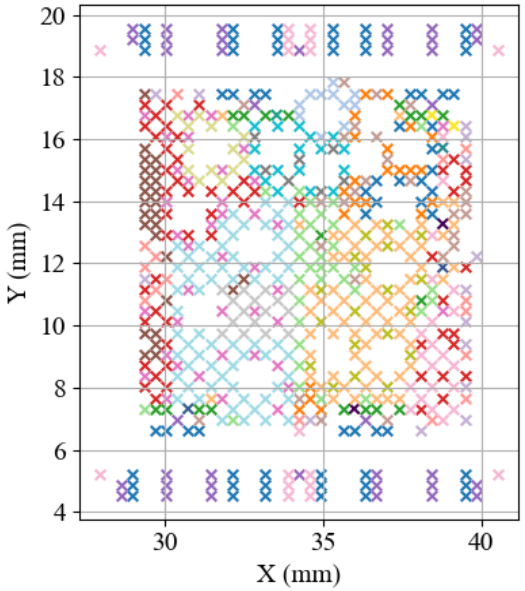
November 4–6, 2026 | Hangzhou, China

wai-emc.com/wai2026

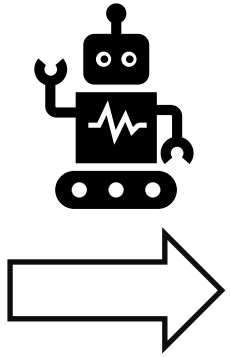
Autonomous PDN Design Synthesis

"Synthesize" layout (power shapes, vias, and decap placement) to meet DC/AC targets

Pin maps and stack-up are already determined

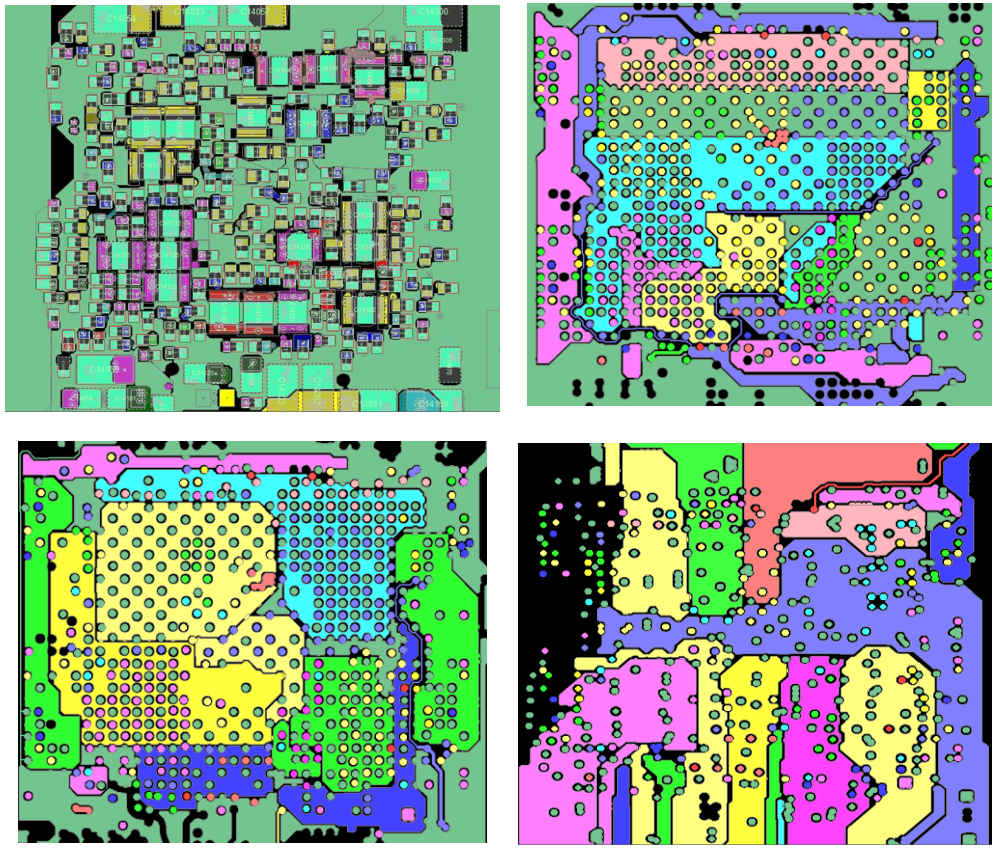


Pin Maps (SoC, PMIC)



Target impedance (AC)

Target DCR / IRdrop



Two Independent Design Flow (For Now)

DC

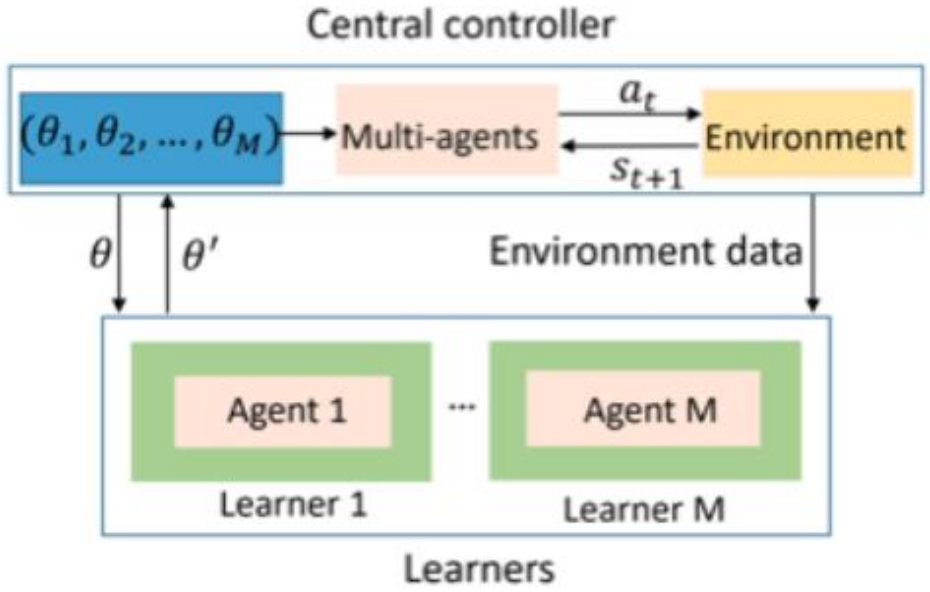
- Power shape synthesis (layout generation)
- DCR / IRdrop target–based
- Pre-fixed stack-up

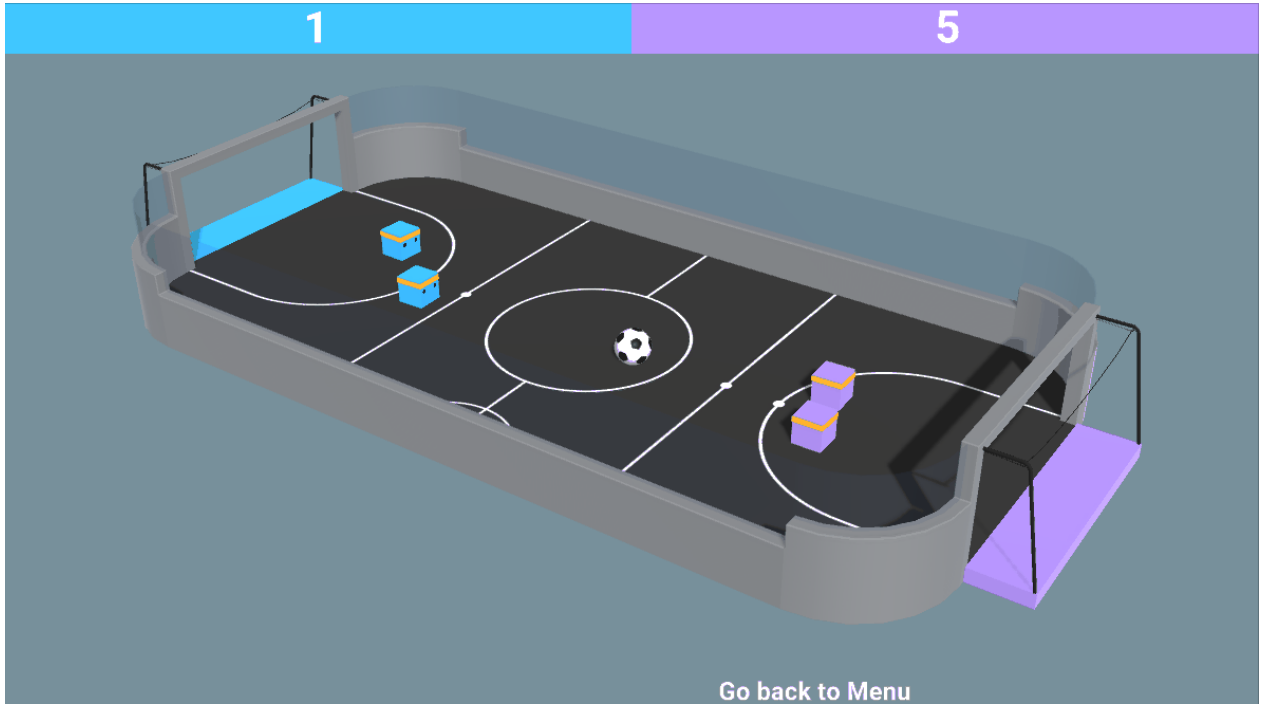
AC

- Decap location, package size, and value
- AC target impedance–based
- Fixed or variable BOM

Power Shape Layout Generation (DC)

Multi-Agent RL (MARL)





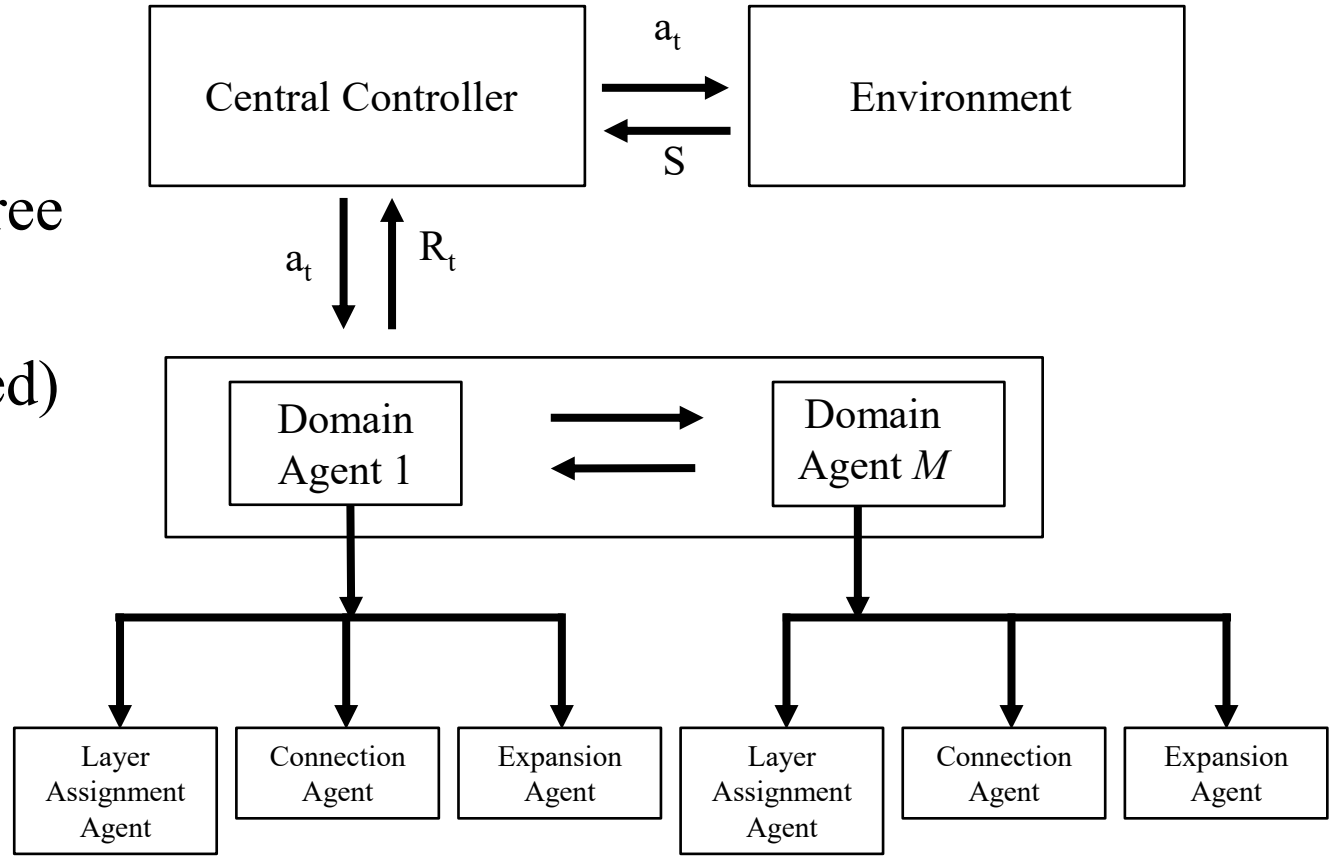
Well suited for multiple players (multiple power domains) sharing the same resources (space)

B. Wang, IEEE ICRA 2021. https://huggingface.co/learn/deep-rl-course/unit7/introduction-to-marl

MARL Framework for Layout Synthesis

The problem is divided hierarchically into three agents for each power domain

- Layer Assignment Agent (Q learning based)
- Connection Agent (multi-layer A *)
- Expansion Agent (grid-based)



H. Manoharan, "Multi-Agent Reinforcement Learning Based Power Plane Shape and Stackup Synthesis for Multi-Domain Power Delivery Networks" DesignCon 2026
H. Manoharan, "Pre-Layout Design Synthesis for Multi-Domain Power Distribution Networks using Hybrid Multi-Agent Reinforcement Learning" *IEEE T-SIPI.*

Graph Representation

Ports and pins:

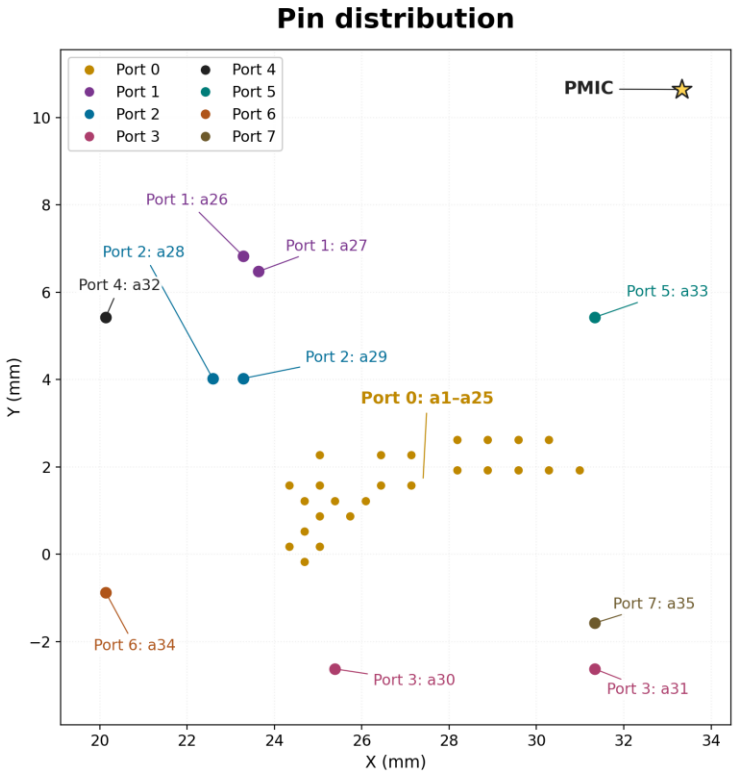
Each port has a known set of SoC pins and a spec.

Clusters as vertices:

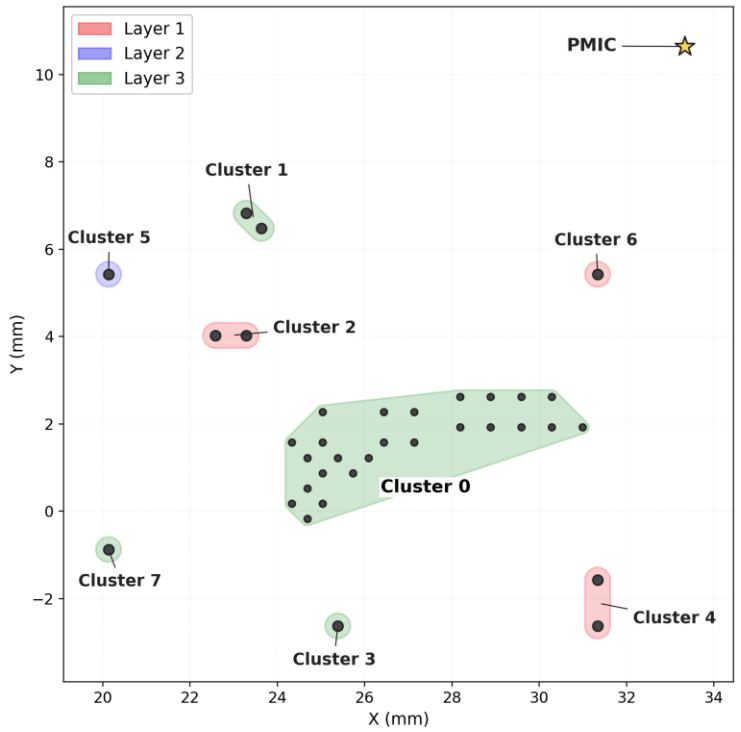
Group nearby pins into clusters and retain the pin-to-cluster and cluster-to-port relationships.

Connections as edges:

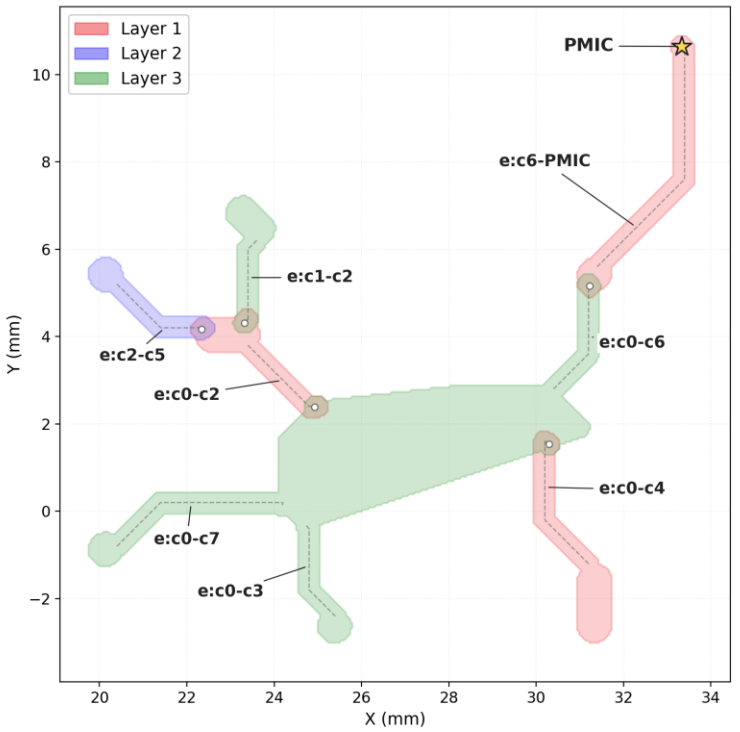
Route copper between clusters and the PMIC, then record the resulting graph connectivity



Known ports and their SoC pins



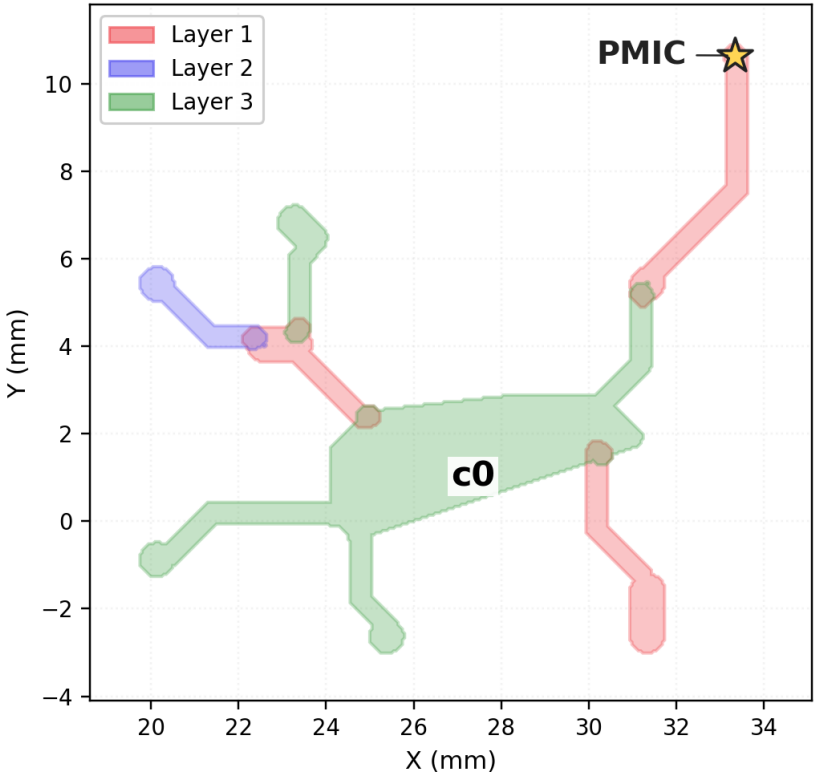
Clusters become graph vertices



Routed connections become graph edges

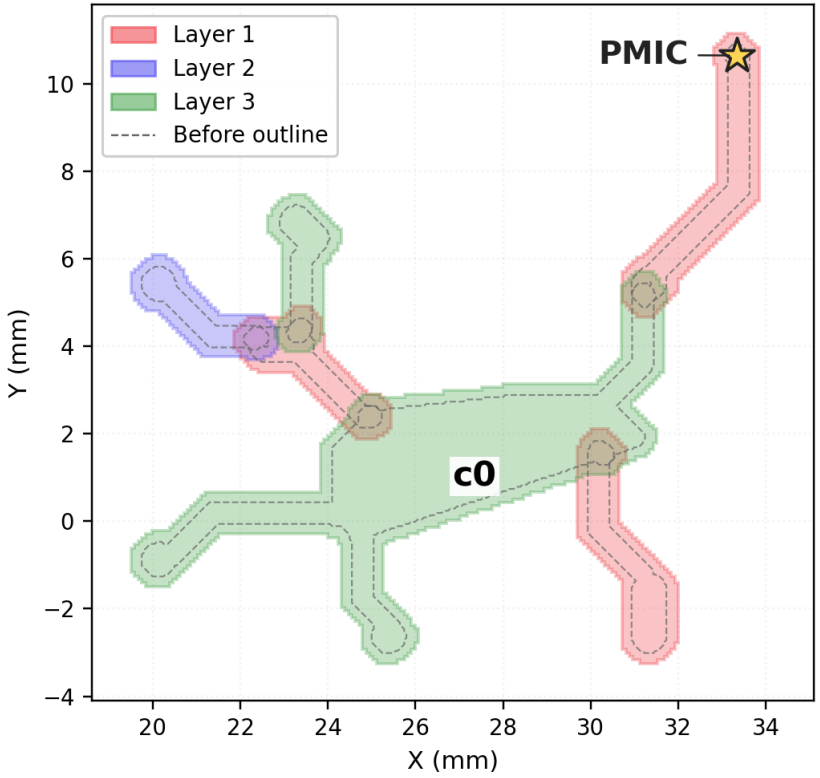
Physics-Guided Design: Smart Expansion

Before expansion



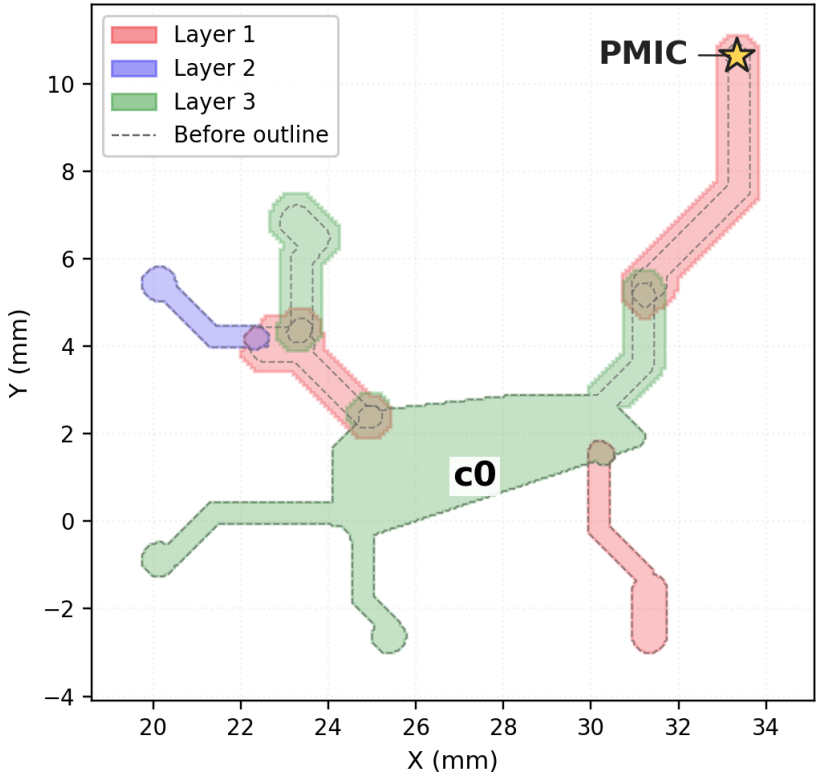
Copper area: 32.55 mm²

Uniform expansion



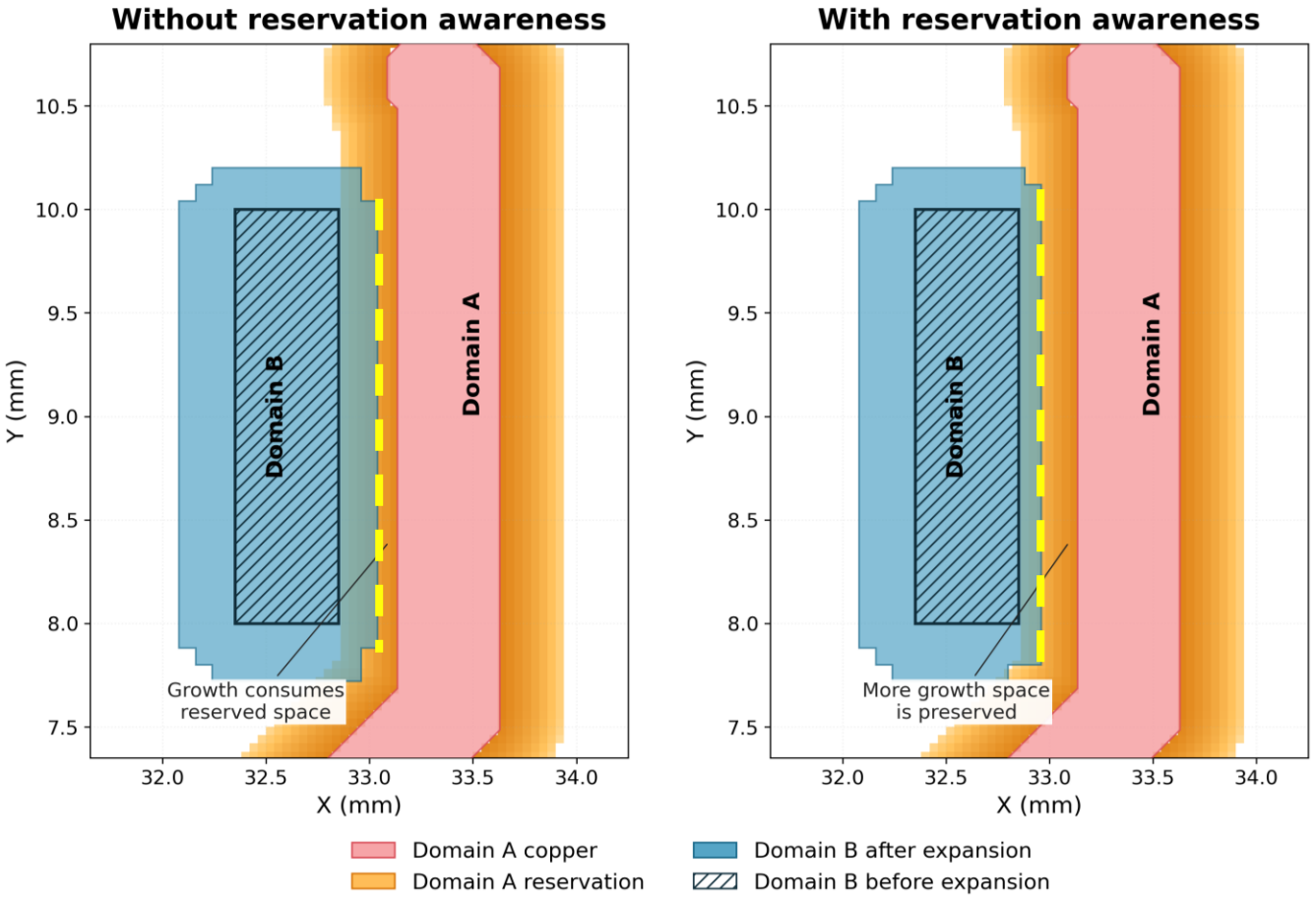
Copper area: 32.55 → 54.80 mm²

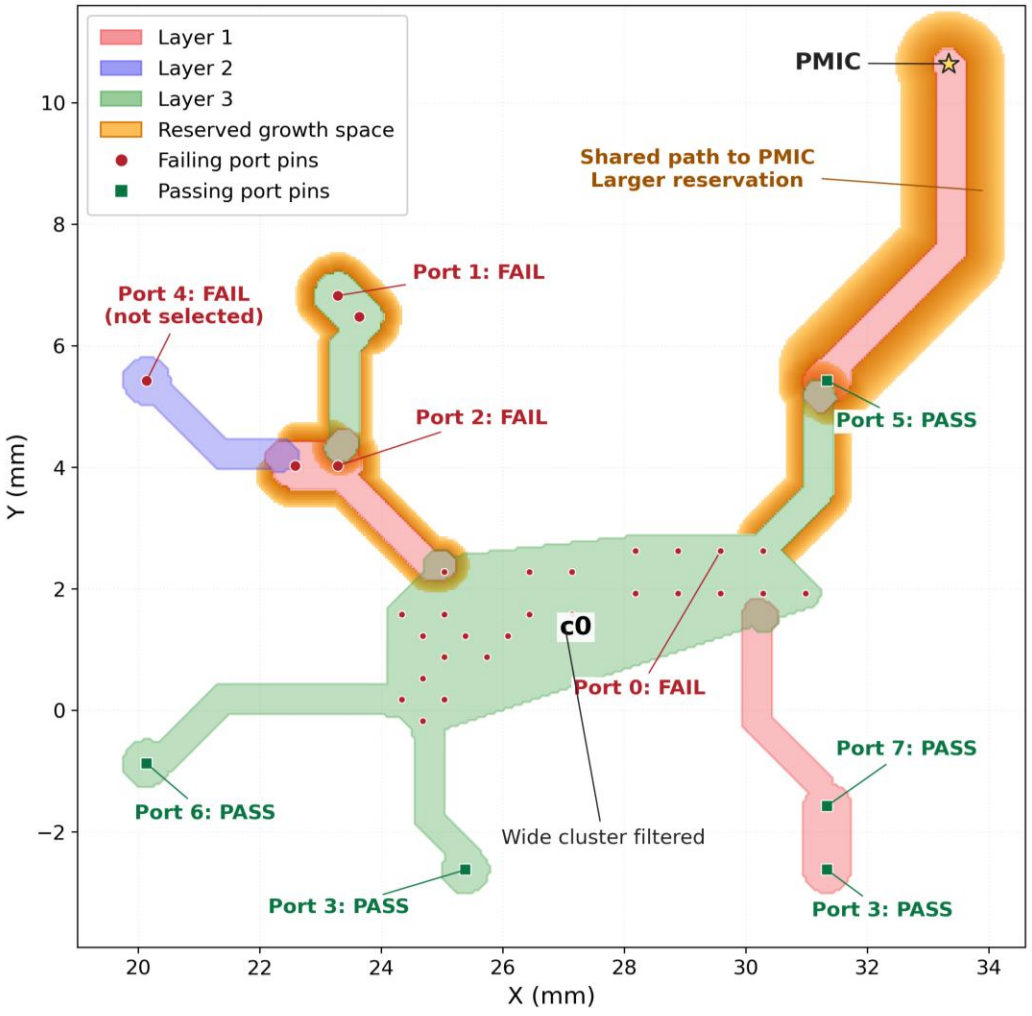
Smart expansion



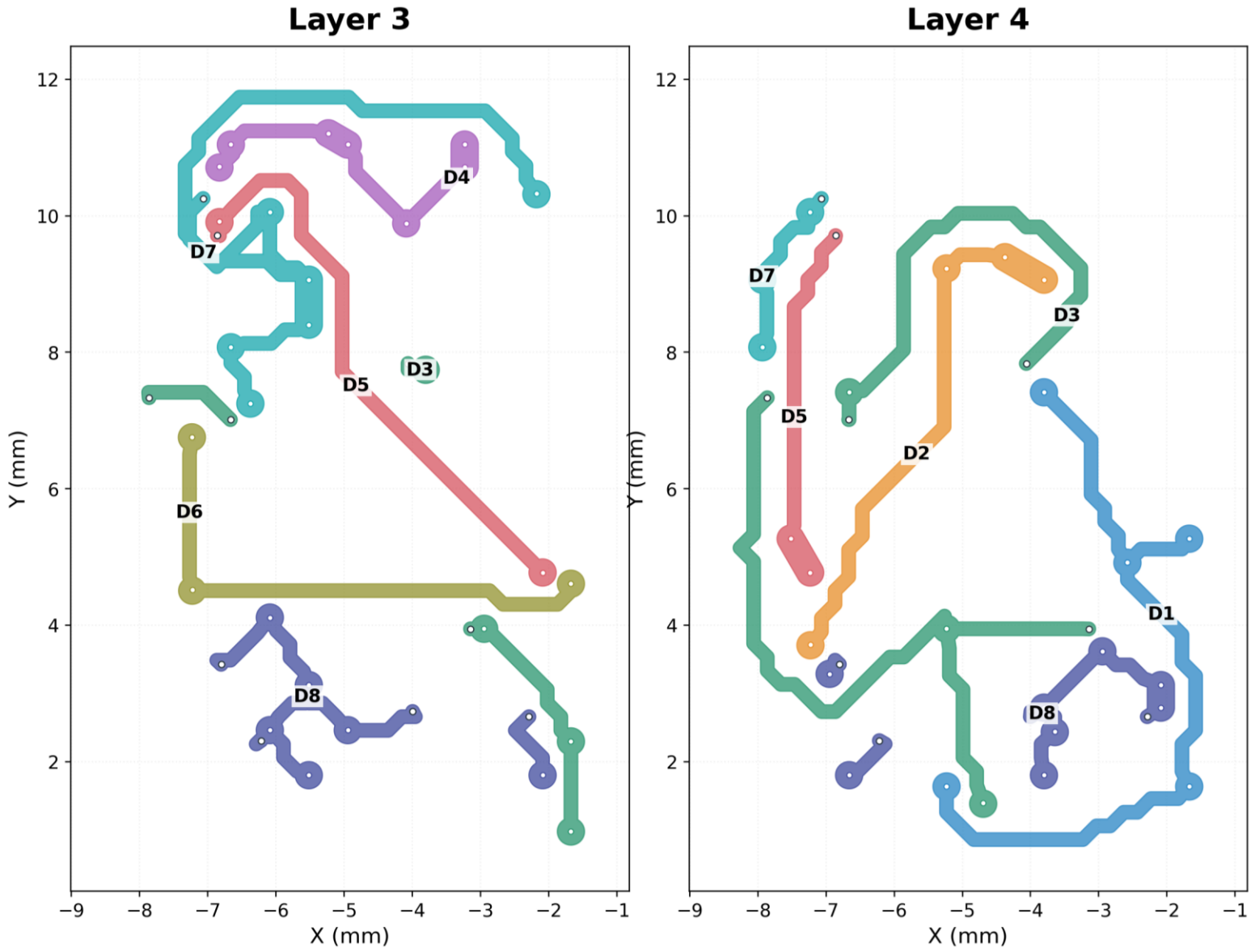
Copper area: 32.55 → 41.94 mm²

Physics-Guided Design: Soft Reservation





Physics-Guided Design: Vulnerability Analysis



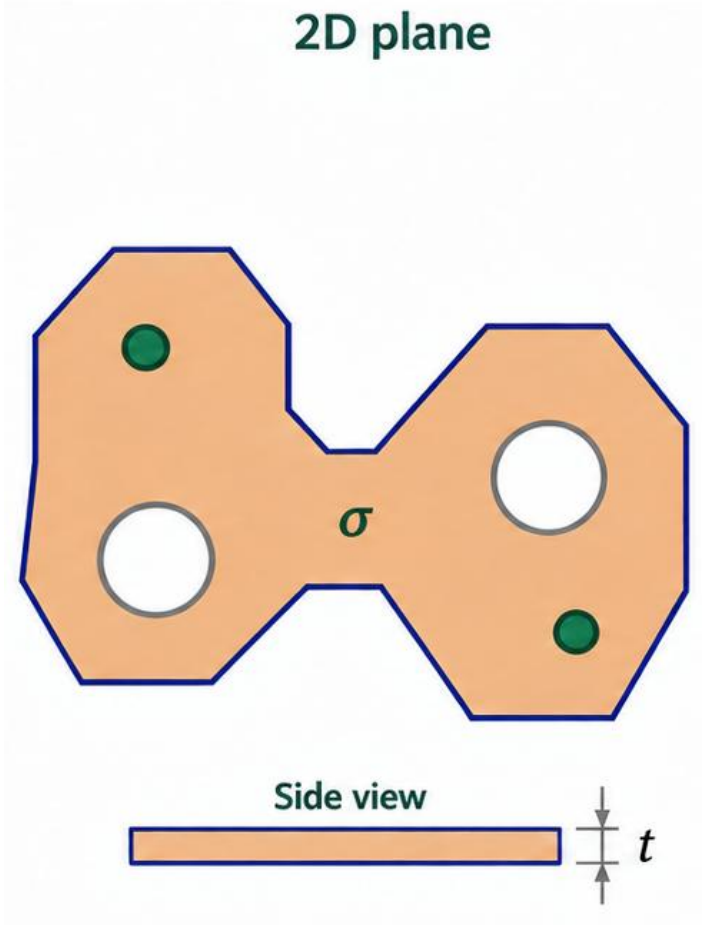
Vulnerability ranking

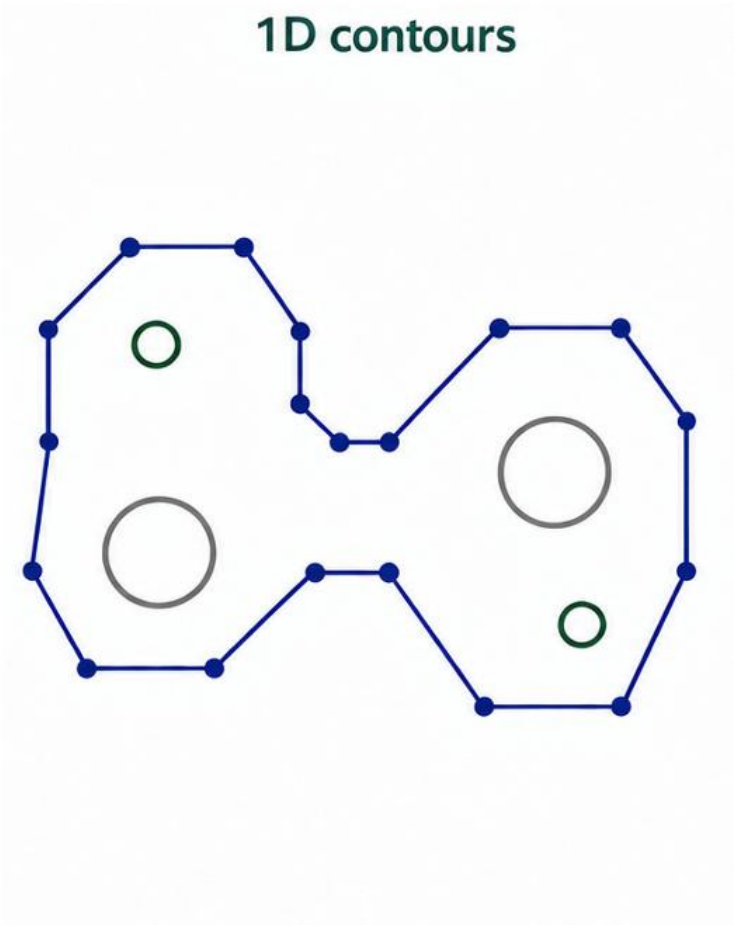
Rank	Domain	Score
1	**D4**	**0.1735**
2	D7	0.1569
3	D3	0.1532
4	D5	0.1340
5	D2	0.1331
6	D6	0.0884
7	D1	0.0554
8	D8	0.0000*

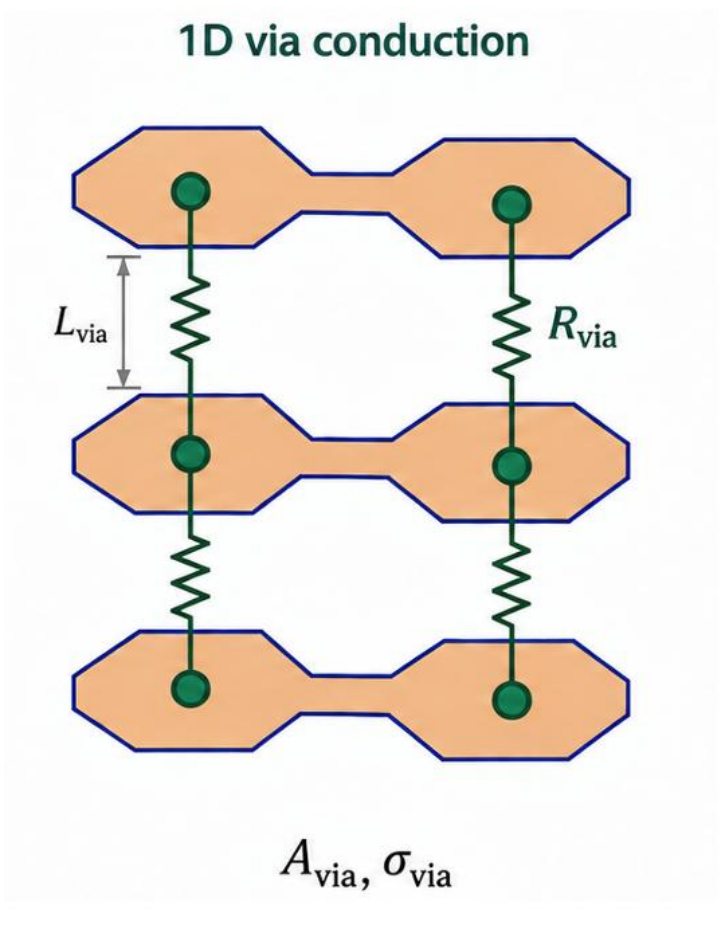
0–1 index
Higher = more constrained growth

* No failing paths to score

DCR Calculation using CIM

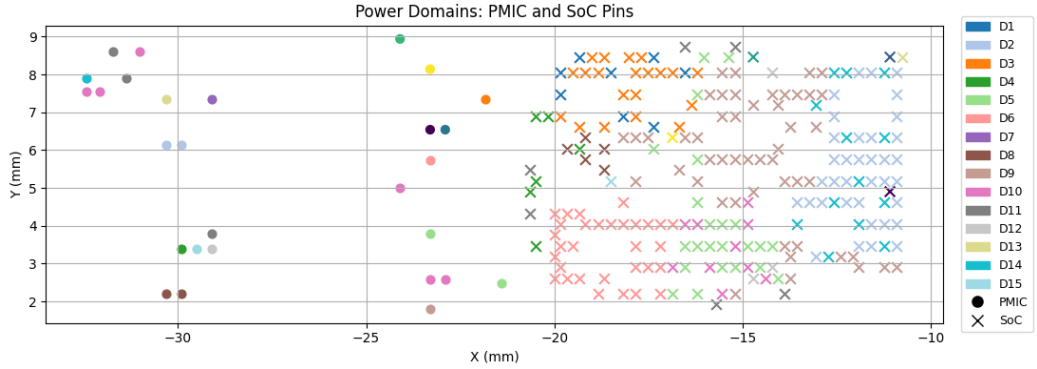




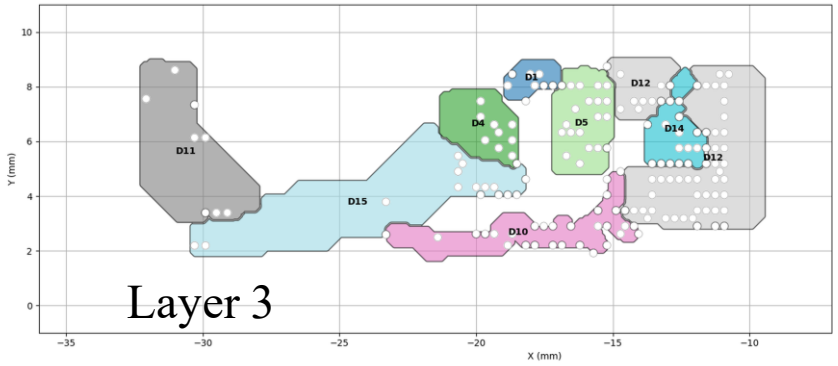


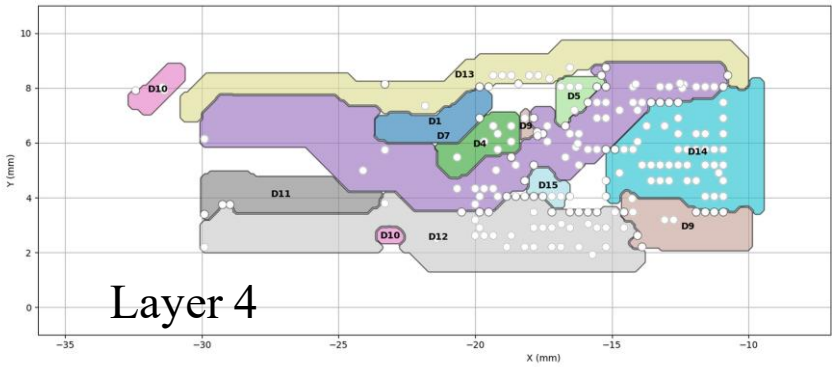
X. Duan, "Efficient DC Analysis of Power Planes Using Contour Integral Method With Circular Elements," IEEE T-CPMT, 2013
L. Zhang, "Efficient DC and AC Impedance Calculation for Arbitrary-Shape and Multilayer PDN Using Boundary Integration," IEEE T-SIPI 2022.

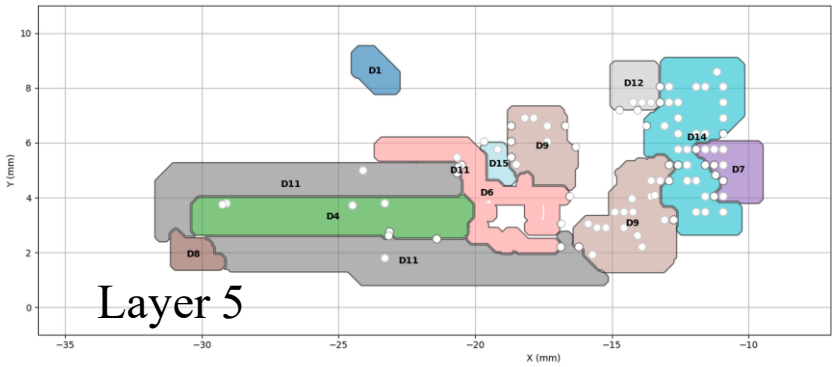
Example #1 – Wearable Device

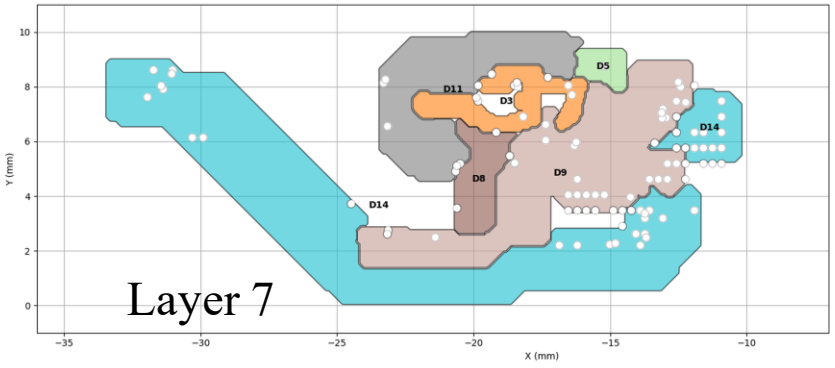


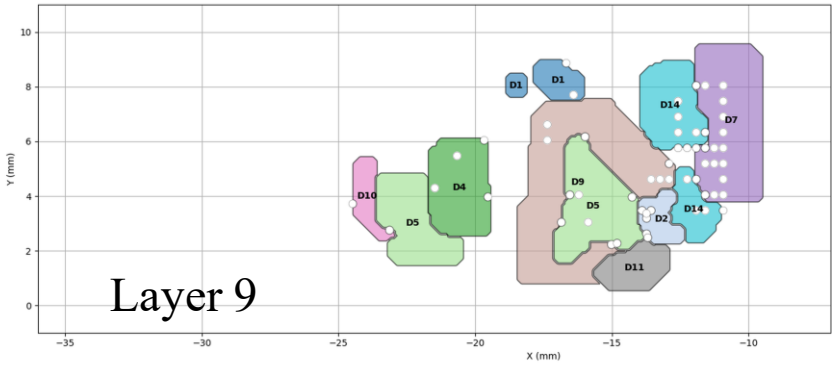
- # of available layers – 6
- # of power domains – 15
- PMIC – top layer
- SOC – top layer

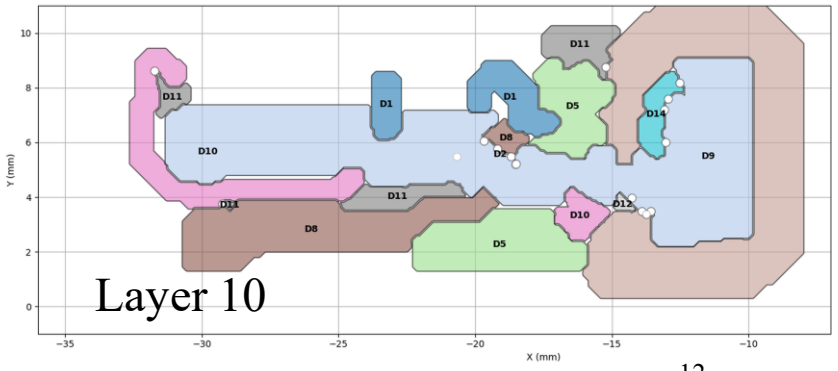




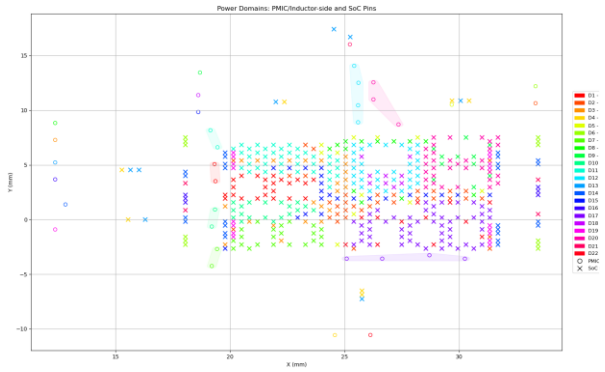




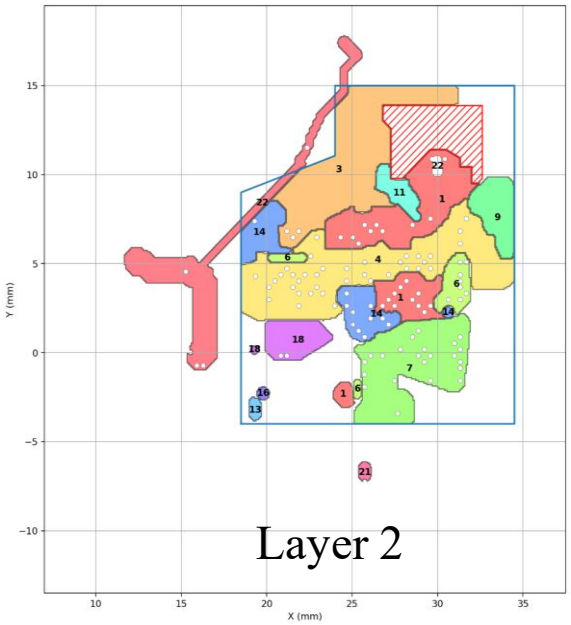


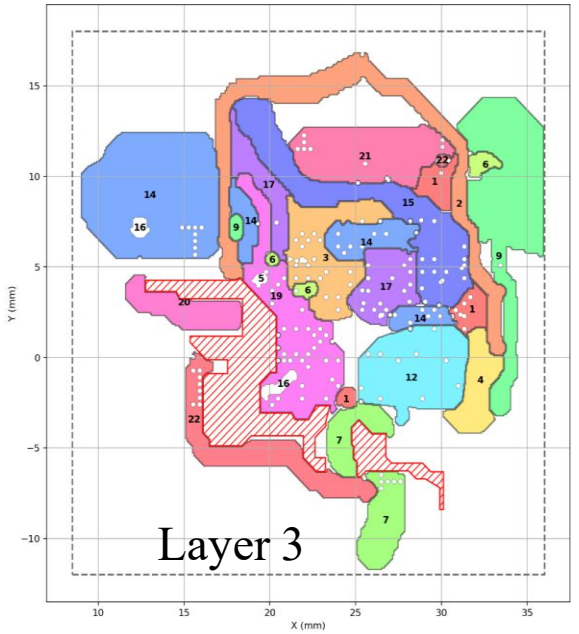


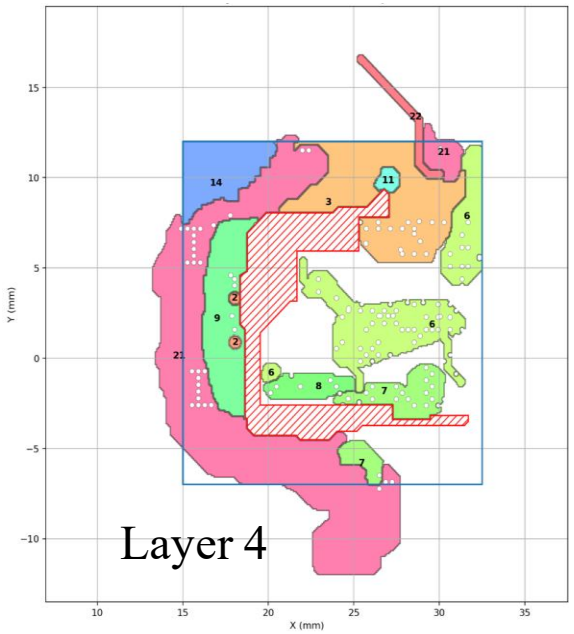
Example #2 – Mobile Device

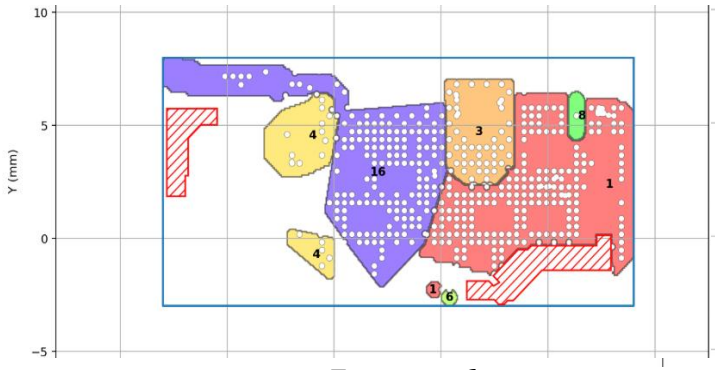


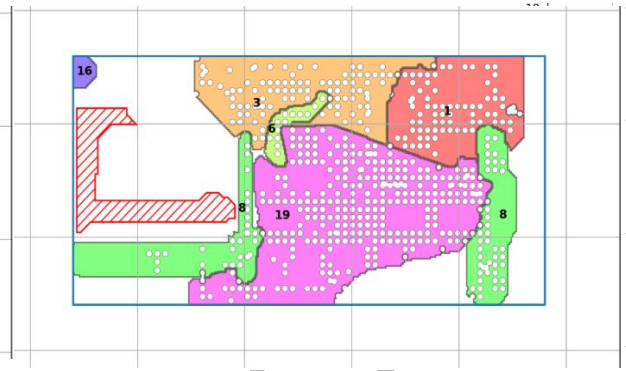
- # of available layers – 7
- # of power domains – 22
- PMIC – top layer
- SOC – top layer

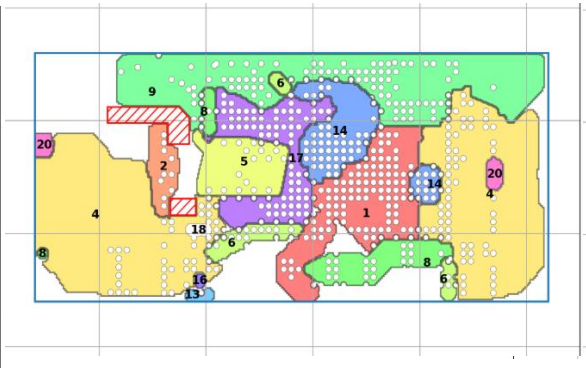

Layer 2

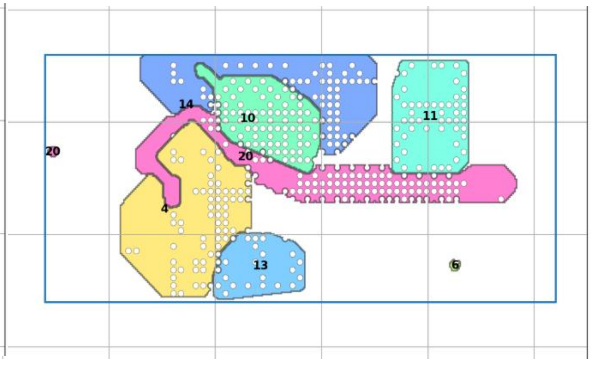

Layer 3


Layer 4


Layer 6

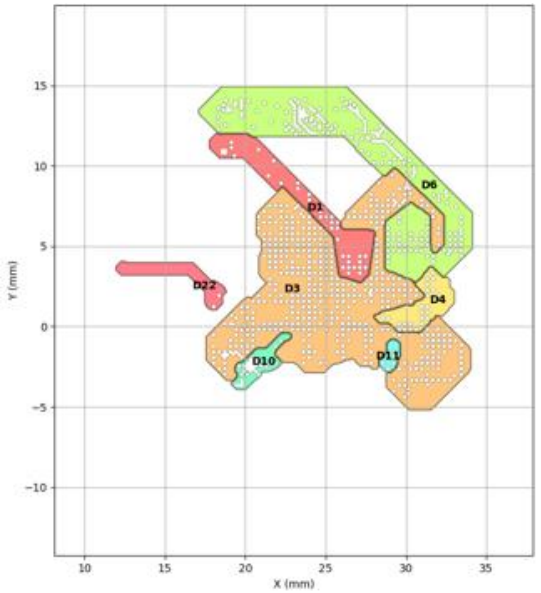

Layer 7


Layer 8

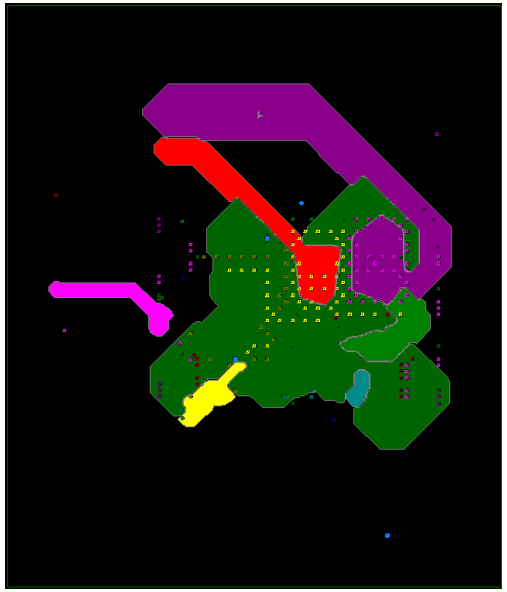

Layer 9

CAD Tool Compatibility

Python



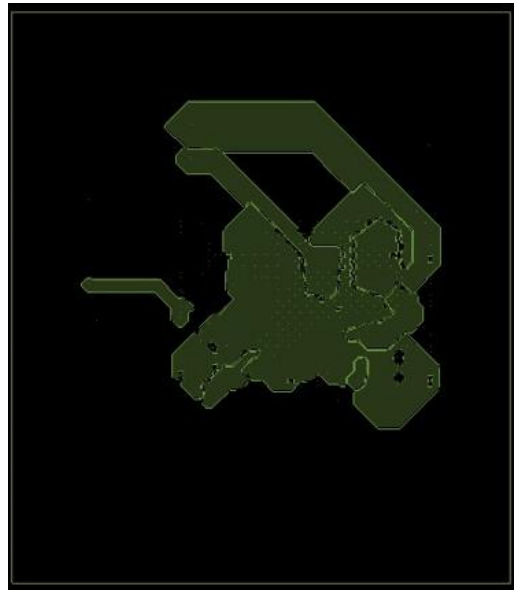
EDA Tool A



EDA Tool B



EDA Tool C



Decap Layout Generation (AC)

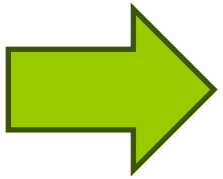
- Variable BOM case
- Fixed BOM case

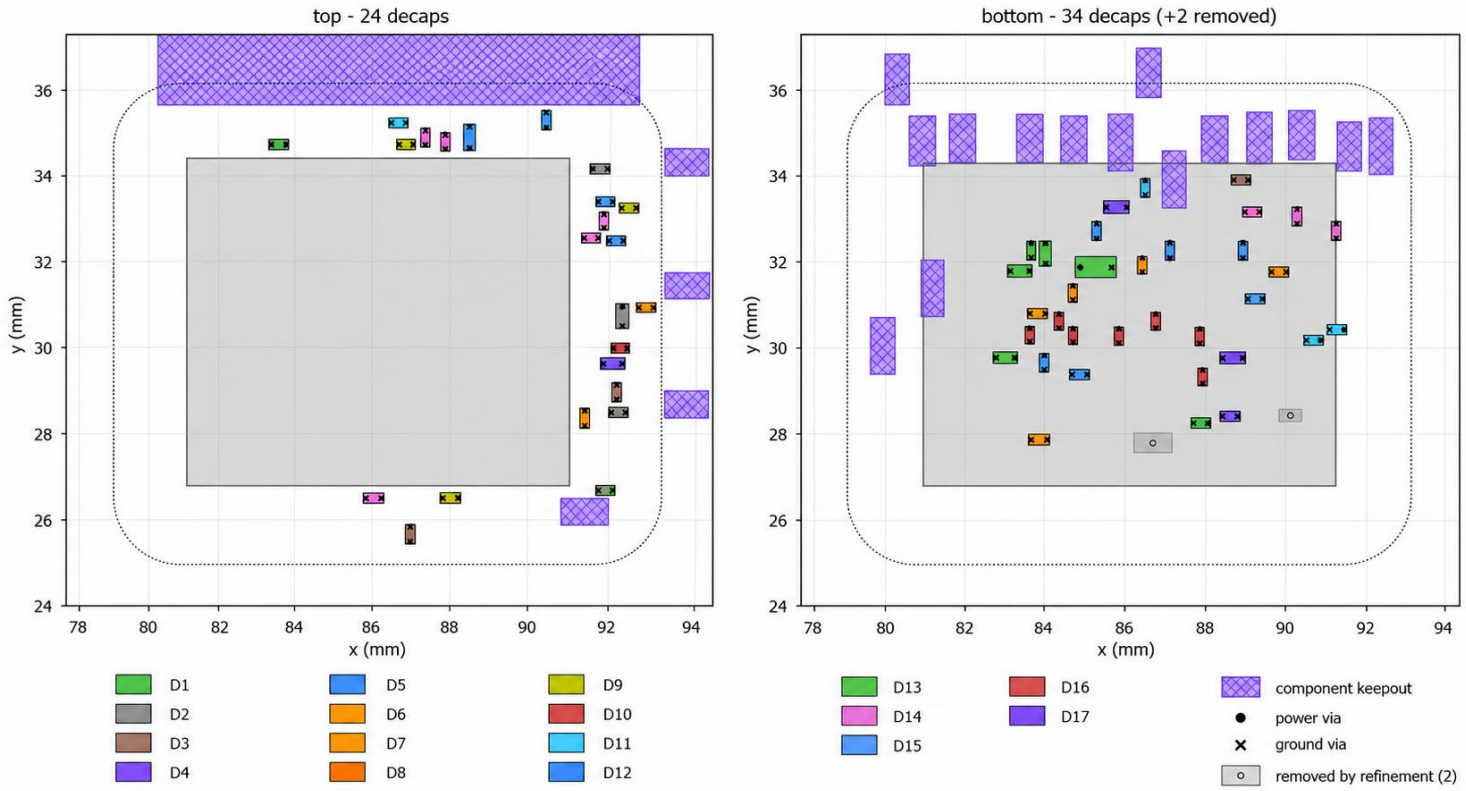
AC Design Generation without Fixed BOM

Objective: Place decaps from the library to meet all AC target impedances

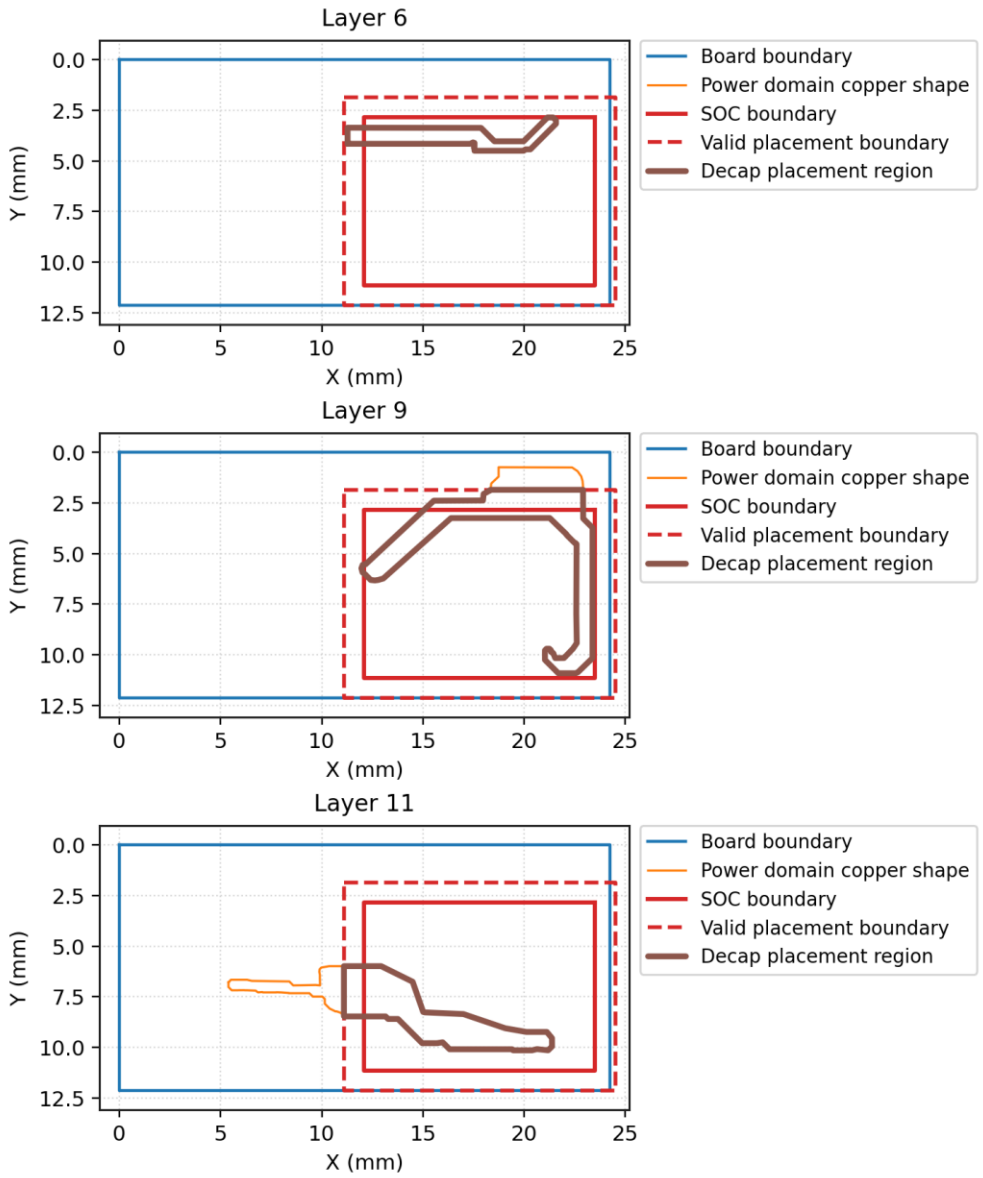
Decap Library



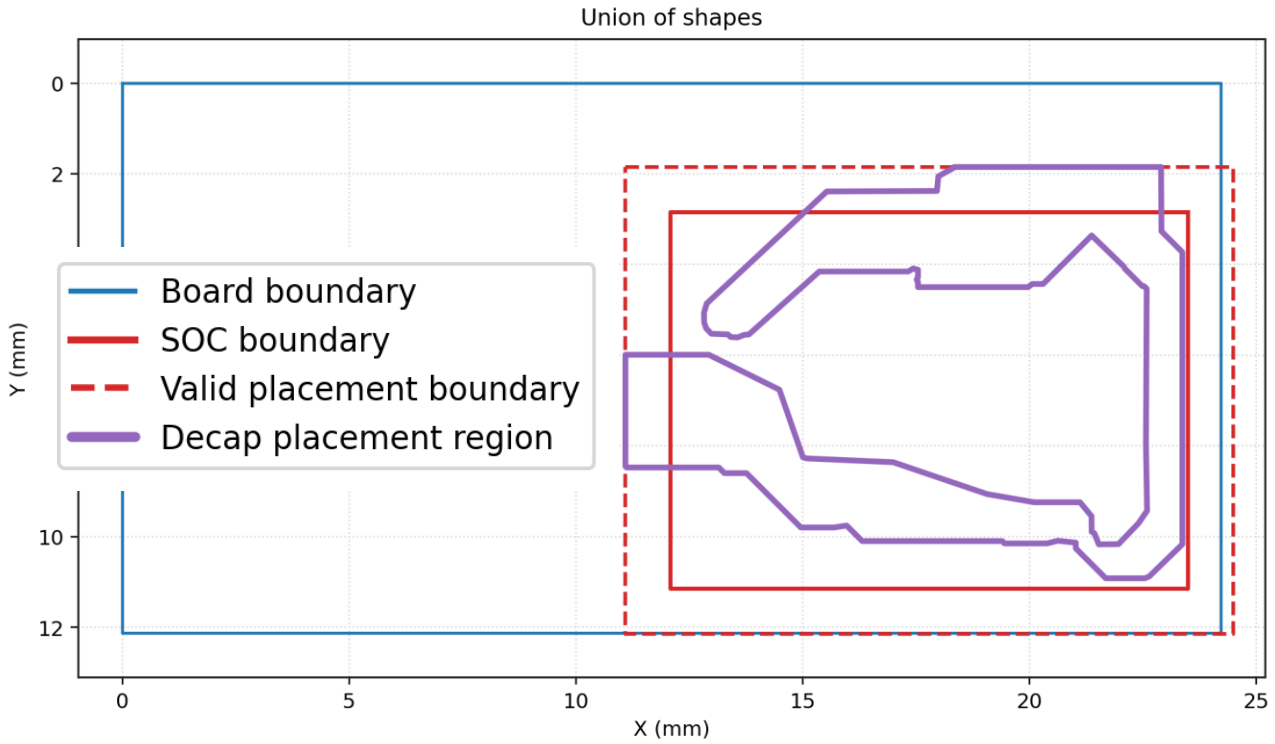




Generation of Boundary Valid for Placement

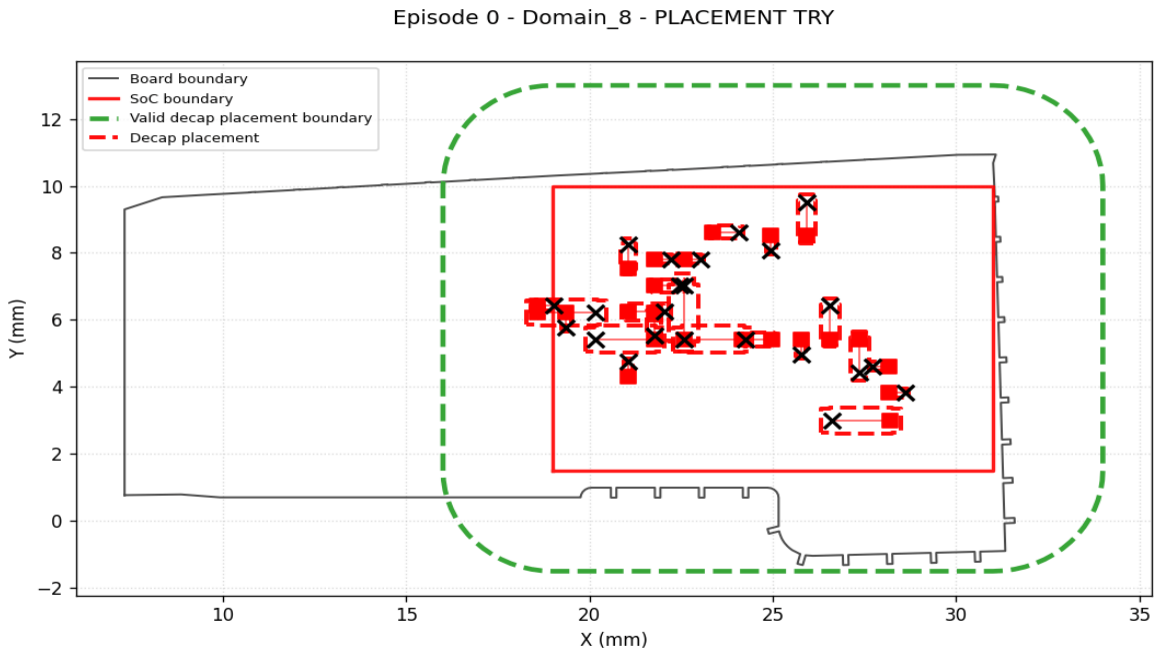


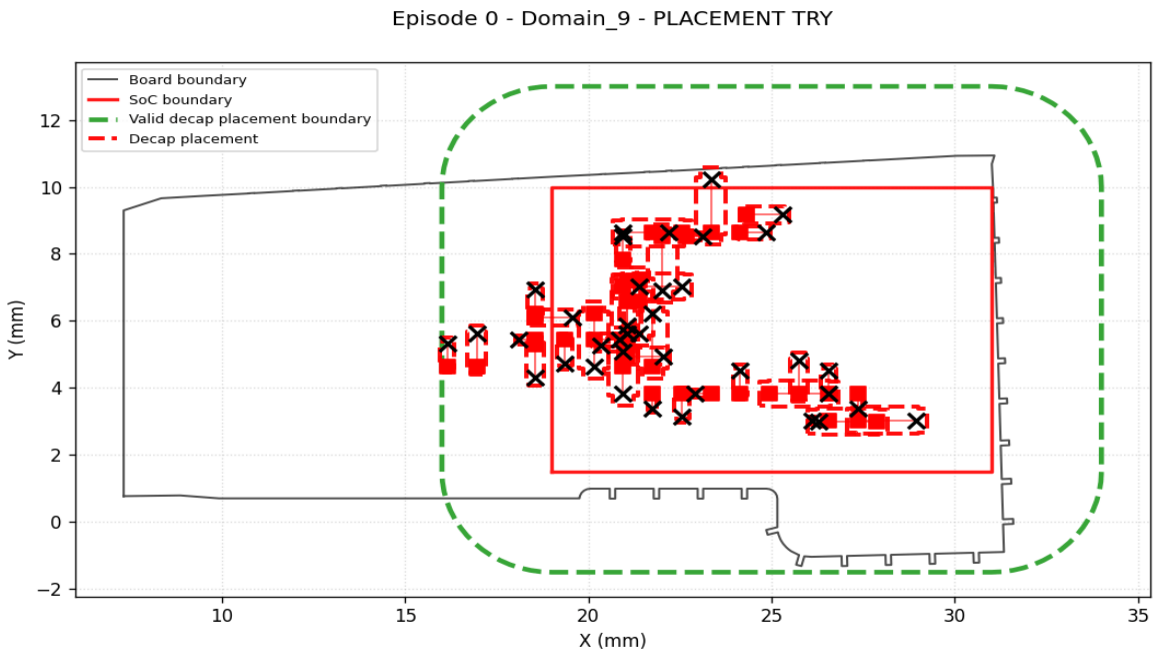




Decap Placement

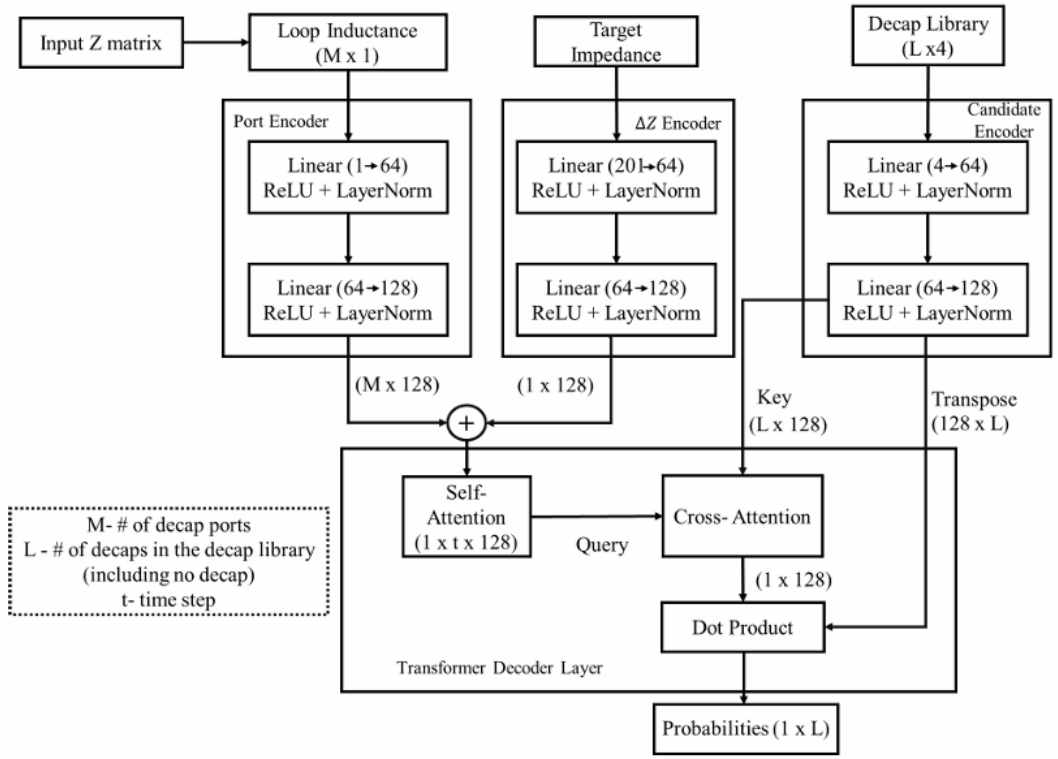
The agents makes decision on the decap package size, the layer (top or bottom) to place, and the orientation, and if or not to place decaps and tries to place the decaps without any physical violation

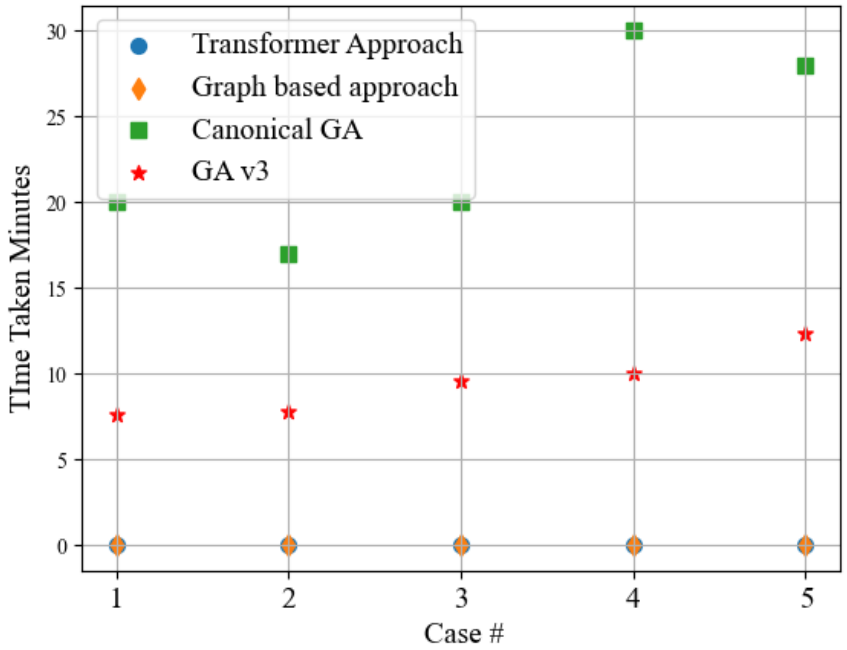


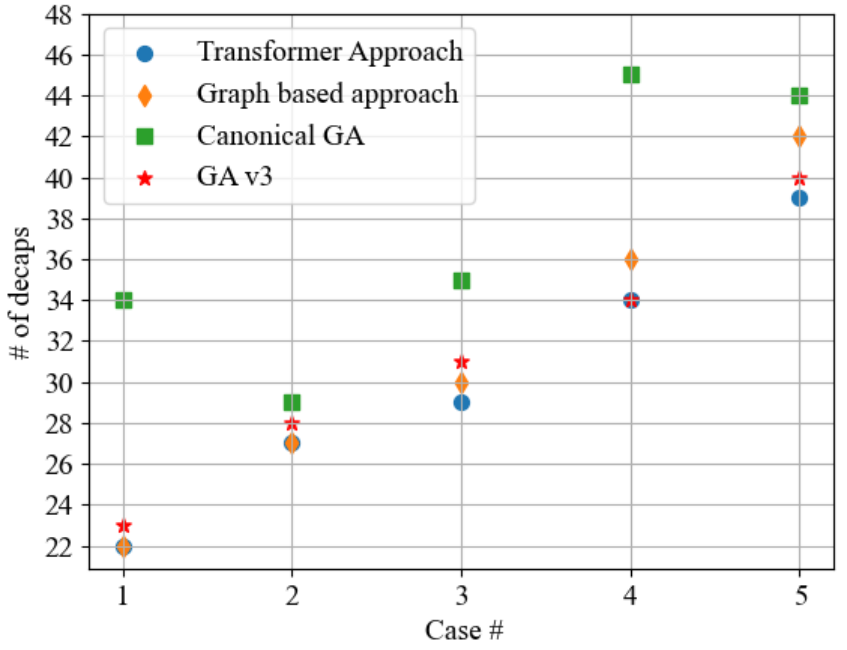


Decap Selection Optimizer

Transformed-based decap optimizer



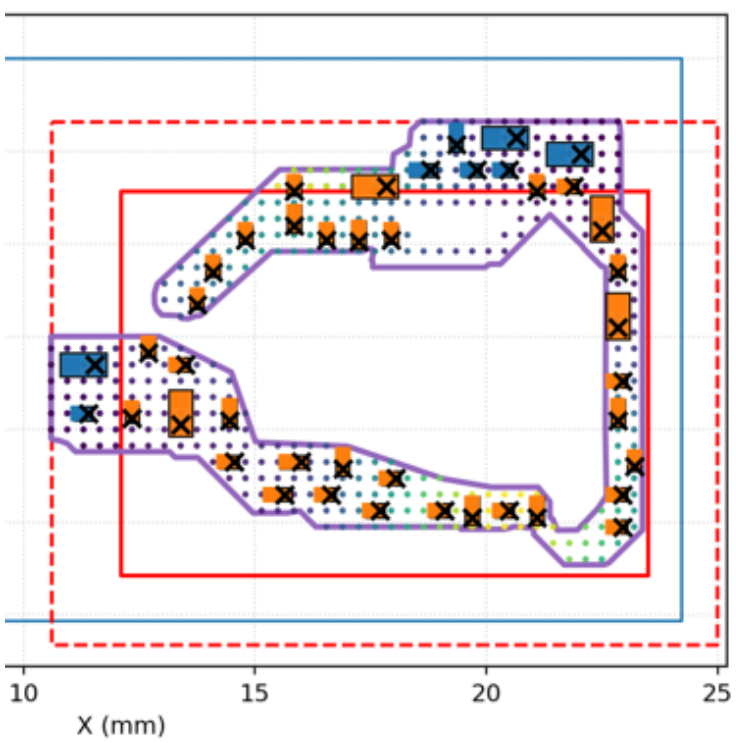




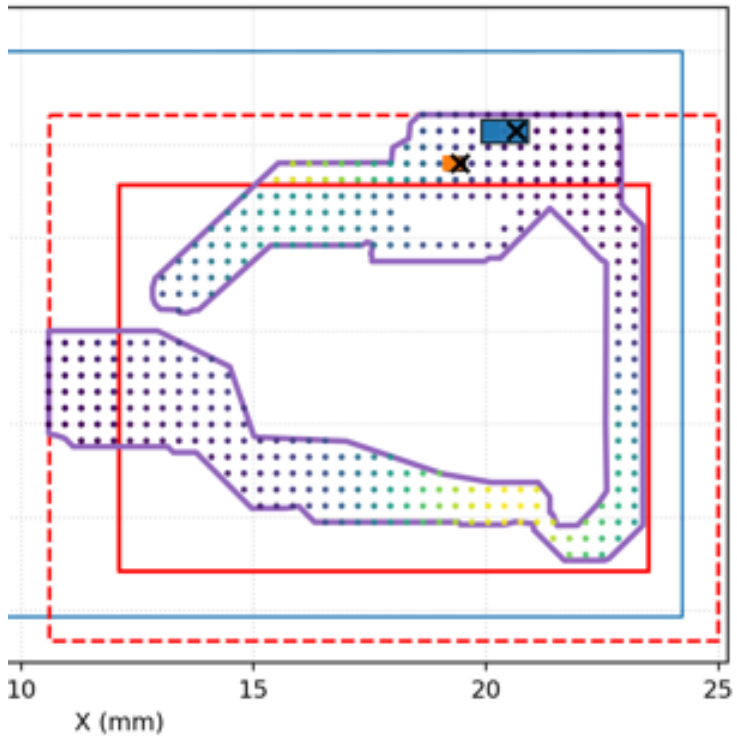
H. Manoharan, "Reinforcement Learning for Decoupling Capacitor Optimization in Postlayout PDNs Using Transformer Architecture," IEEE T-SIPI 2026.

Final Layout Generation

- After the decap values are chosen the unused caps are removed given the target is still met



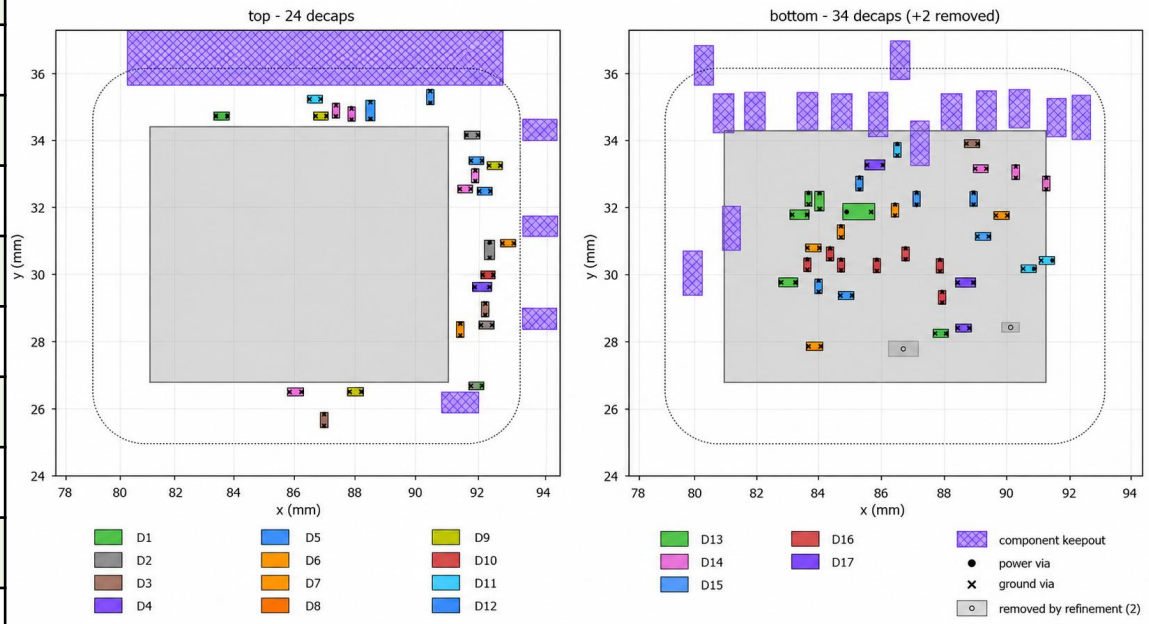
Physical violation passed



Selected decaps

Practical Example

Power Rail	Number of caps in Human design	Number of caps in Optimized design
Domain 1	8	5
Domain 2	2	1
Domain 3	7	5
Domain 4	3	2
Domain 5	10	7
Domain 6	8	5
Domain 7	3	2
Domain 8	5	3
Domain 9	7	8
Domain 10	5	4
Domain 11	8	6
Domain 12	3	2
Total	**69**	**50**

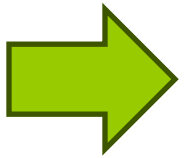


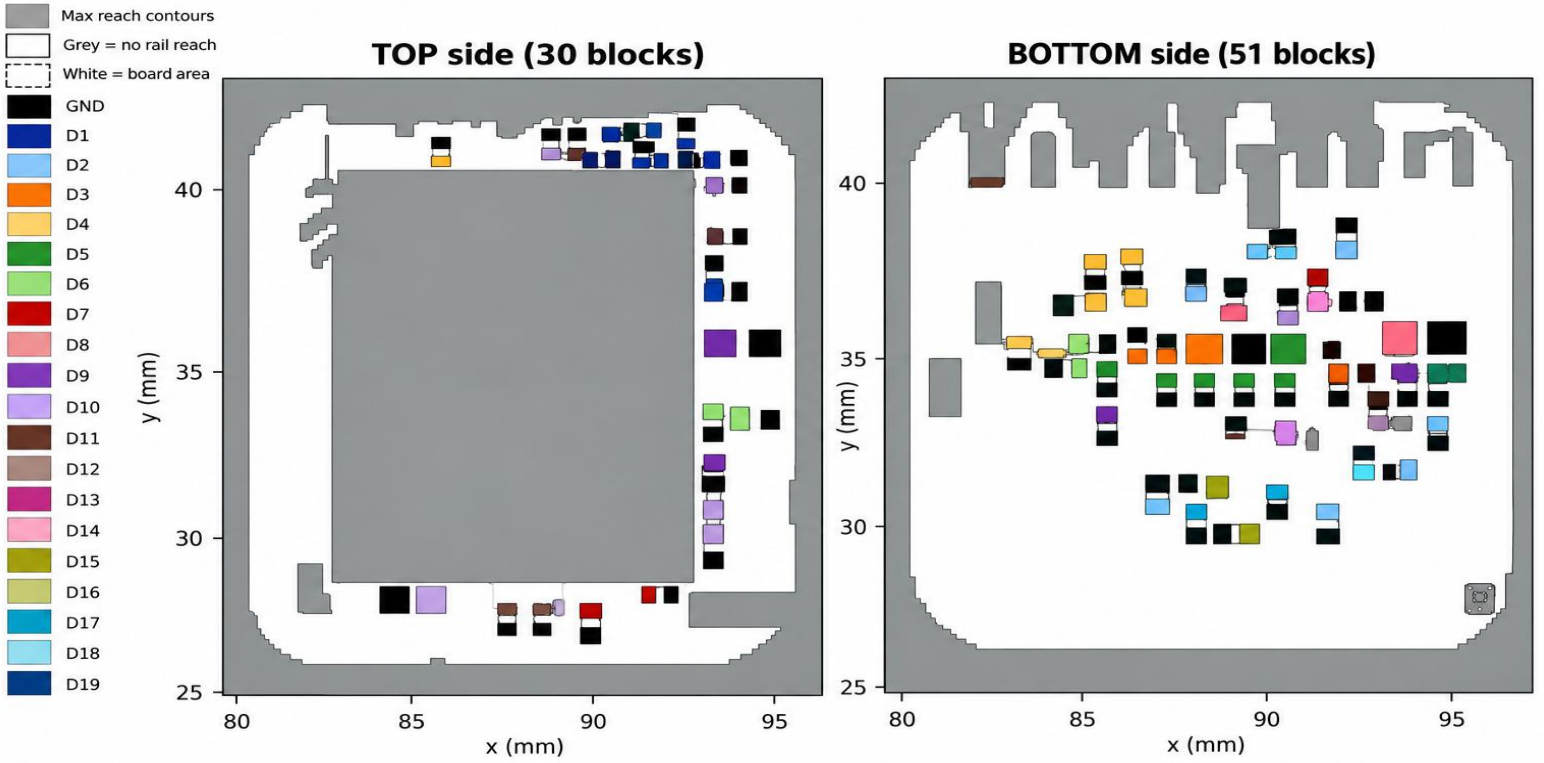
AC Design Generation with Fixed BOM

Objective: Place decaps in the BOM in the best possible locations on the board

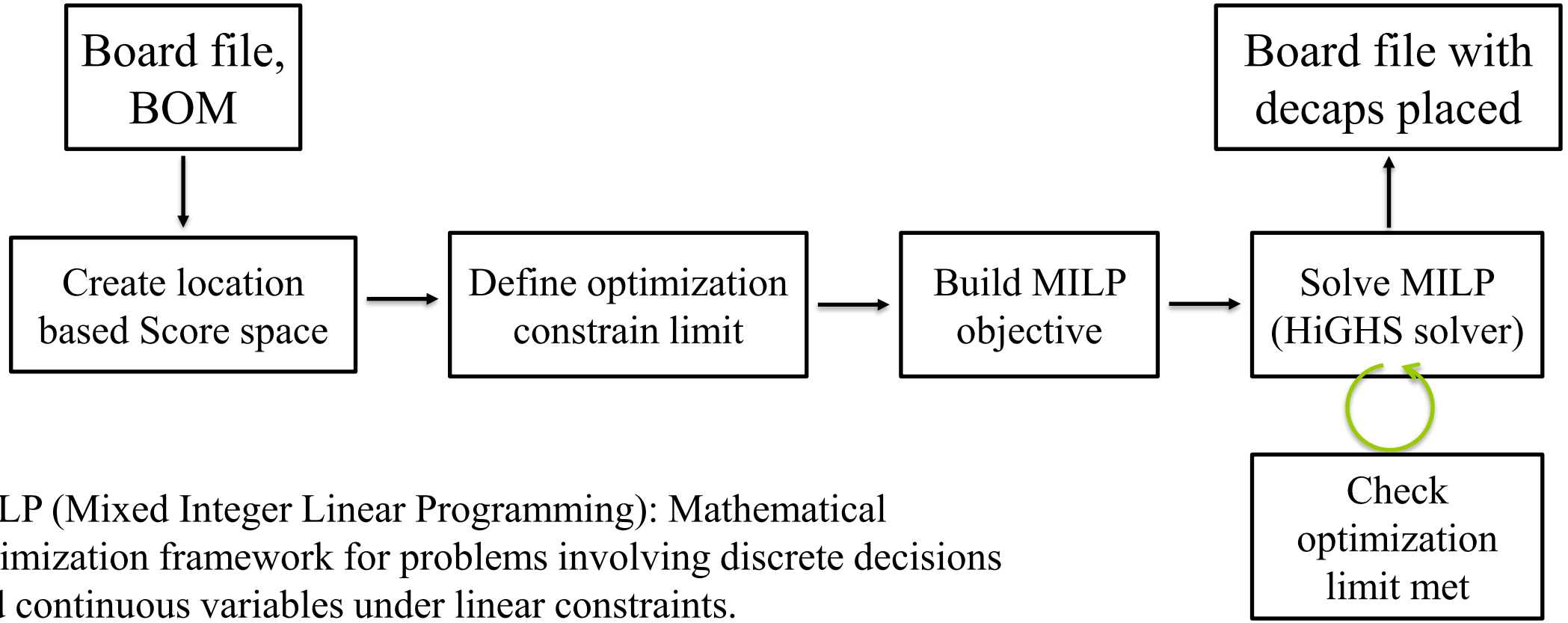
BOM







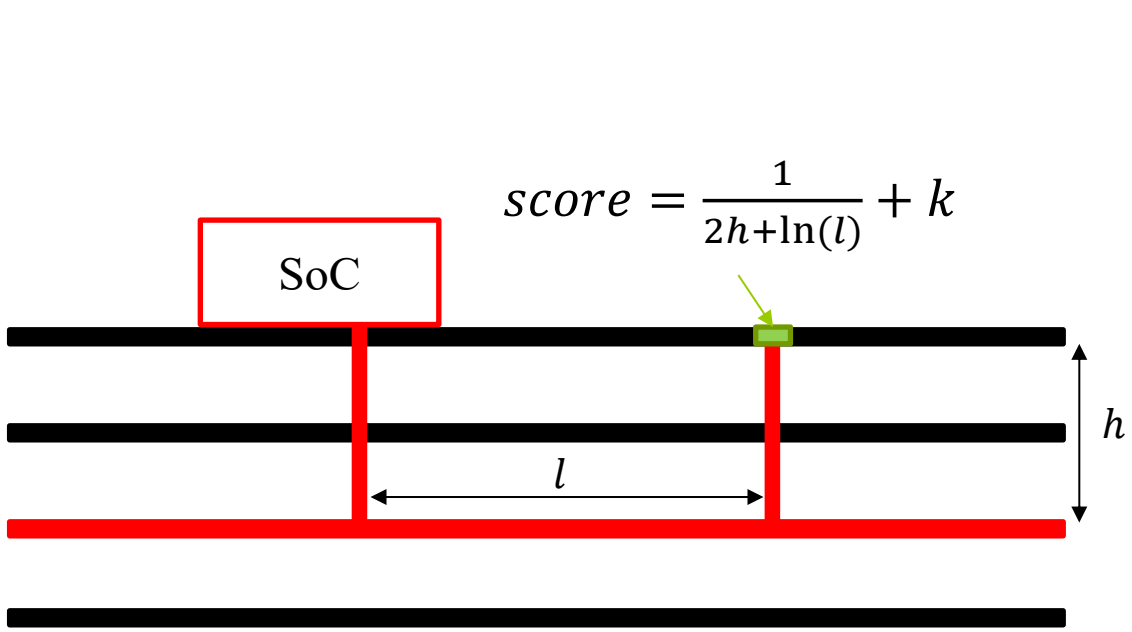
MILP Framework for AC Optimization

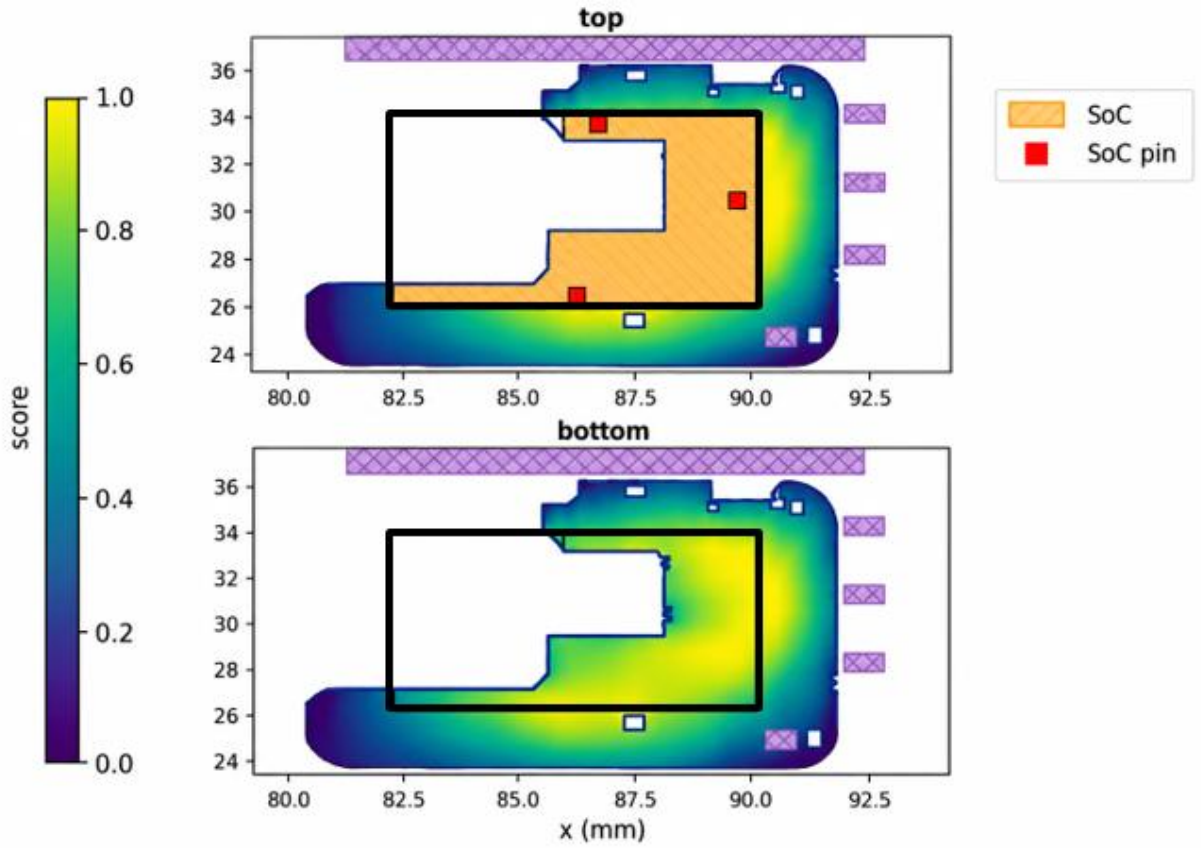


MILP (Mixed Integer Linear Programming): Mathematical optimization framework for problems involving discrete decisions and continuous variables under linear constraints.

The **underlying physics** must be expressed through **linear equations** or suitable linear approximations.

Score per Placement



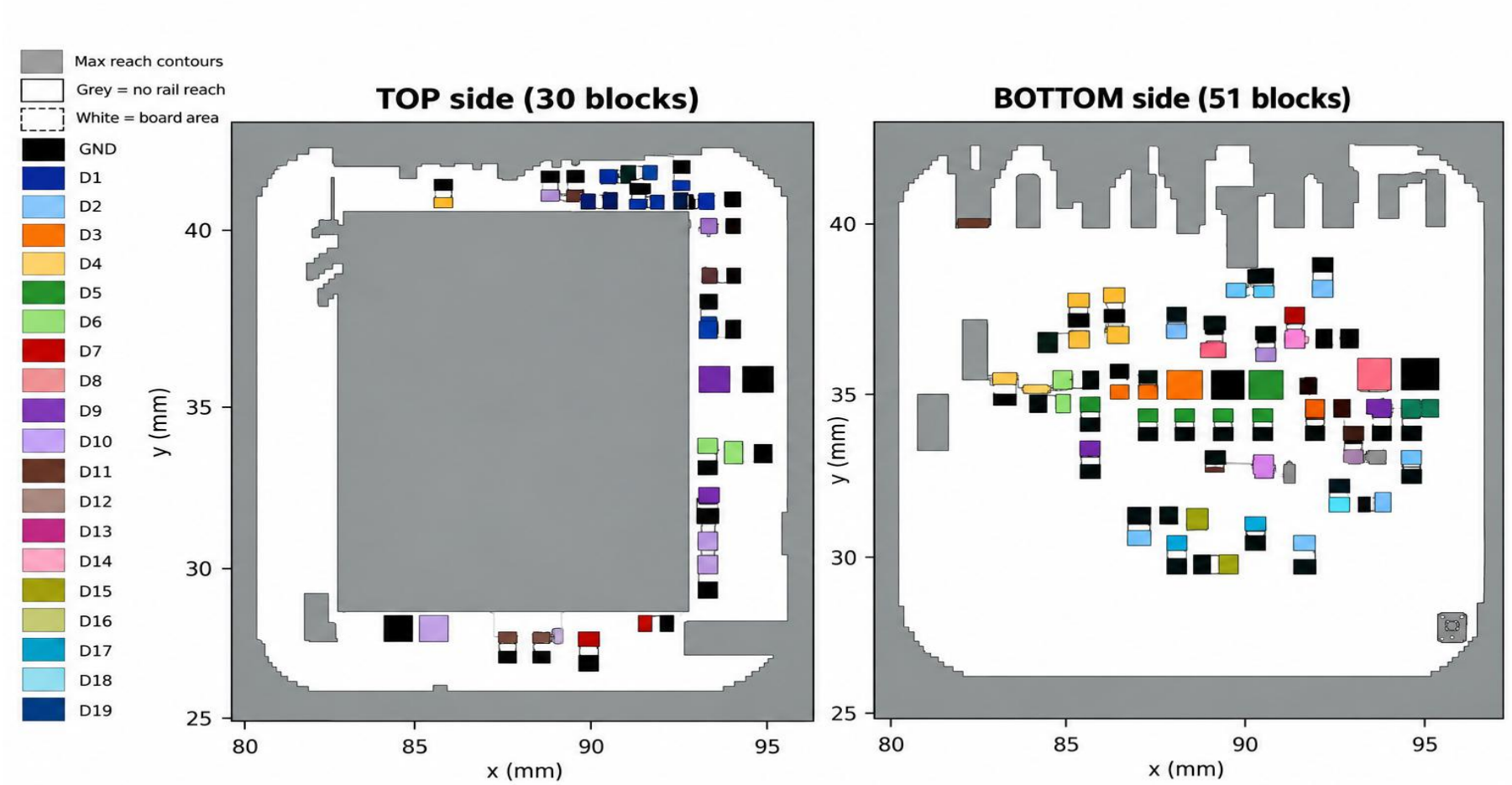


The valid copper region are discretized into small cells.

The cells of each rail is scored based on approximate inductance loop from SoC to decap

Practical Example

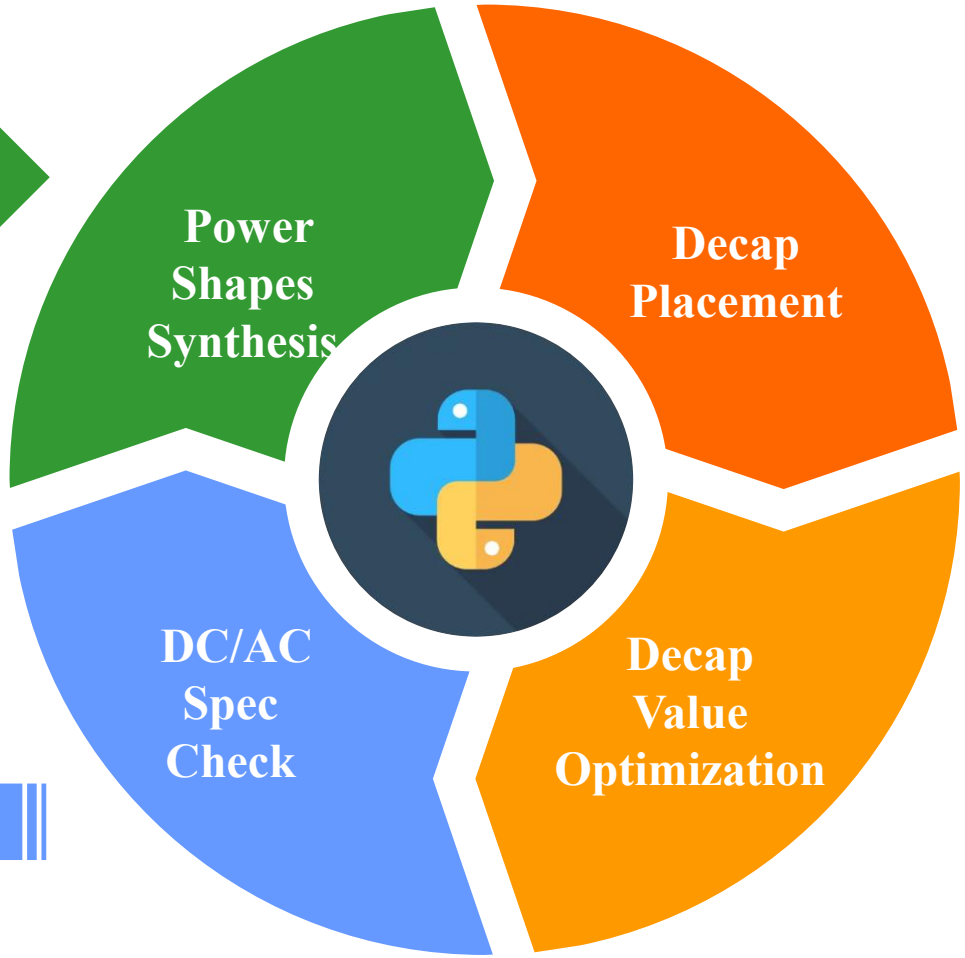
- A real board with 19 power domain with the fixed BOM
- Time: 130s



Next Step

Input

- Stack-up
- Pin map (Spreadsheet or layout file)
- Specs (DC/AC Target)



Output

- Full PDN Layout
- Decap placement (type & value)

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