WAI 2026 · HANGZHOU

2026 International Workshop
on Advanced Interconnects

AI-Assisted Signal Integrity Analysis and Optimization for High-Speed Links

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wai-emc.com/wai2026

OUTLINE

1. Background

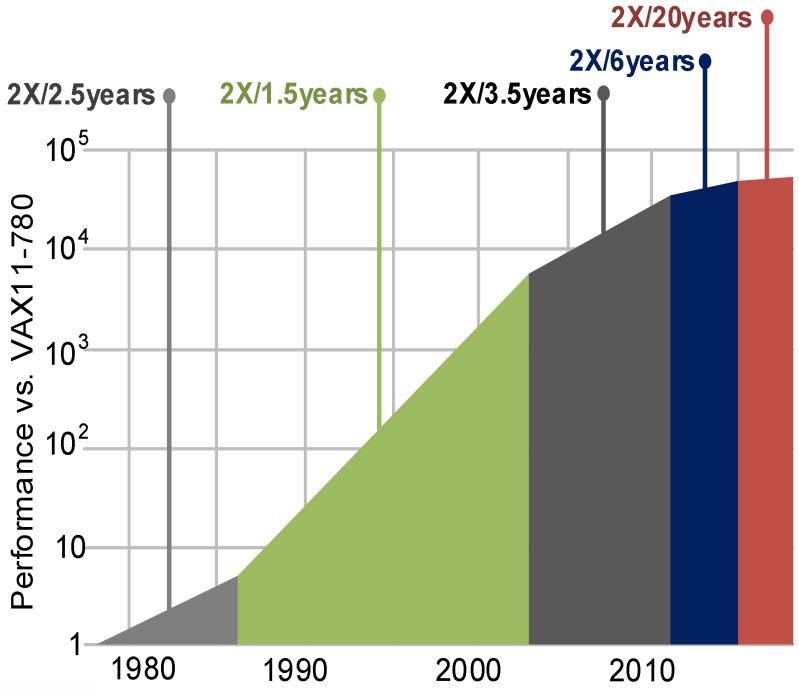
2. Surrogate modeling and analysis

3. Co-design optimization

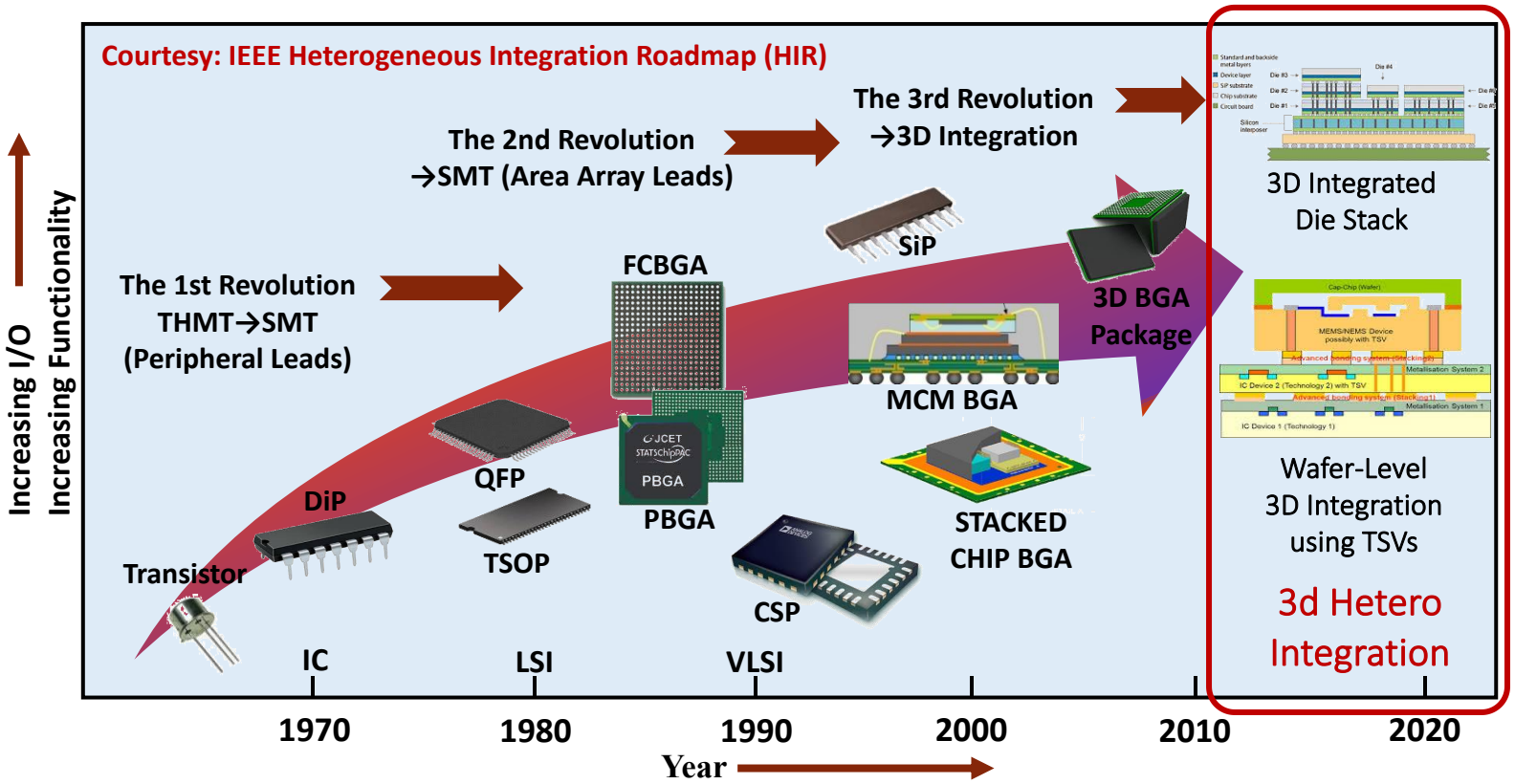
4. Conclusions

1 Technology Trends

- **Semiconductor tech nears physical limits, Moore's Law slows, IC industry struggles!**
- **3D stacking boosts chips density, a strategic path to solve China's IC bottleneck!**
  - **Cost & efficiency gains:** Use mature processes, skip advanced nodes, boost performance, lower costs.
  - **Flexible customization:** Application-driven with high flexibility and scalability for customization.

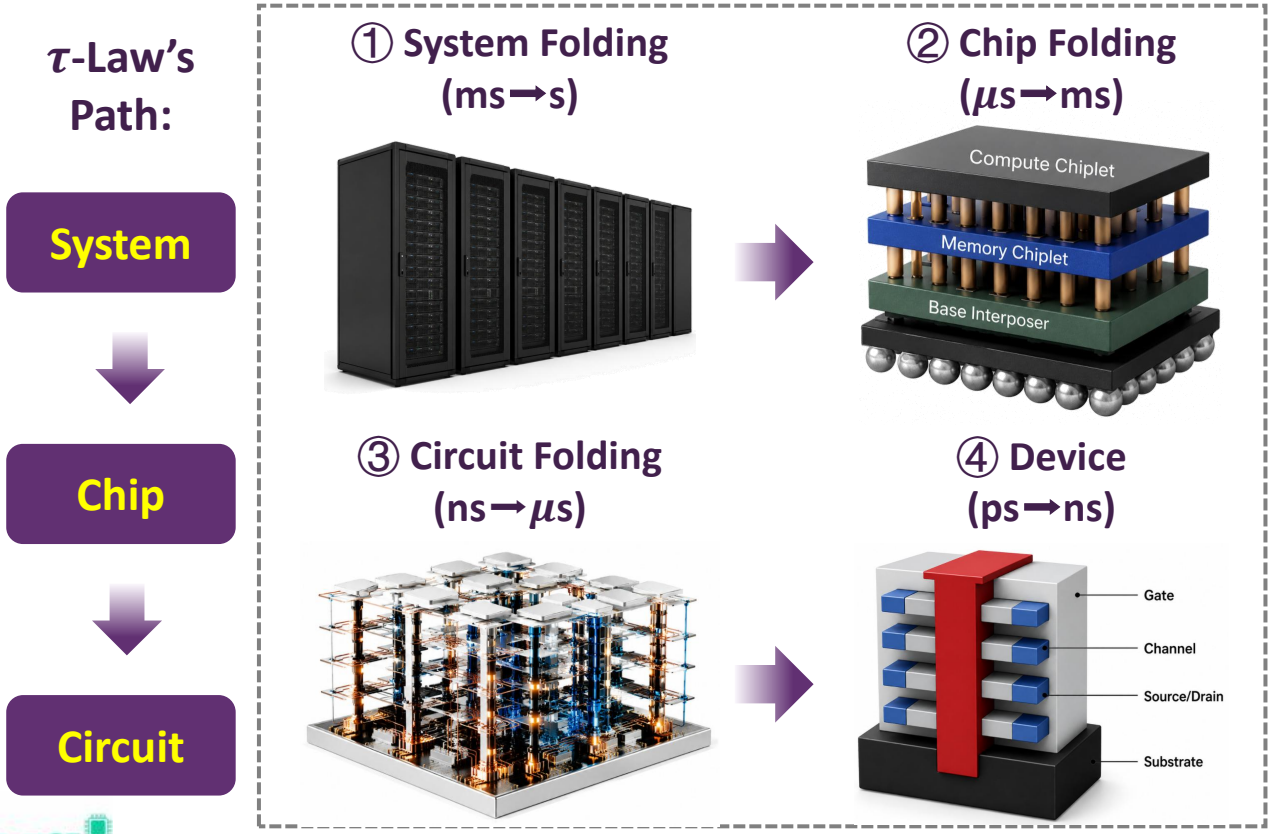


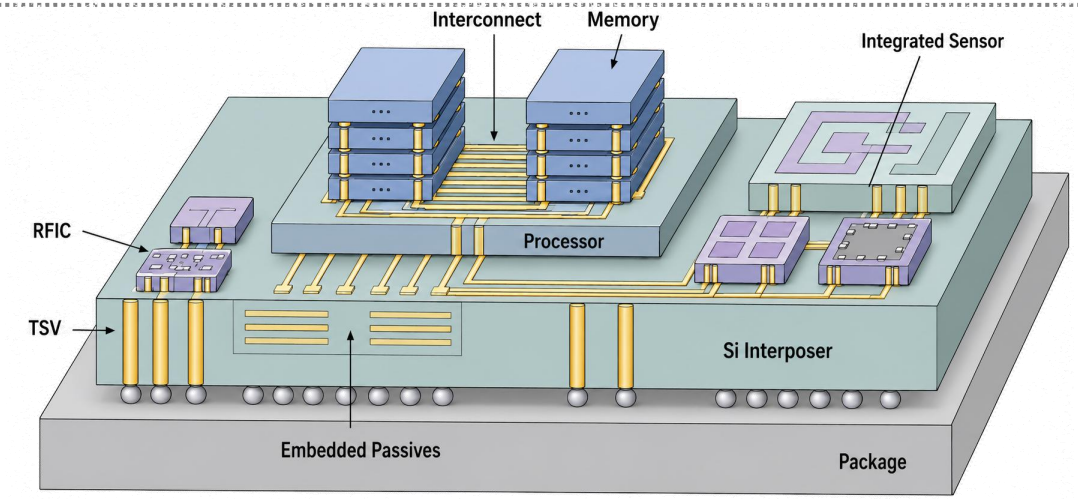
Slowing Moore's Law progress



1 Technology Trends

- 3D IC scaling shifts from transistor-level to interconnect/system-level optimization.
- Tau Law improves performance by reducing signal delay and interconnect cost.[1]
- TSV/die-stacking 3D ICs are evolving into a system-level integration platform.





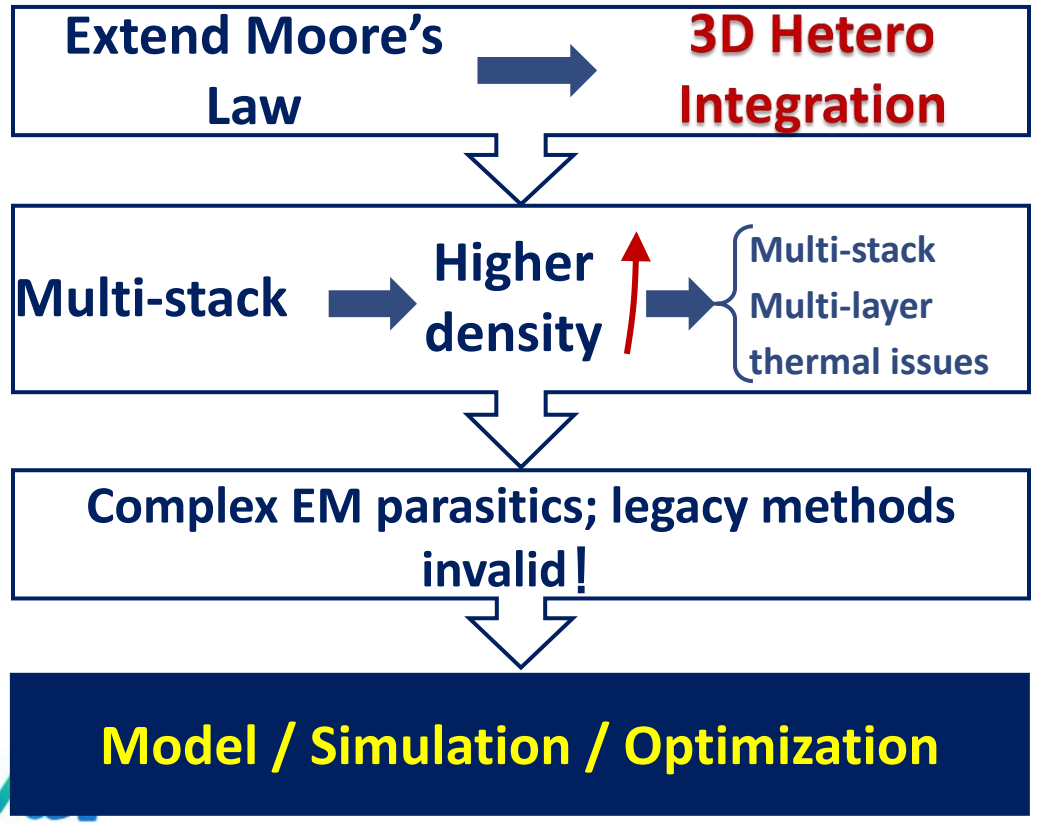
TSV Vertical Interconnect +
RDL Horizontal Redistribution

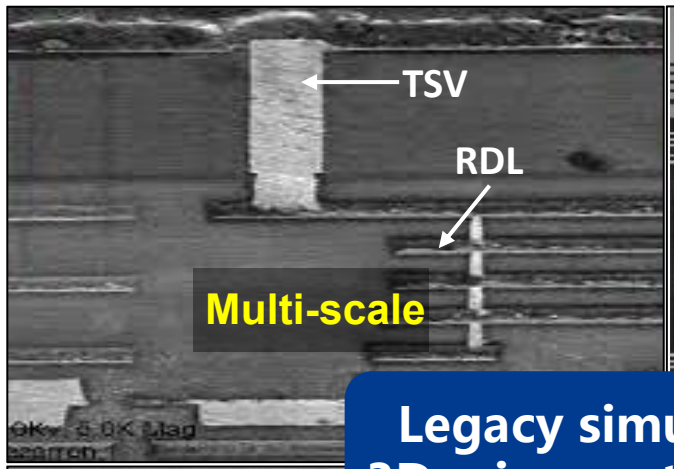
System-Level 3D IC

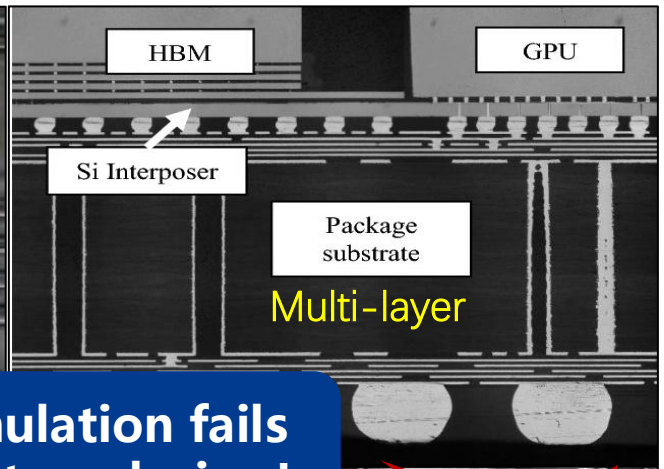
[1] Huawei's He Tingbo introduced the "Tau (τ) Law" during a keynote at IEEE ISCAS 2026, May 25, 2026. https://www.huawei.com/en/news/2026/5/ieee-iscas-tau-scaling

1 Challenges

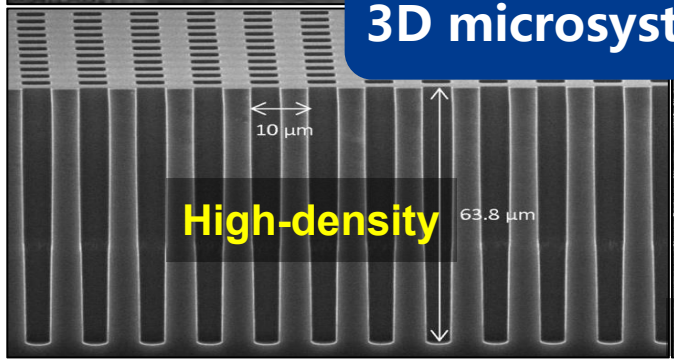
- **Higher 3D density raise complexity & heat, challenging microsystem simulation:**
  - **Model deficiency:** Conventional methods fail to capture 3D interconnect EM effects
  - **Simulation inefficiency:** Tools struggle with multi-scale coupled computation
  - **Optimization difficulty:** Standard techniques fail to meet 3D interconnect co-design

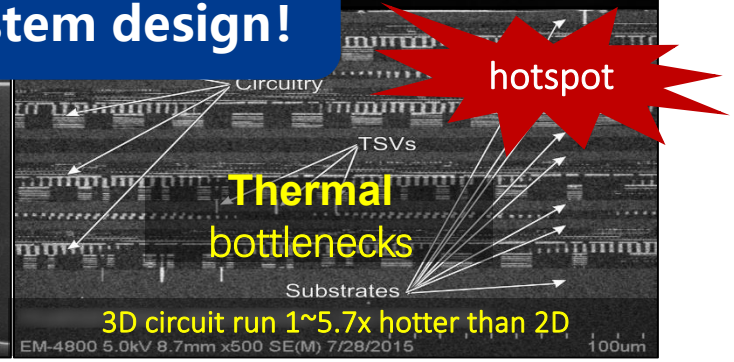






Legacy simulation fails 3D microsystem design!

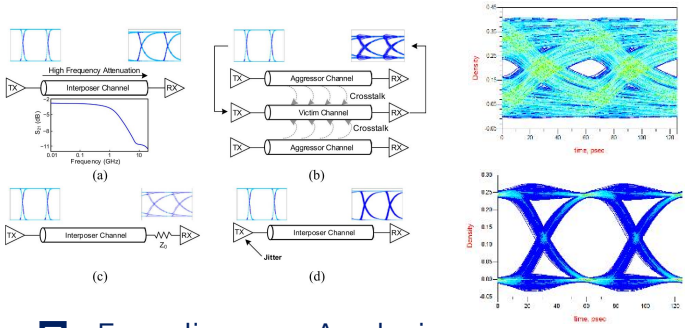




1 Challenges

- **Data-driven AI** speeds package performance prediction and design-space exploration.
- Existing methods still analyze **SI, PI, TI** separately, missing coupled physical feedback.
- **Multiphysics integrity** enables unified system-level co-design for advanced packages.

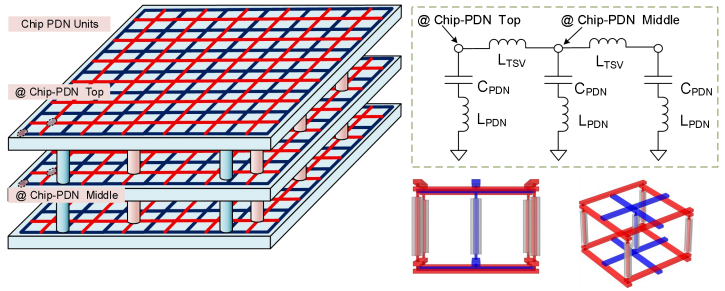
Signal Integrity



- Eye-diagram Analysis
- Waveform Modeling
- Impedance Matching

...

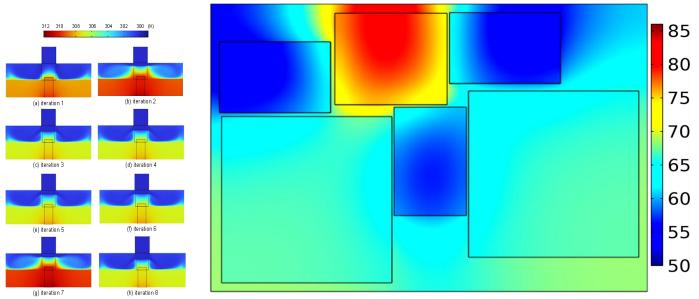
Power Integrity



- PDN Modeling
- Decap Optimization
- IR Drop Analysis

...

Thermal integrity



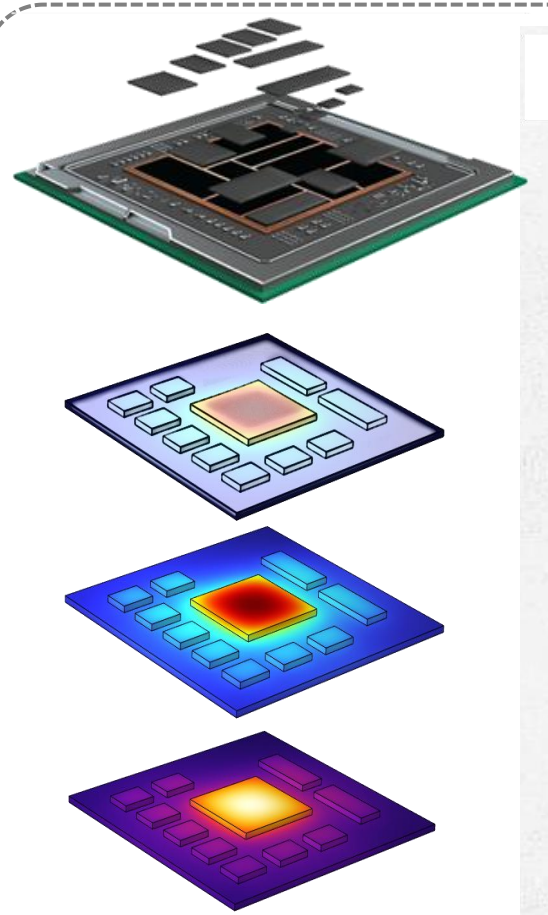
- Thermal Management
- Temperature Analysis
- Heat-Path Design

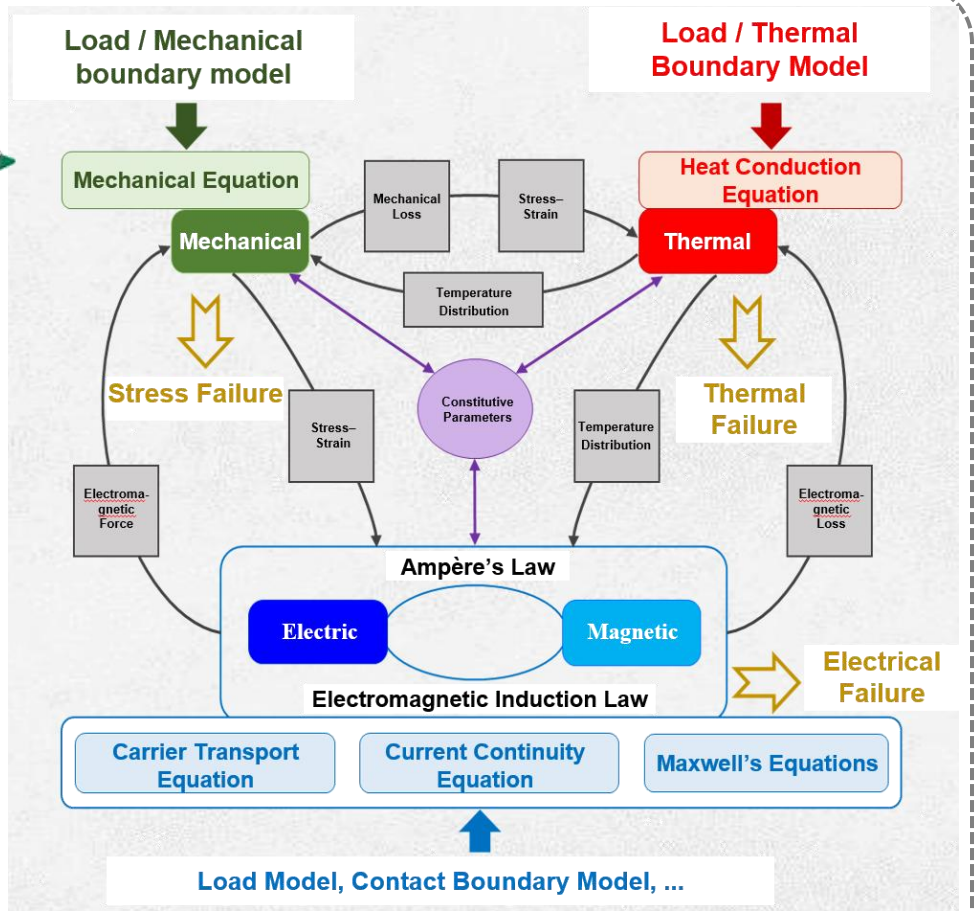
...

Isolated Integrity Analysis → **Missing Coupled Feedback** → **Multiphysics Integrity Analysis!**

1 Multiphysics integrity

- Multiphysics integrity： Ensure density heterogeneous 3D microsystems: stable electricity, controllable heat, reliable mechanics throughout lifecycle.





Electromagnetic Integrity

- Signal & Power Integrity: High density & lossy silicon cause severe delay, crosstalk and SSN.
- EMC: High-speed structures act as antennas, leading to serious EMC.

Thermal Integrity

- Thermal Management: Thermal stacking lengthens and complicates heat dissipation paths, while mismatched thermal expansion coefficients aggravate thermal stress.

Mechanical Integrity

- Reliability： Interfacial thermal mismatch creates thermomechanical stress. TSV stress modulates mobility via piezoresistive effect, harming system stability.

"Whole exceeds the sum of parts"：
Coupled multiphysics need co-optimization!

Multiphysics integrity is typical system engineering!

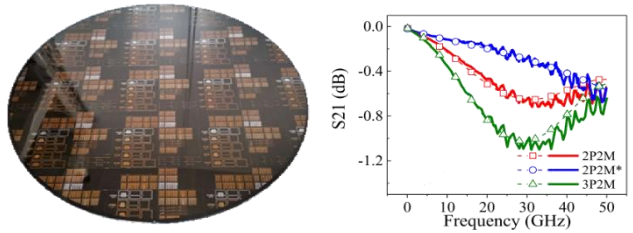
1 Research Framework

- Solve microsystem multi-physics & signal integrity issues via cross-disciplinary electromagnetics, math and AI for modeling-simulation-optimization pipelines.

model deficiency	Simulation inefficiency	Optimization difficulty

① Device Modeling

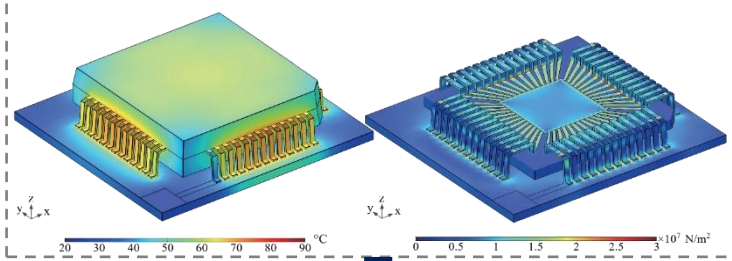
- Device equivalent topo optimization
- Wideband Precise Modeling
- Multi-objective surrogate optimization



- ✓ Interconnect framework built
- ✓ Efficient EM computation
- ✓ Wideband models developed

② Multi-physics Sim.

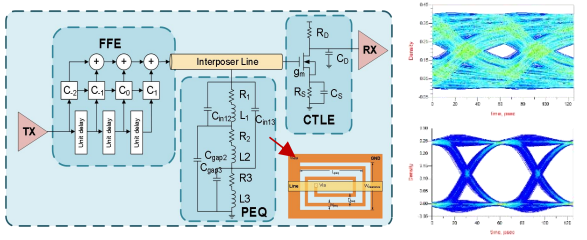
- Multi-physics high-fidelity modeling
- Multi-scale hybrid numerical algorithm
- Model reduction & digital twin



- ✓ FVM-FEM hybrid framework
- ✓ Chiplet IP multi-physics models
- ✓ Multi-physics simulator prototype

③ Anal. & Opt.

- Intelligent eye diagram evaluation
- Cm noise filter optimization
- High-dimensional co-optimization



- ✓ AI-assisted SI optimization
- ✓ Eye diagram enhancement
- ✓ Multi-objective optimization

OUTLINE

1. Background

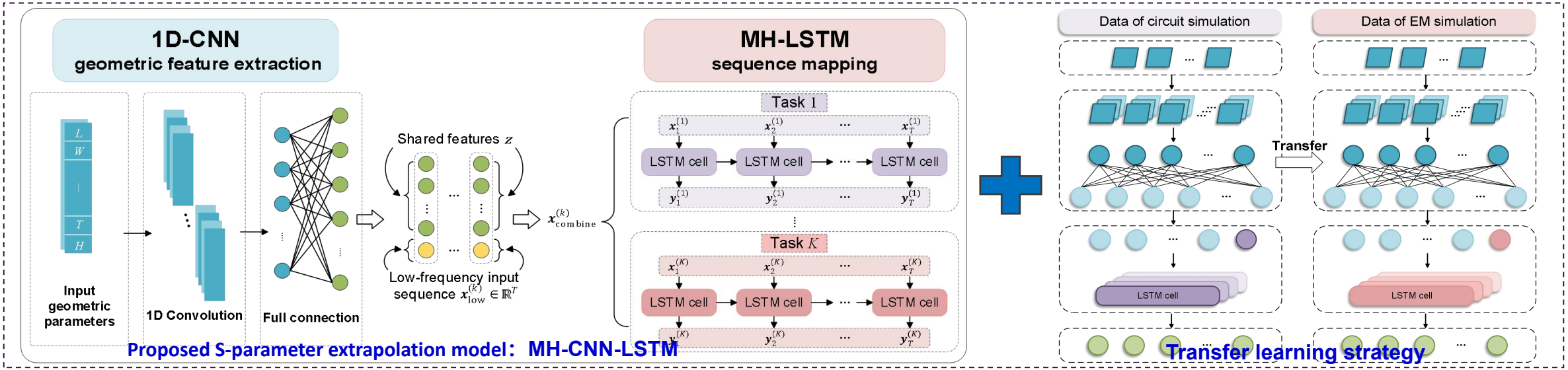
2. Surrogate modeling and analysis

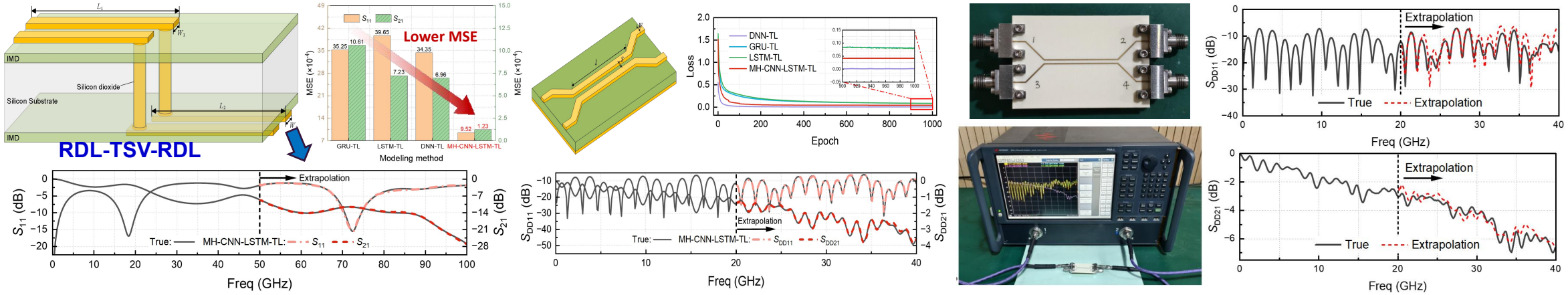
3. Co-design optimization

4. Conclusions

2 Broadband S-Parameter Extrapolation Method

- Machine learning-based nonlinear mapping enables accurate S-parameter extrapolation from low to high frequencies, effectively overcoming limitations in high-speed circuit.

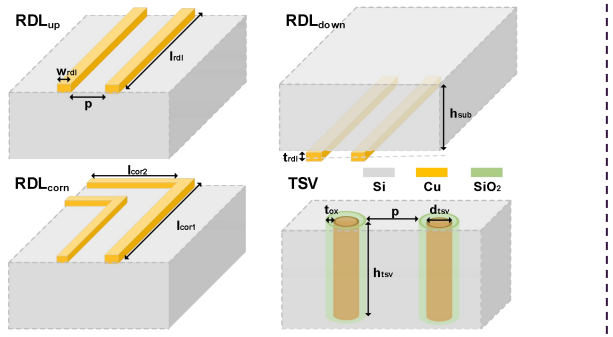




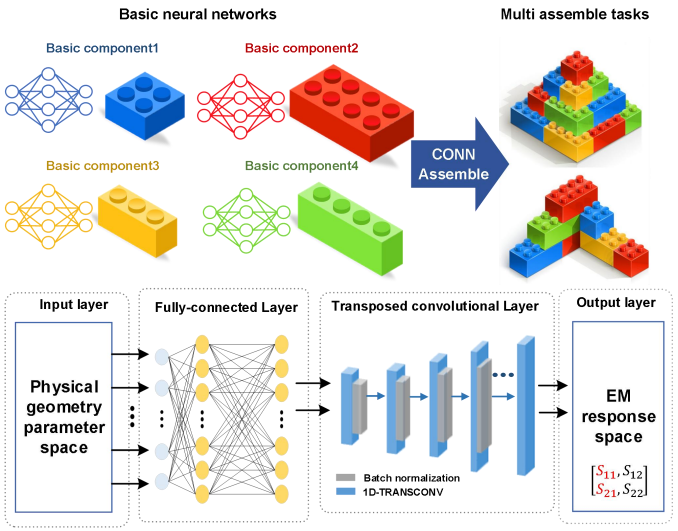
F. Zhou, **W.-S. Zhao***, et al., Machine Learning-Assisted Broadband *S*-Parameter Frequency-Domain Extrapolation Method, ***IEEE Trans. MTT***, 2026.

2 Assemble-NN S-parameter modeling Method

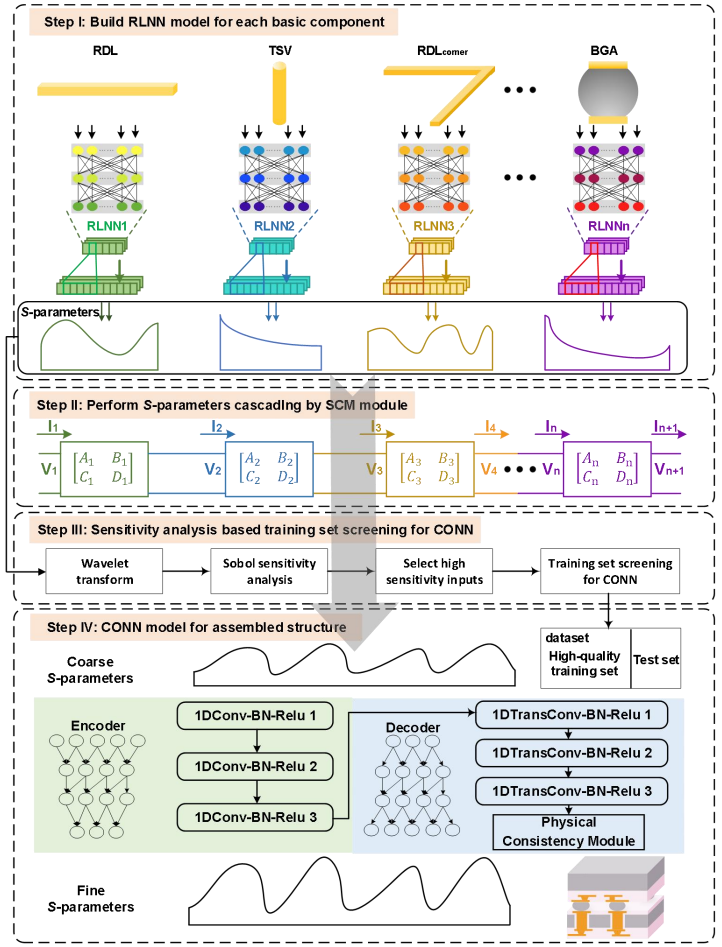
- An assemble-NN surrogate with physically consistent interconnect-unit modeling enables efficient reuse, overcoming conventional models' generalization limits and data hunger.



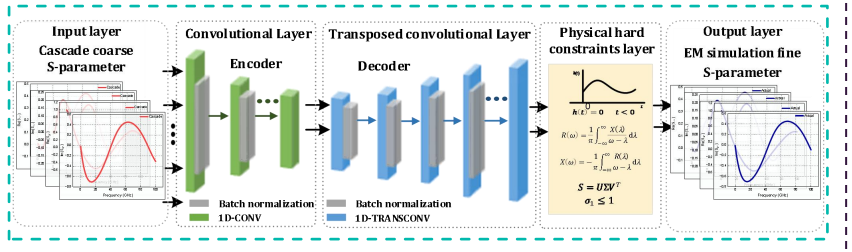
3D package interconnects: TSV, RDL



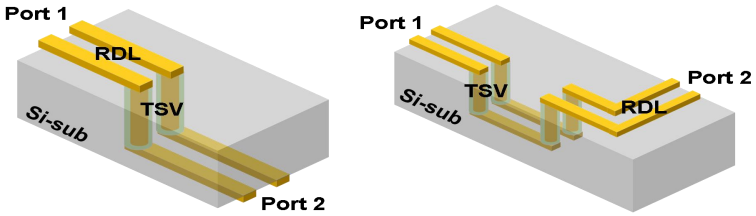
Surrogate model: RLNN



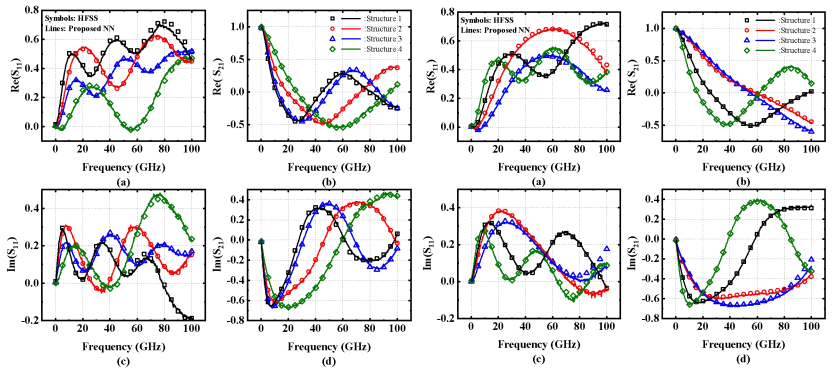
Overall architecture of assembled neural network



Couple model: CONN



Test structure

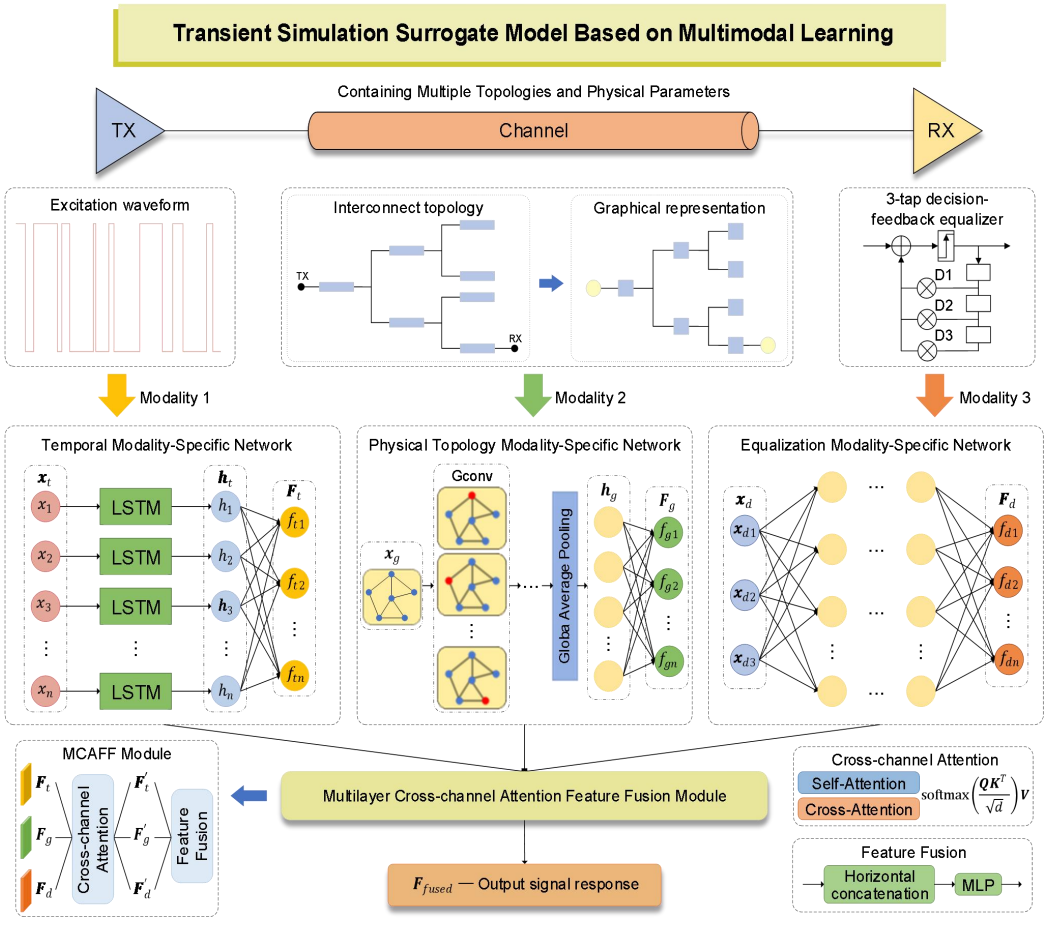


S-parameter prediction results

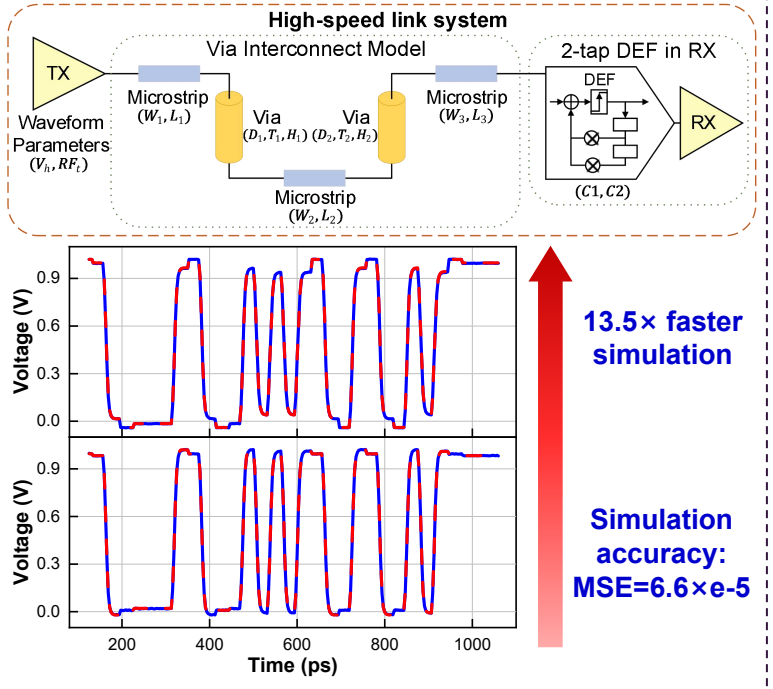
Z.-X. Ye, **W.-S. Zhao***, et al., Frequency Domain Modeling of Interconnects Based on Assemble Neural Network for 3D Integration, ***IEEE Trans. CAD***, 2025.

2 Multimodal ML-Based Surrogate Modeling

- A multimodal-machine-learning surrogate with co-optimization overcomes complex interactions for efficient high-speed link system-level analysis.



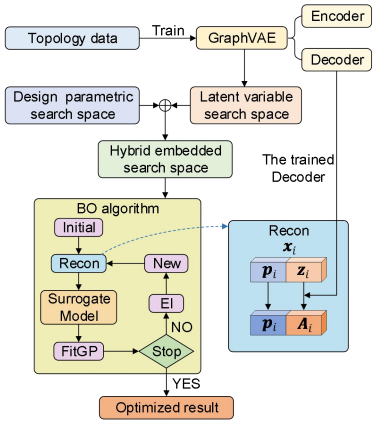
Multimodal ML-Based Transient Surrogate Modeling



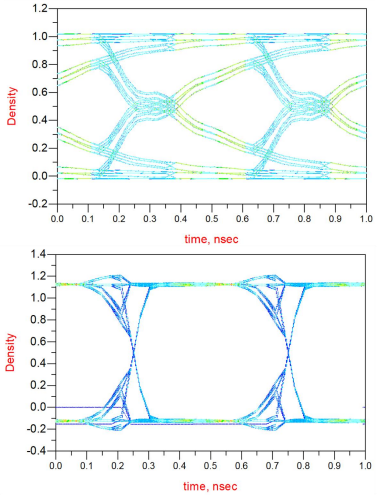
Prediction Results of the Surrogate Model

Model	Known System		Unknown System	
	MSE (V^2)	MAE (V)	MSE (V^2)	MAE (V)
RNN	3.8×10^{-4}	1.5×10^{-2}	3.6×10^{-3}	5.1×10^{-2}
LSTM	2.9×10^{-4}	1.3×10^{-2}	3.7×10^{-3}	5.2×10^{-2}
GRU	1.5×10^{-3}	3.6×10^{-2}	2.7×10^{-3}	4.9×10^{-2}
Proposed	2.9×10^{-5}	3.9×10^{-3}	6.6×10^{-5}	5.7×10^{-3}

Accuracy Comparison of Different Methods



Co-Optimization Workflow

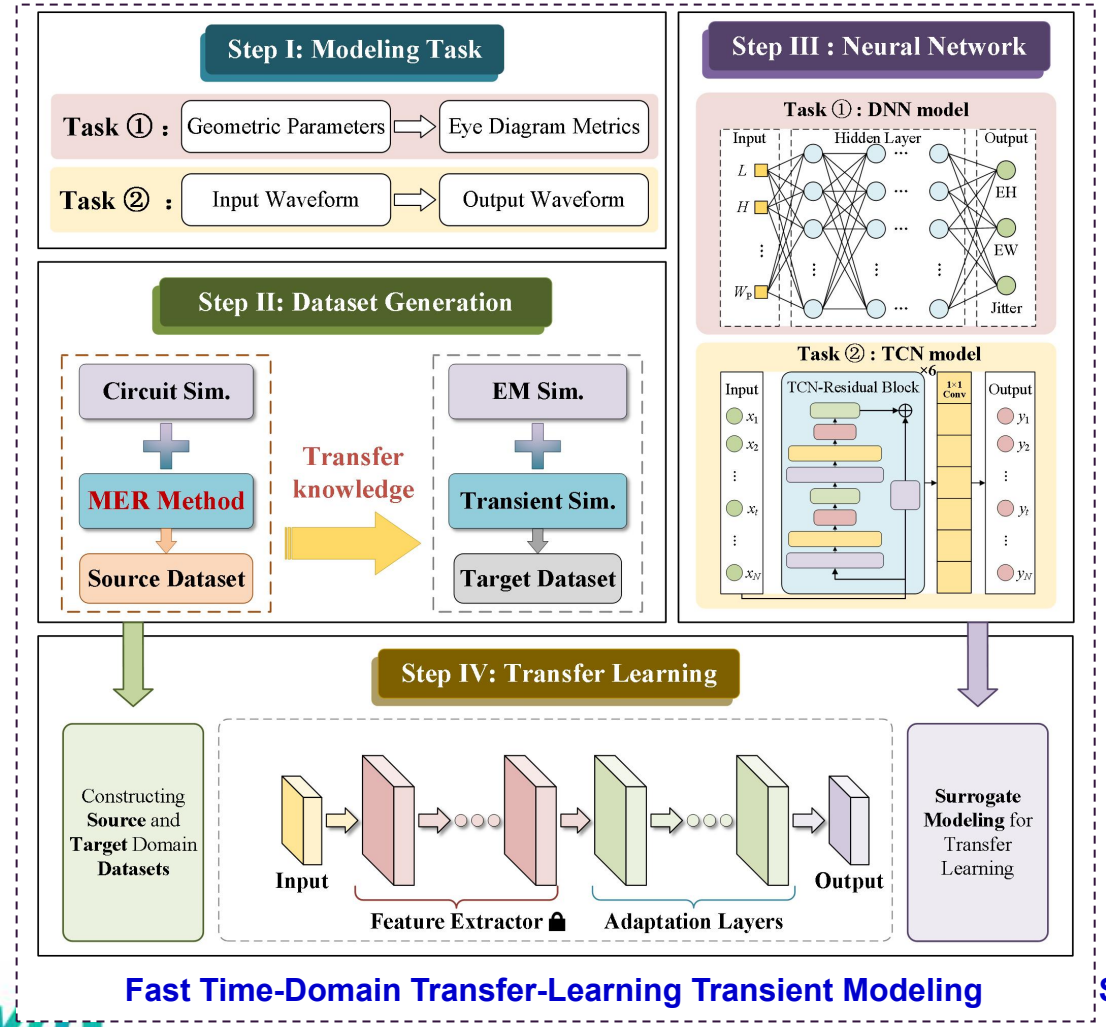


Before and After

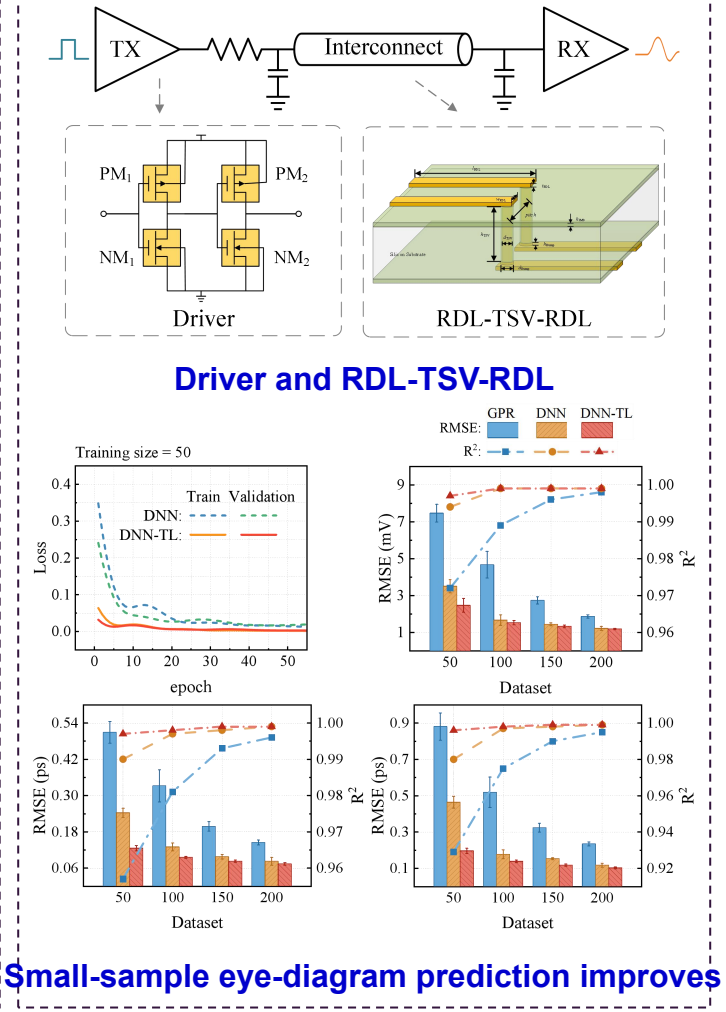
X.-Y. Wu, **W.-S. Zhao***, et al., High-Speed Link System Surrogate Modeling and Co-Optimization Based on Multimodal Machine Learning and GraphVAE, ***IEEE Trans. MTT***, 2025.

2 Transfer-Learning Time-Domain Modeling

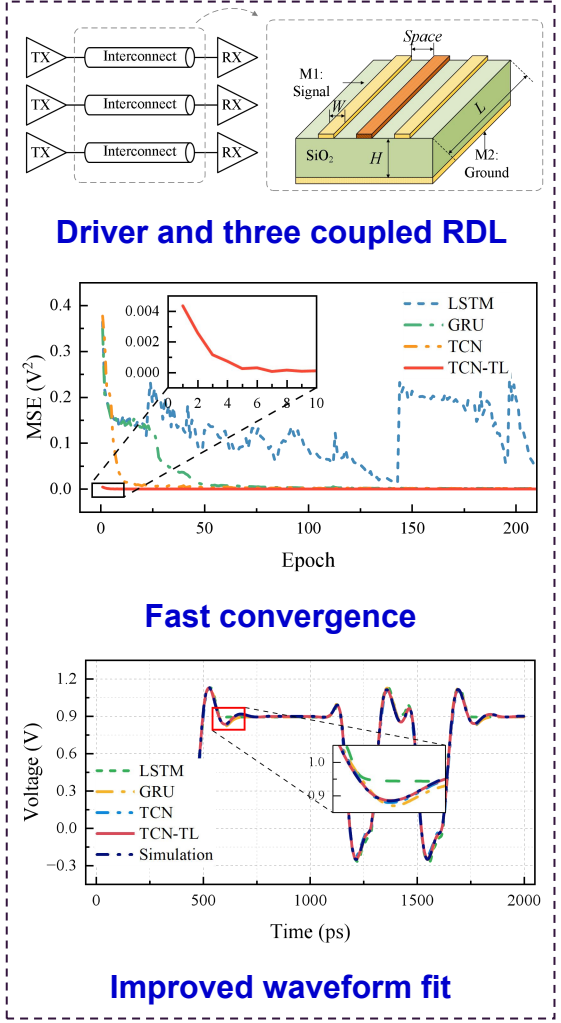
- Integrating fast time-domain simulation with transfer learning overcomes conventional simulation bottlenecks, enabling efficient modeling under small-sample conditions.



Fast Time-Domain Transfer-Learning Transient Modeling



Small-sample eye-diagram prediction improves

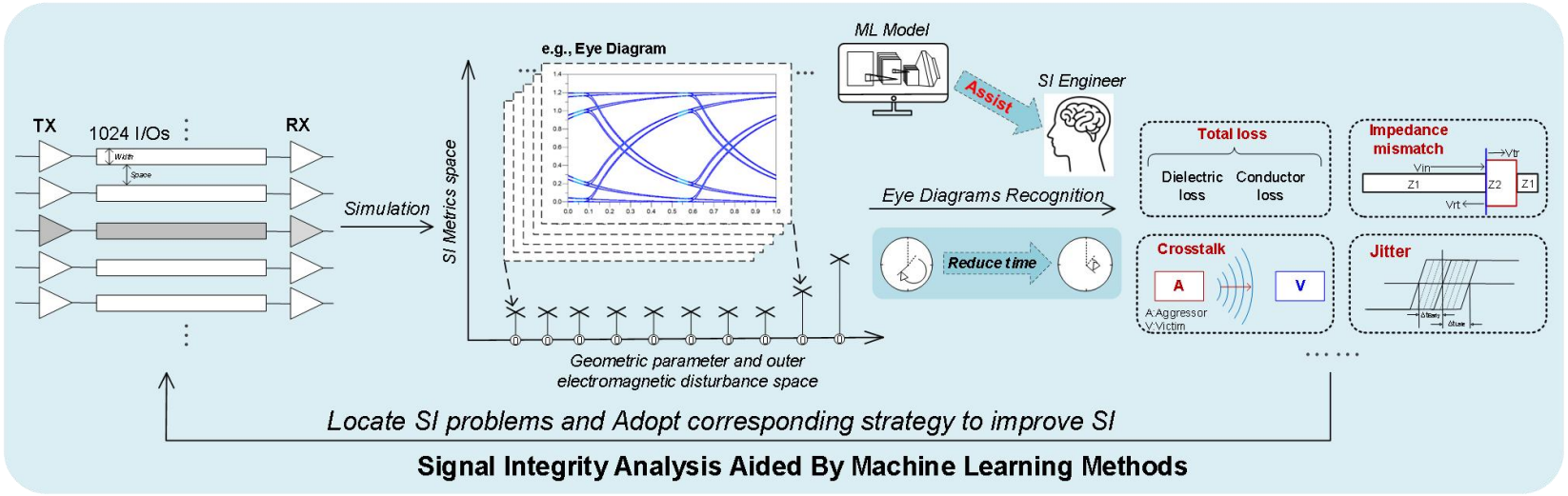


Improved waveform fit

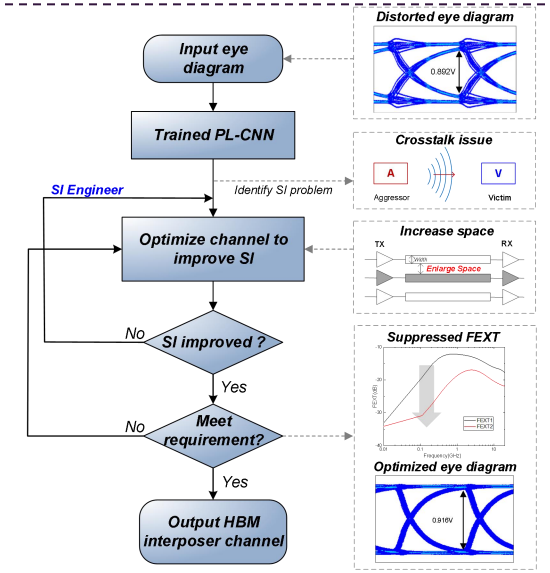
M.-Y. Yu, **W.-S. Zhao***, et al., A Novel Surrogate Modeling Framework Based on Fast Time-Domain Simulation and Transfer Learning for Signal Integrity Analysis, ***IEEE Trans. CPMT,*** (early access).

2 Eye-Diagram Quality Classification Method

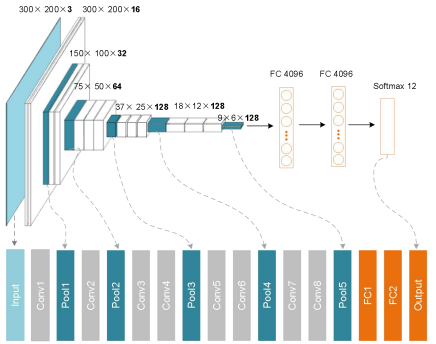
- PL-CNN with clustering and CNNs provides rapid eye-diagram degradation diagnosis via semi-supervised distortion-mechanism identification for SI engineers.



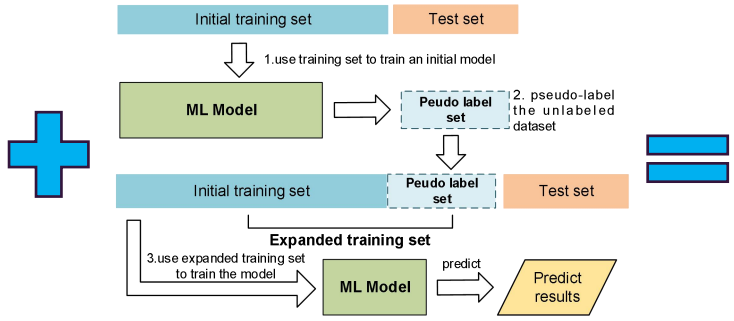
Machine Learning-Accelerated SI Analysis Method



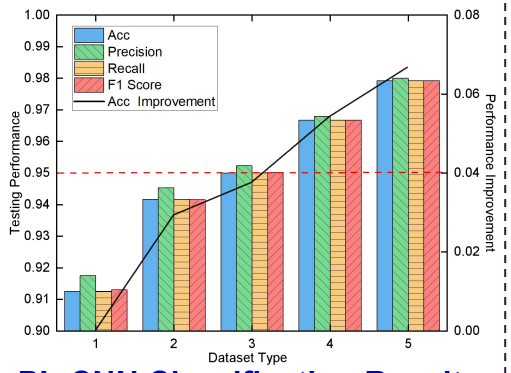
SI Analysis with the Proposed Method



Structure of CNN



Flowchart of the PL-CNN Learning Method



PL-CNN Classification Results

	LeNet	[16]	[17]	AlexNet	This study
Training Epochs	100	170	150	350	320
Training Time (s)	~ 1500	~ 2770	~ 2630	~ 8400	~ 4194
Testing Time (s)	1.5806	2.5729	1.7491	6.3009	3.8666
Testing Accuracy	0.7375	0.8542	0.7958	0.8708	0.9125
Testing Precision	0.7823	0.8601	0.8149	0.8733	0.9175
Testing Recall	0.7375	0.8542	0.7958	0.8708	0.9125
Testing F1 Score	0.7420	0.8534	0.7940	0.8703	0.9130

Results of Different Methods

C.-S. Mao, **W.-S. Zhao***, et al., Pseudo-Labeling Based Semi-Supervised Learning for Signal Integrity Analysis of High-Bandwidth Memory (HBM) Interposer, ***IEEE Trans. EMC***, 2024.

OUTLINE

1. Background

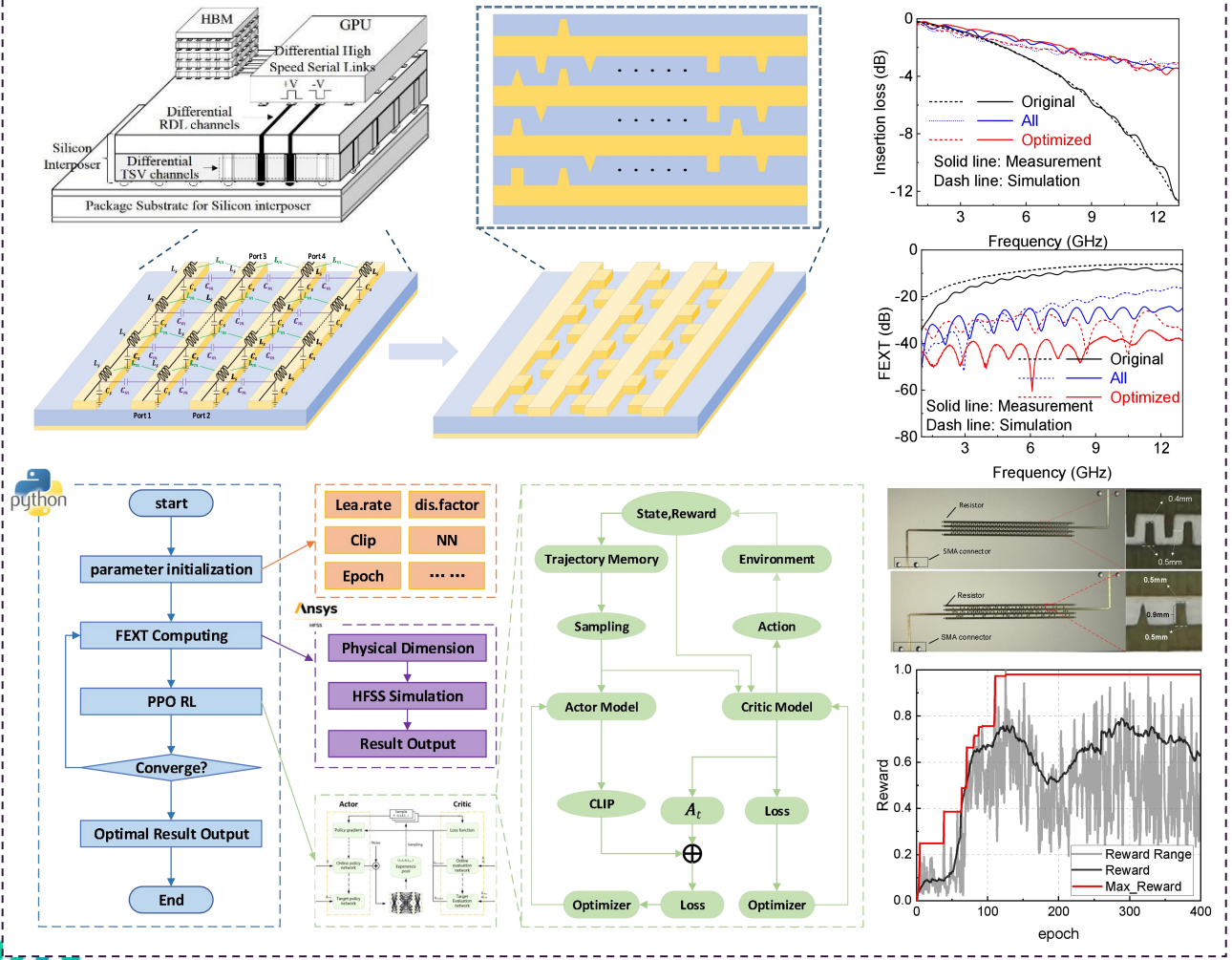
2. Surrogate modeling and analysis

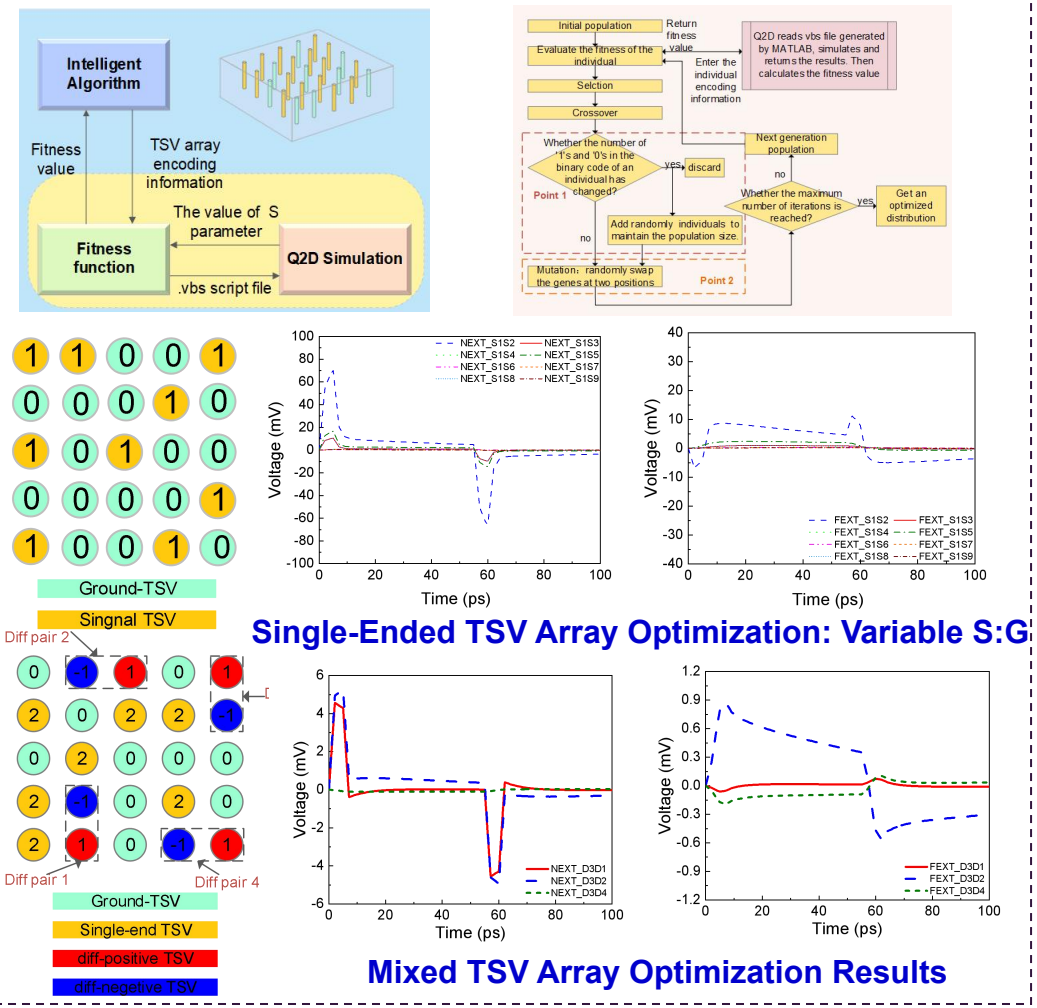
3. Co-design optimization

4. Conclusions

3 Crosstalk Suppression Method

- RL-based optimization of stub number and layout for crosstalk reduction
- GA-based TSV layout optimization for crosstalk suppression



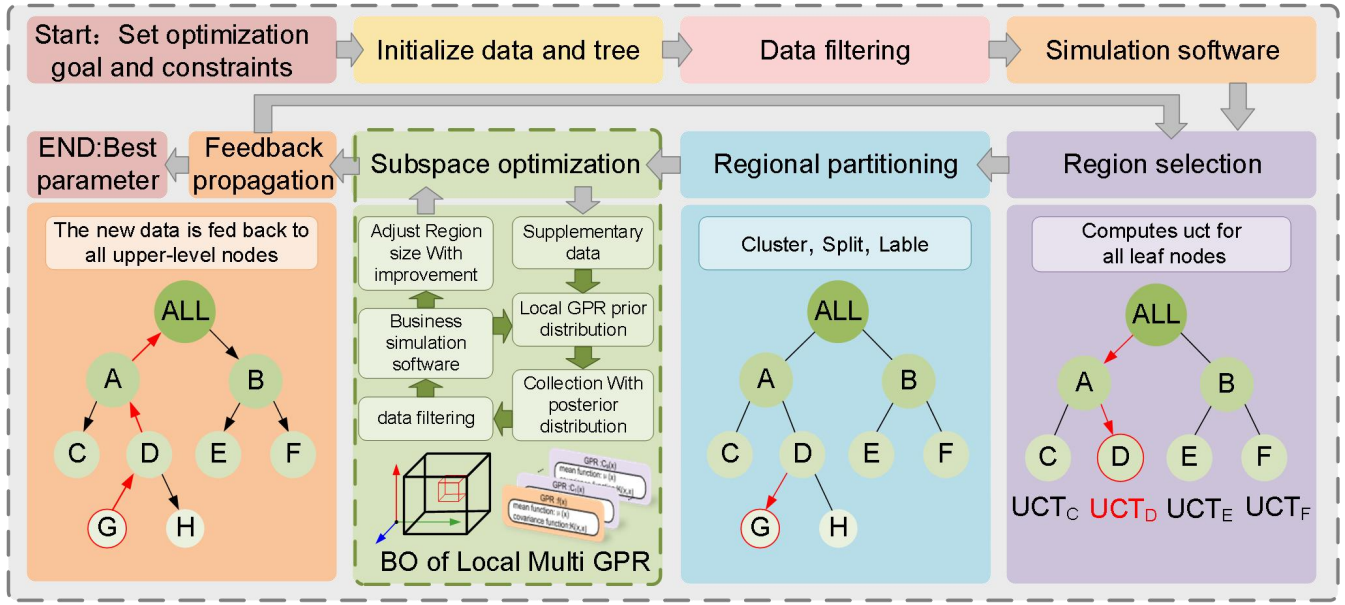


C.-J. Mai, **W.-S Zhao***, et al., ***IEEE Trans.EMC***, 2025.

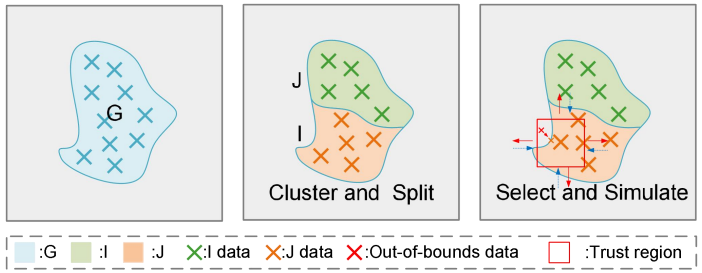
J.-Y. Ju, **W.-S. Zhao***, et al., ***IEEE Trans. CPMT***, 2025.

3 High-Dimensional Equalizer Optimization

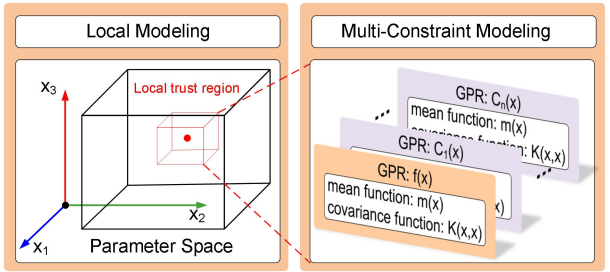
- **Bayesian optimization with local constraints and region partitioning enables fast high-dimensional equalizer design and eye-diagram quality enhancement for PCIe/UCIe links.**



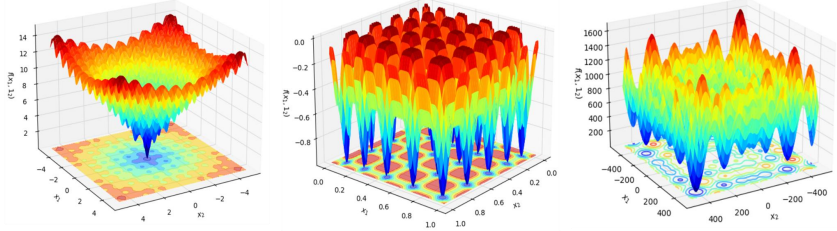
Local GPR-Based Bayesian Optimization



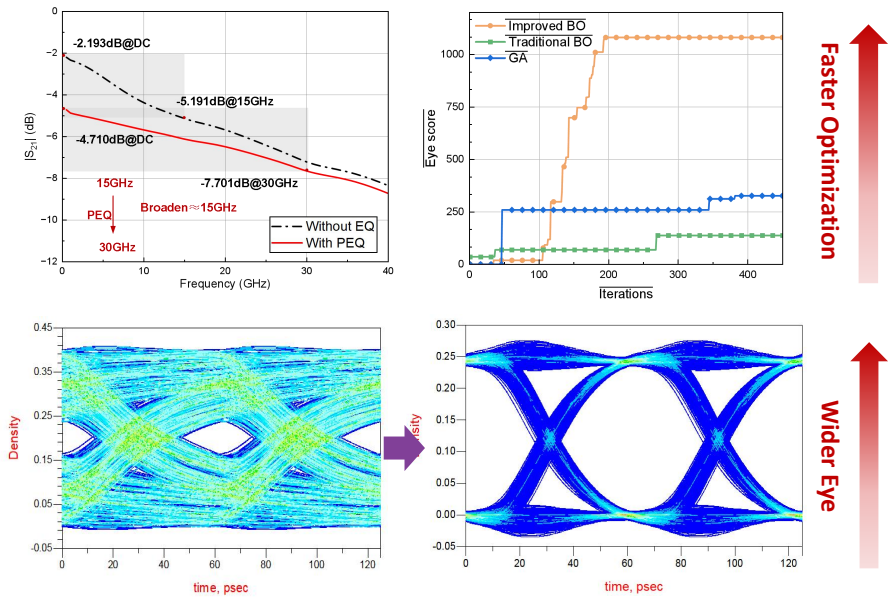
Region Partitioning Technique



Multi-Constraint Modeling



Benchmark Functions

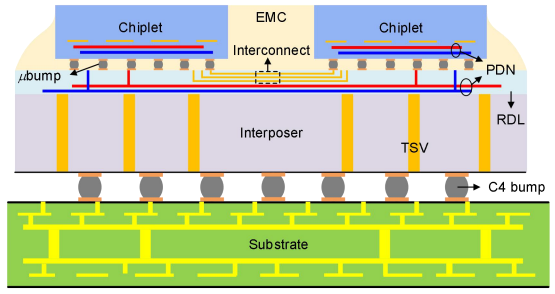


Algorithm Validation & Performance Evaluation

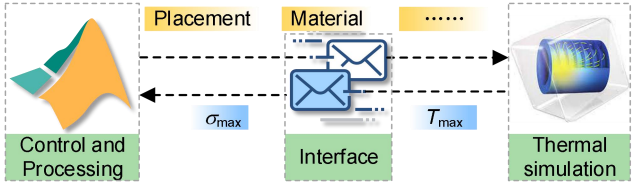
X.-R. Li, **W.-S. Zhao***, et al., Equalizer Optimization Method Based on Local Multi-Constraint Modeling-Bayesian Optimization with Region Partitioning, ***IEEE Trans. CAS-I***, 2025.

3 Thermal-Power Integrity Co-Design

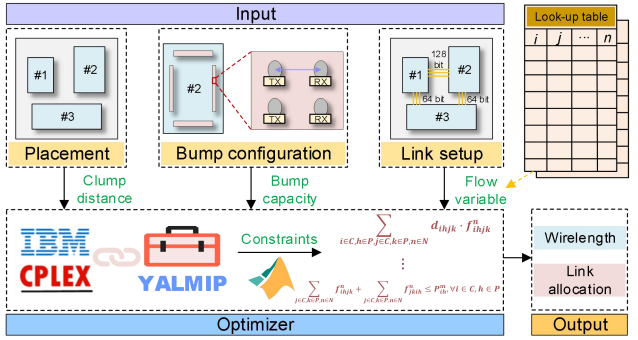
- **Adaptive genetic algorithm-driven thermal-power co-design optimizes layout and decoupling capacitors, enhancing thermal and power integrity beyond mainstream.**



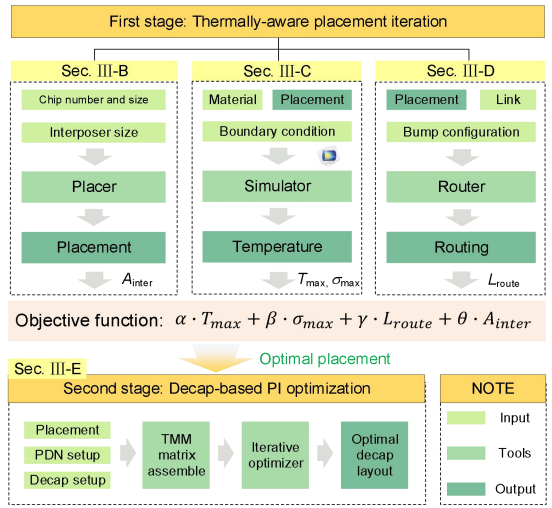
2.5-D Chiplet Package



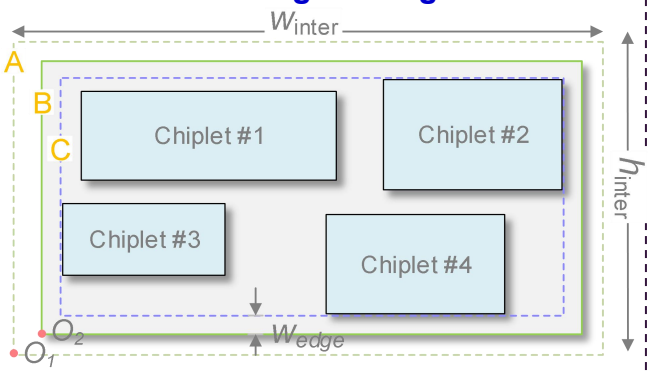
Thermal Evaluation



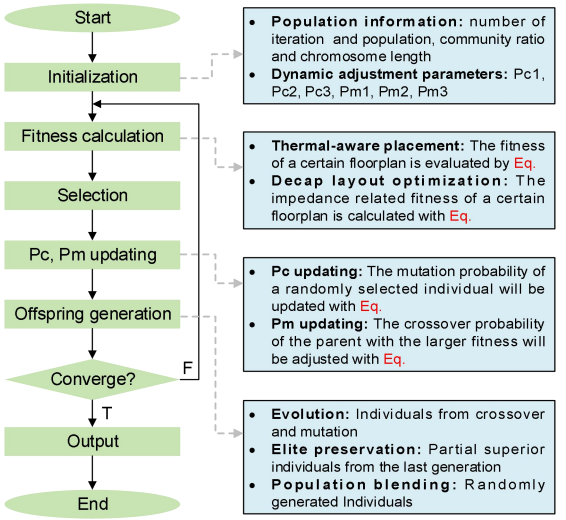
Wirelength Design



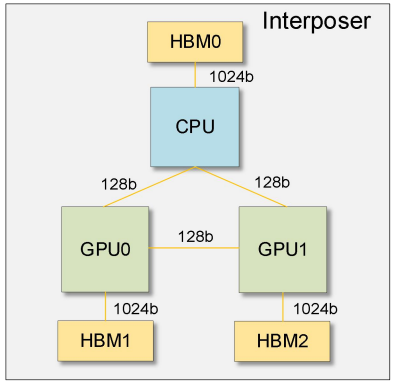
Co-Optimization Framework



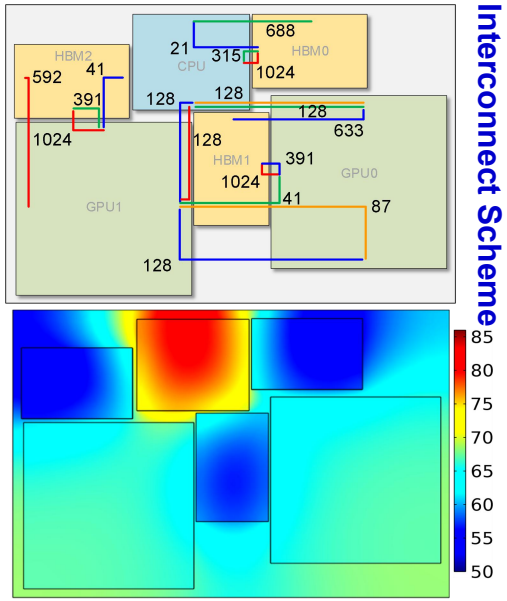
Area Constraint

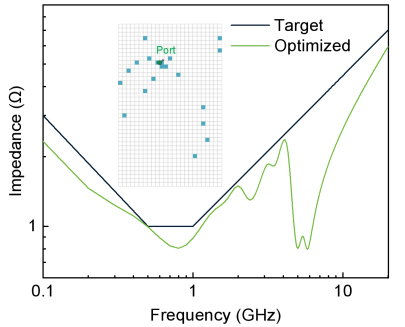


IAGA Algorithm



Baseline Scheme



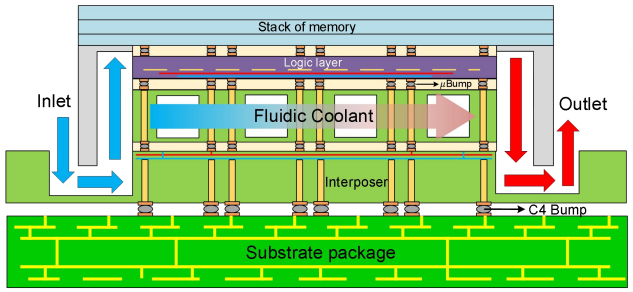


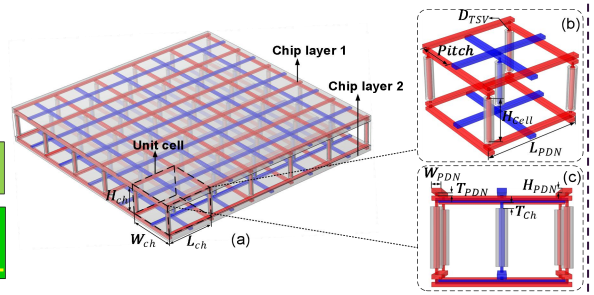
Optimized Impedance Curve

P. Zhang, **W.-S. Zhao***, et al., A Thermal and Power Integrity Co-Optimization Framework for 2.5-D Integrated Microsystem," ***IEEE Trans. CAS-I***, 2025.

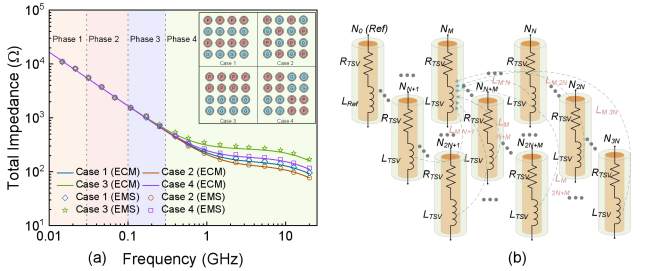
3 Electro-Thermal Co-Optimization Method

- A scalable 3D-IC multiphysics flow using equivalent circuits, Transformer-Pointer PPO, and Tri-HSSL-NSGA-II jointly optimizes PDN integrity, cooling, and efficiency.

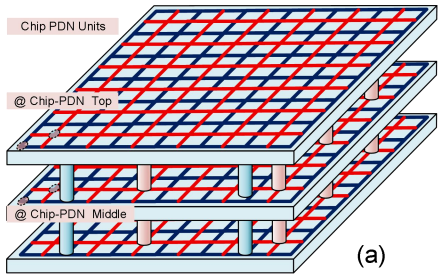


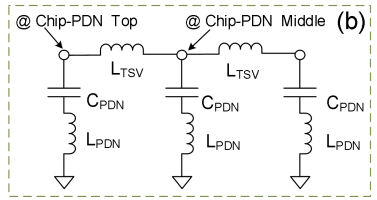


3-D Stacked Package with Embedded Microchannels

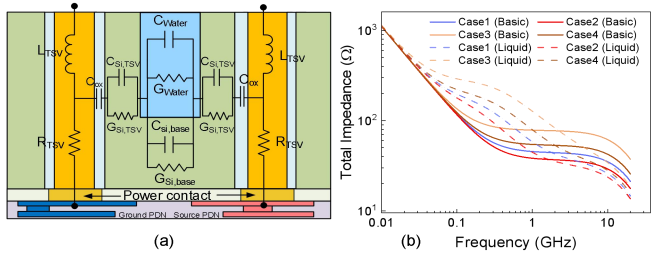


3-D Power Delivery Network Structure



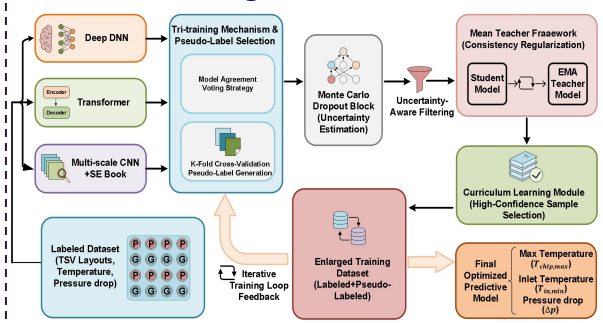


Equivalent PDN Circuit Model with TSV Arrays and Embedded Microchannels

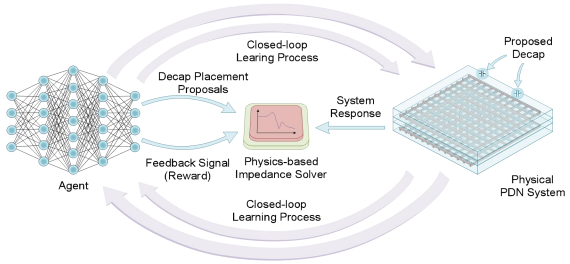


Stacked PDN Equivalent Circuit Model

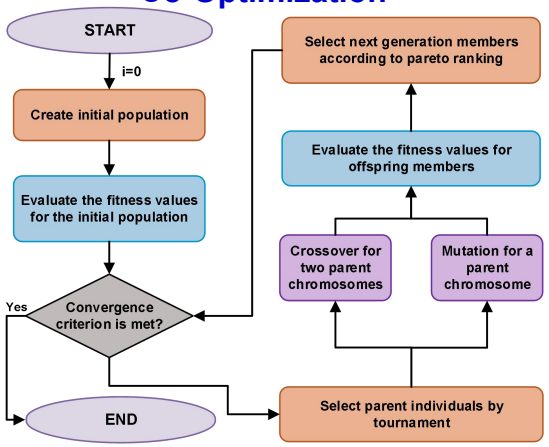
Multi-Agent Thermal Surrogate Framework

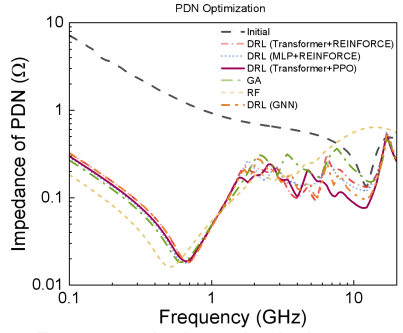


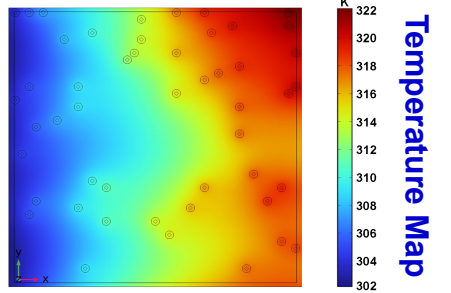
Transformer-Pointer Optimizer Framework



Fast GA for Thermal–Electrical–Flow Co-Optimization







Optimized Impedance Temperature Map

C.Y. Feng,**W.-S. Zhao*** et al., Machine Learning-Assisted Electro-Thermal Co-Optimization Framework for PDN in 3-D Integrated Microsystem With ...," ***IEEE Trans. CAS-I***, 2026.

OUTLINE

1. Background

2. Surrogate modeling and analysis

3. Co-design optimization

4. Conclusions

4 Summary and Outlook

- For multiphysics integrity in 3-D integrated microsystems, preliminary studies have been carried out across the “modeling–simulation–optimization” flow:
  - Develop surrogate models for 3-D interconnect frequency responses;
  - Improve multiphysics simulation efficiency using hybrid methods;
  - Explore co-optimization methods for multiphysics integrity.
- Challenges ahead(representative cross-domain issues remain to be addressed):
  - How to build heterogeneous interface models for multiphysics simulation?
  - How to substantially improve multiphysics simulation efficiency?
  - How to achieve cross-hierarchy co-optimization of multiphysics integrity?
  - How to collaborate with industry to establish data acquisition mechanisms?
  - …… ……
- Advances in co-packaged optics (CPO), flexible electronics, and related technologies will introduce higher-dimensional challenges!

4 Representative Publications

- F. Zhou, W.-S. Zhao*, et al., Machine Learning-Assisted Broadband *S*-Parameter Frequency-Domain Extrapolation Method, *IEEE Trans. MTT*, 2026.
- Z.-X. Ye, W.-S. Zhao*, et al., Frequency Domain Modeling of Interconnects Based on Assemble Neural Network for 3D Integration, *IEEE Trans. CAD,* 2025.
- X.-Y. Wu, W.-S. Zhao*, et al., High-Speed Link System Surrogate Modeling and Co-Optimization Based on Multimodal Machine Learning and GraphVAE, *IEEE Trans. MTT*, 2025.
- M.-Y. Yu, W.-S. Zhao*, et al., A Novel Surrogate Modeling Framework Based on Fast Time-Domain Simulation and Transfer Learning for Signal Integrity Analysis, *IEEE Trans. CPMT,* (early access).
- D.-W. Wang, W.-S. Zhao*, et al., Proper Orthogonal Decomposition and LSTM NN Based Multiphysics DT Model for Electronic Device Online Condition Monitoring, *IEEE Trans. IM*, 2025.
- D.-W. Wang, WS Zhao*, et al., A proposal of fast thermal simulation method for 2.5-D advanced packaging to enable efficient thermal-aware placement optimization, *IEEE Trans. CAD*, 2026
- C.-S. Mao, W.-S. Zhao*, et al., Pseudo-Labeling Based Semi-Supervised Learning for Signal Integrity Analysis of High-Bandwidth Memory (HBM) Interposer, *IEEE Trans. EMC*, 2024.
- X.-R. Li, W.-S. Zhao*, et al., Equalizer Optimization Method Based on Local Multi-Constraint Modeling-Bayesian Optimization with Region Partitioning, *IEEE Trans. CAS-I*, 2025.
- P. Zhang, W.-S. Zhao*, et al., A Thermal and Power Integrity Co-Optimization Framework for 2.5-D Integrated Microsystem," *IEEE Trans. CAS-I*, 2025.
- P. Zhang, W.-S. Zhao*, et al., *IEEE Trans. CPMT*, 2023; C.-Y. Feng, W.-S. Zhao, et al., *ICHMMT*, 2024; C.-Y. Feng, W.-S. Zhao*, et al., *Appl. Thermal Eng.*, 2025
- C.Y. Feng,W.-S. Zhao* et al., Machine Learning-Assisted Electro-Thermal Co-Optimization Framework for PDN in 3-D Integrated Microsystem With ...," *IEEE Trans. CAS-I*, 2026.
- ……





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Thanks.

Hangzhou Dianzi University



Feedback/Ph.D. welcome. Contact: davidw.zoeq@hdu.edu.cn