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A Transformer-Driven Engine for High-Speed Interconnect Modeling and Multi-Objective Optimization in Seconds

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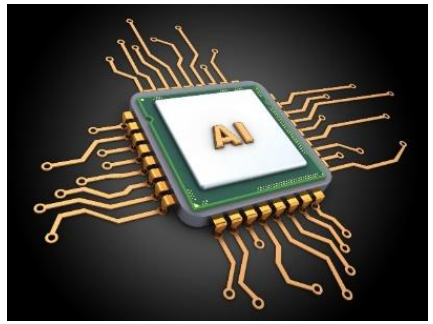
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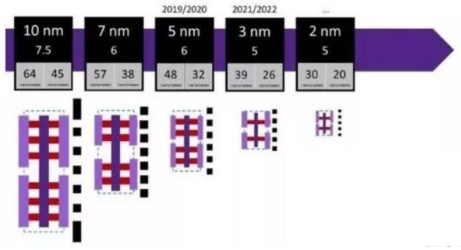
Research Background

Rapid advances in integrated circuits

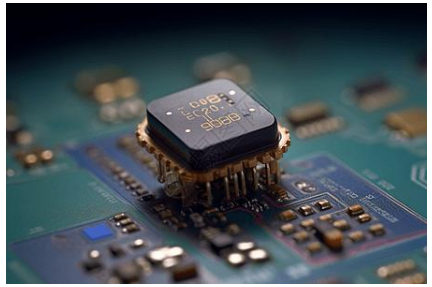
Data-driven demand



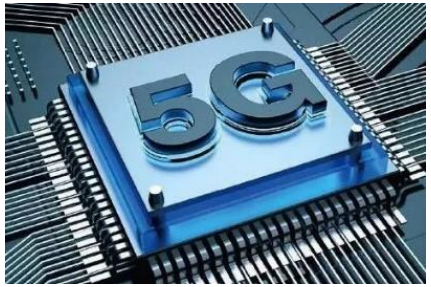
High integration



Miniaturization



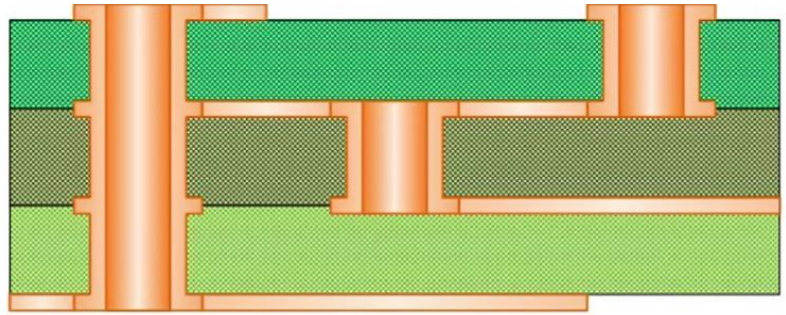
High speed / frequency



Data transfer
High rate
High bandwidth

High-speed interconnects are critical

Rapid growth in data exchange
Interconnects become a **bottleneck**



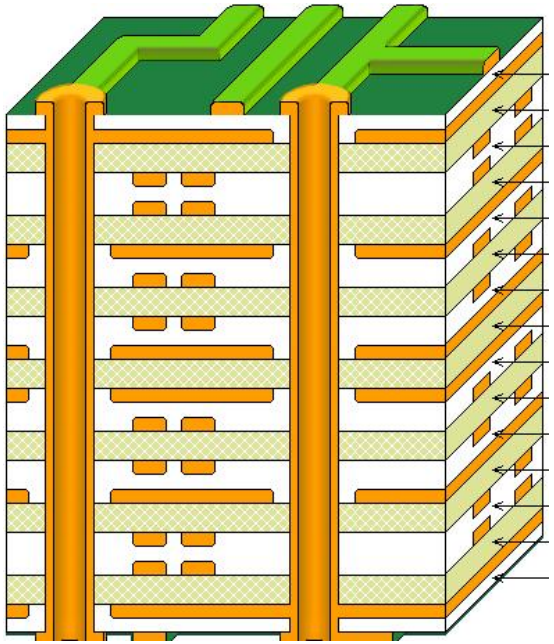
Importance
Remove **bottleneck**s
Enable computing
Support technology
Enable applications

Applications
On-chip links
Data centers
Consumer devices
Manufacturing

High-speed interconnects support many application areas

Research Background

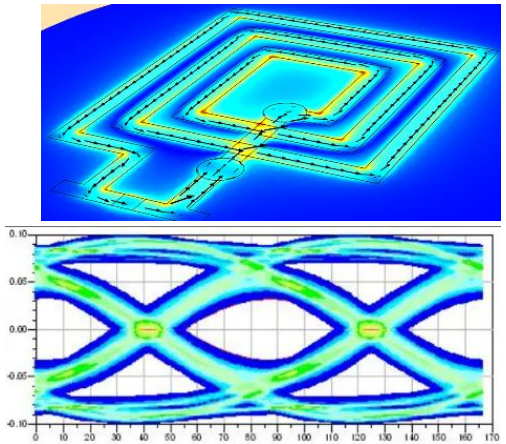
High-speed interconnects
Design parameters
SI performance metrics



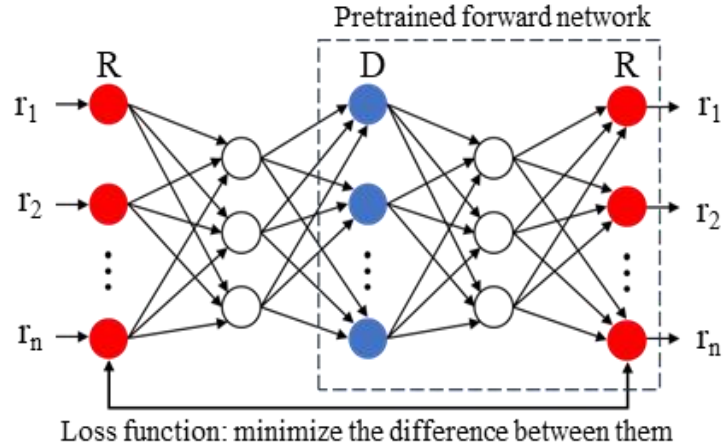
Conventional optimization
Numerical computation
Mathematical models

VS

AI inverse optimization
Data-driven learning
Parameter mappings



Full-wave simulation



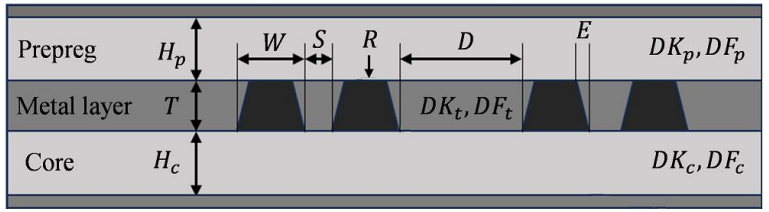
Cascaded DNN architecture

High simulation cost → **Faster optimization**

AI-based methods improve optimization efficiency

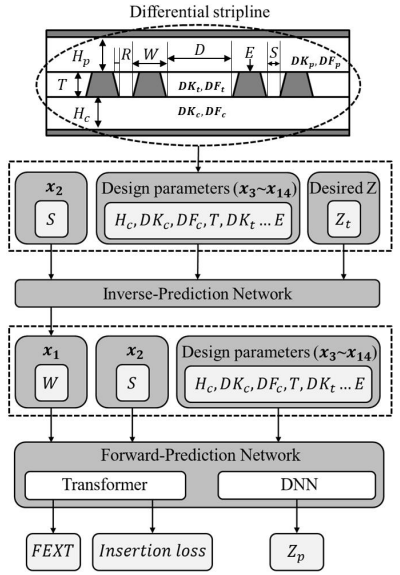
Research Objectives

Interconnect geometry and parameters



Parameter	Meaning	Range
x_1	Trace width (W)	2-16 mils
x_2	Trace spacing (S)	2-16 mils
x_3	Core height (H_c)	2-10 mils
x_4	Core DK (DK_c)	2.5-4.5
x_5	Core DF (DF_c)	0.001-0.03
x_6	Trace height (T)	0.4-2.6 mils
x_7	Resin Pocket DK (DK_t)	2.5-4.5
x_8	Resin Pocket DF (DF_t)	0.001-0.03
x_9	Prepreg height (H_p)	2-30 mils
x_{10}	Prepreg DK (DK_p)	2.5-4.5
x_{11}	Prepreg DF (DF_p)	0.001-0.03
x_{12}	Roughness level (R)	-10-10
x_{13}	Pair-to-pair distance (D)	6-40 mils
x_{14}	Etch factor (E)	0.1-1

Conventional design challenges
Large parameter space
Slow, costly simulations
Long design iterations



Transformer-driven modeling
and optimization in seconds

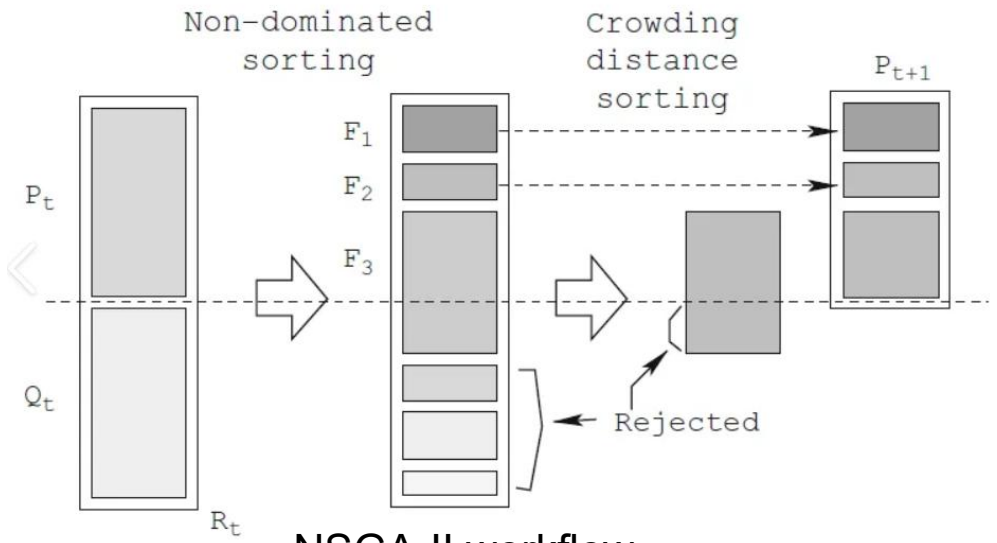
Objectives
Impedance error, loss, FEXT

Variables
Width W, spacing S, distance D

Modeling and multi-objective optimization in seconds

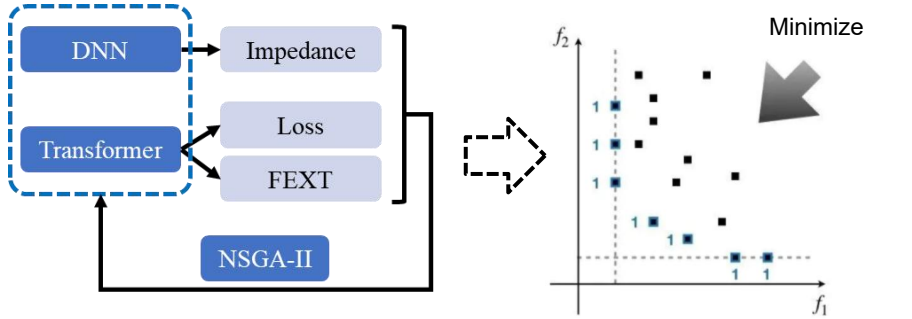
Conventional Multi-Objective Optimization: NSGA-II

NSGA-II multi-objective optimization
Fast non-dominated sorting and elitism
Minimize competing objective functions
Obtain a set of Pareto-optimal solutions



NSGA-II workflow

Minimization of multiple objectives



AI-assisted NSGA-II

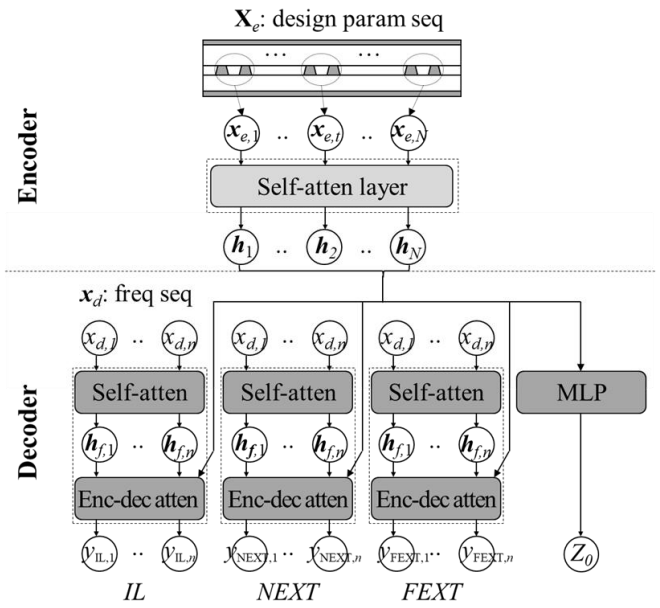
Pareto solution set

Search challenges
Complex Pareto fronts
Large candidate spaces
Slower iterative search

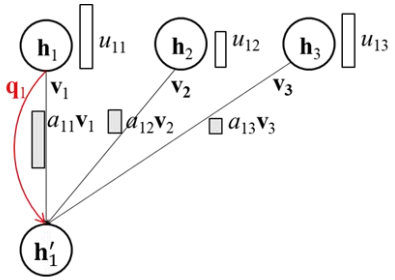
Optimization becomes costly as the model and search space grow

Transformer-Based Interconnect Modeling

Encoder–decoder Transformer model

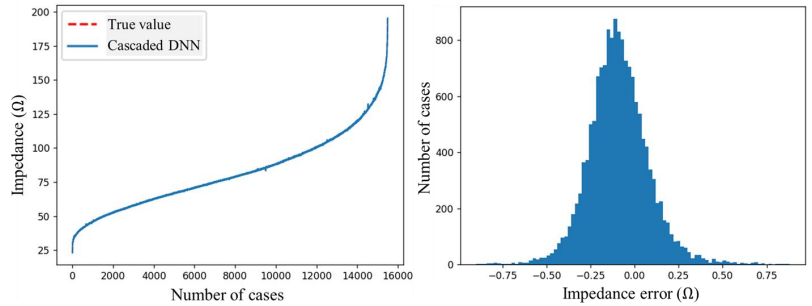


Self-attention
Sequence correlations form a weighted sum

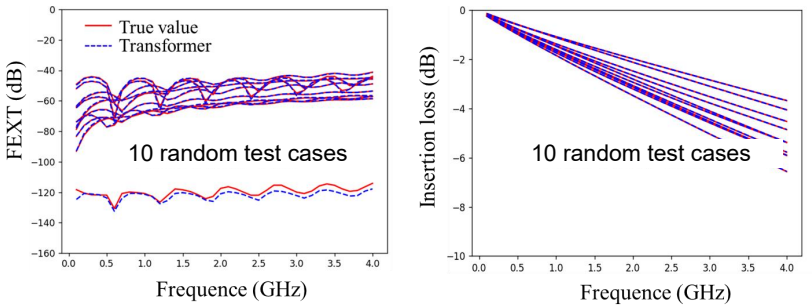


HSCT: Transformer model with **100,000** training samples
HSCT-P: parallel decoding across all frequency points
HSCT-S: sequential decoding with slightly higher accuracy
Scalability: 976 frequency points, reported error **2.47%**

Model input	**14 interconnect design parameters**
Model output	SI metrics across 1–40 GHz



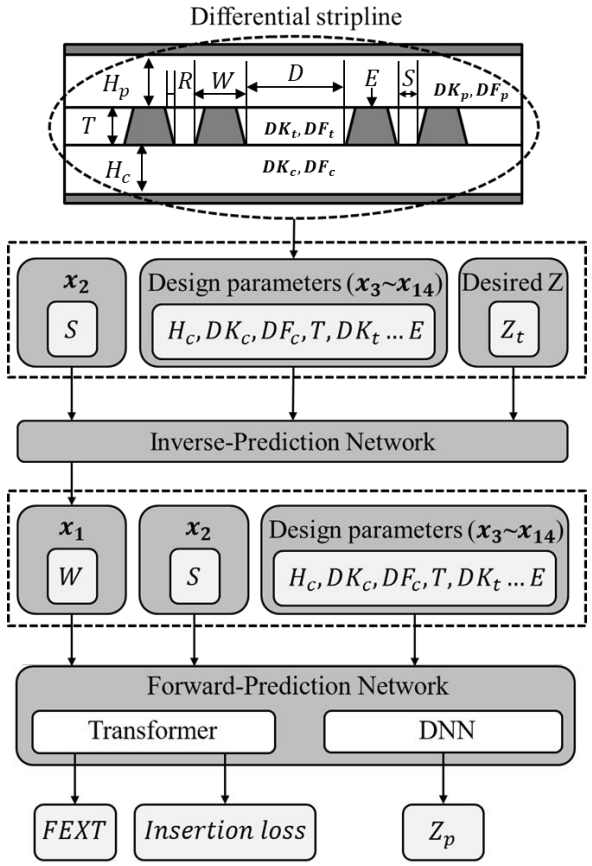
Impedance error: **−0.75 Ω to +0.75 Ω**



FEXT and IL prediction error: **< 2%**

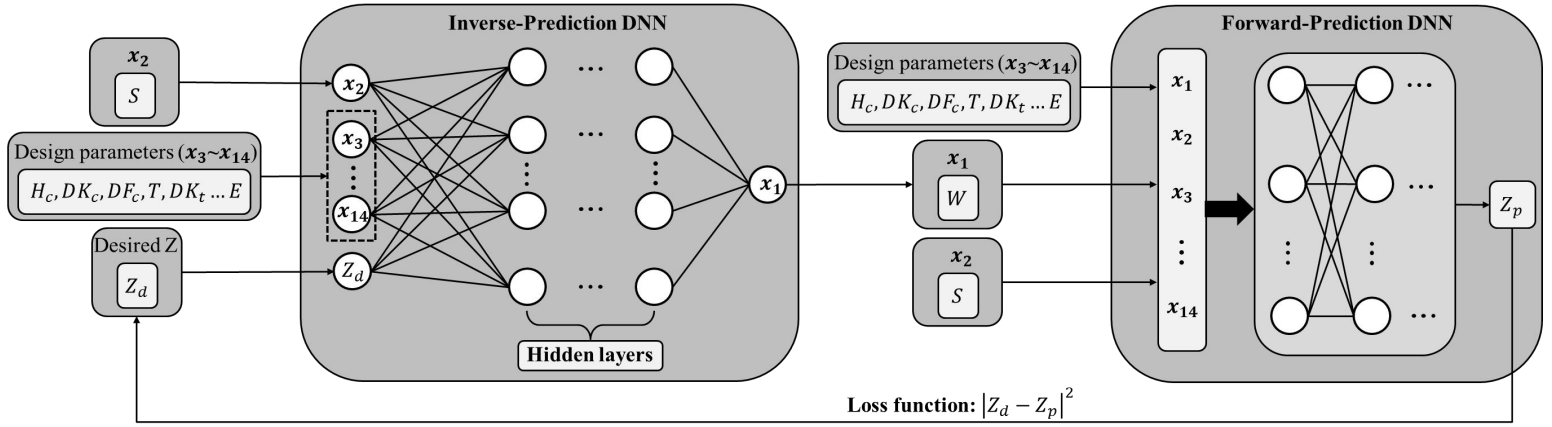
Transformer models provide accurate predictions of SI performance

Transformer-Driven Multi-Objective Inverse Design



Multi-objective inverse design

Transformer-based multi-objective optimization
Variables: trace width, trace spacing, and pair-to-pair distance
Objectives: impedance error, insertion loss, and FEXT



Network training: **predict W** and reduce **impedance error**

Modeling and multi-objective optimization in seconds

Inverse Network Architecture and Training

Item	Configuration
Dataset	**100,000** samples generated using IMLC
Training / validation / test	80,000 / 10,000 / 10,000
Inverse network	**14 inputs**, **5 hidden layers**, **1 output**
Hidden-layer neurons	256 / 128 / 64 / 32 / 16
Training setup	Adam, learning rate **0.0002**, early stopping
Activation functions	LeakyReLU, with Sigmoid at the output

Freeze the pretrained forward model and update only the inverse network.

Parameter Sweeps and Candidate Selection

1 **Fix the stack-up and materials**, and set the **target impedance**

2 **Sweep S** and **predict W** for each candidate

3 **Sweep D** and predict impedance, loss, and FEXT **in batches**

4 **Select feasible designs** based on loss, FEXT, and layout area

Single-layer case: S = 2–16 mil, step = 0.05 mil, **281 points**

Single-Layer Optimization with NSGA-II

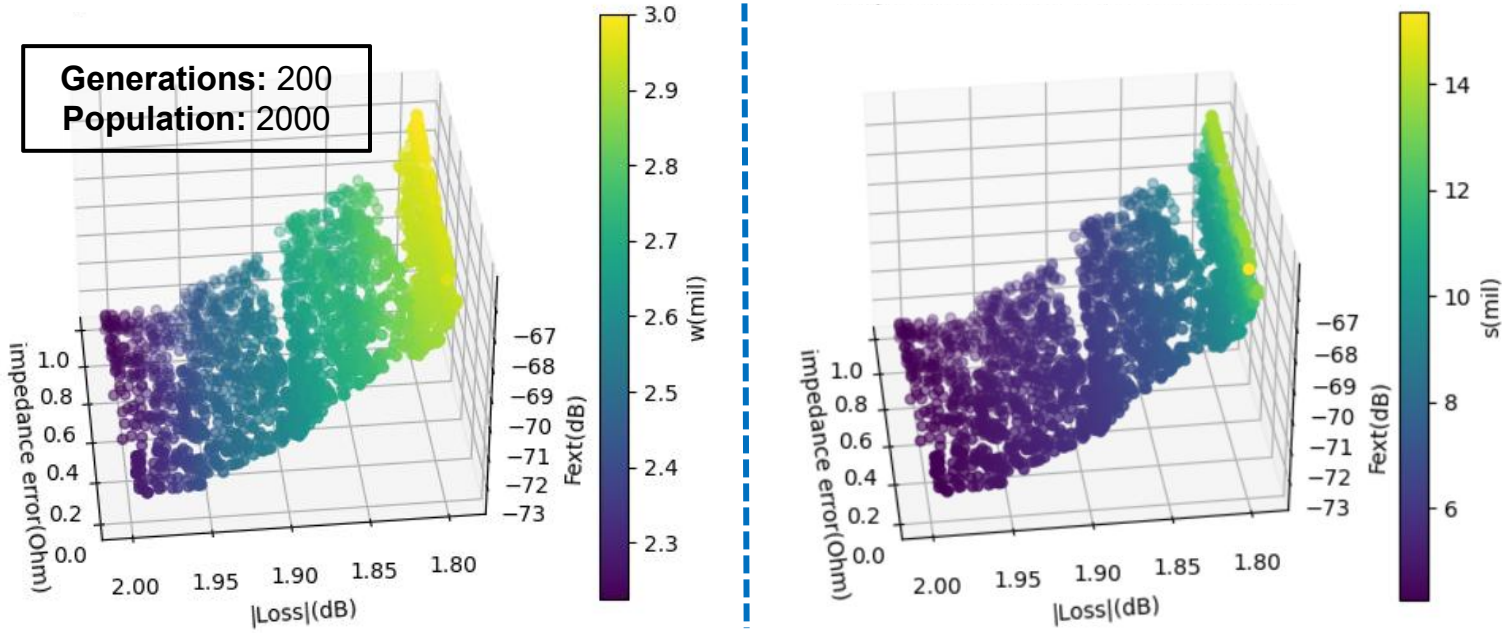
Stripline parameters

W	S	Hc	DKc	DFc	T	DKt	DFt	Hp	DKp	DFp	R	D	E	Zd
2~16	2~16	5	4.4	0.002	1.3	4.4	0.002	3	4.4	0.002	5	10	1	100

Variables
Trace width W
Trace spacing S

NSGA-II optimization

Generations: 200
Population: 2000



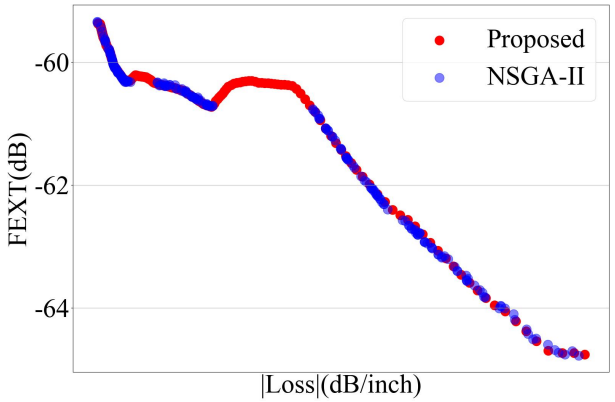
Objective functions
f_1 = |Zc − Ztarget|
f_2 = |Loss|
f_3 = FEXT

Runtime: 330 s

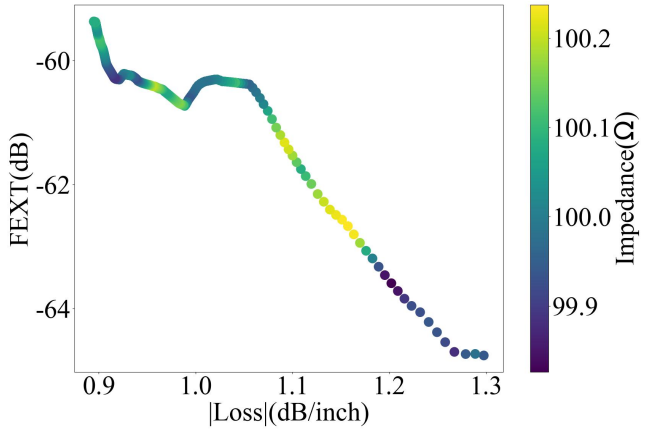
NSGA-II produces a 3D Pareto set in 330 s for this single-layer case

Single-Layer Optimization at Fixed D

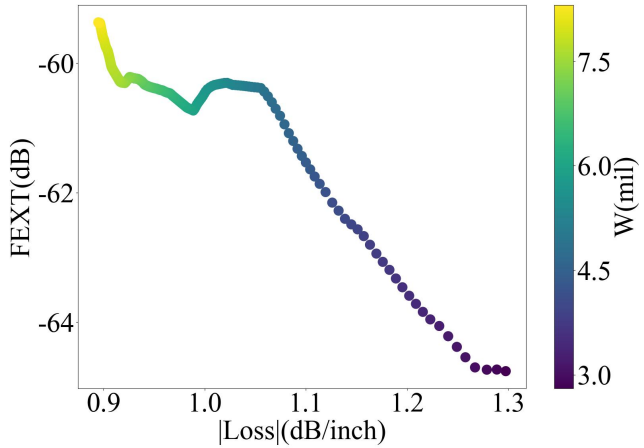
Comparison with NSGA-II



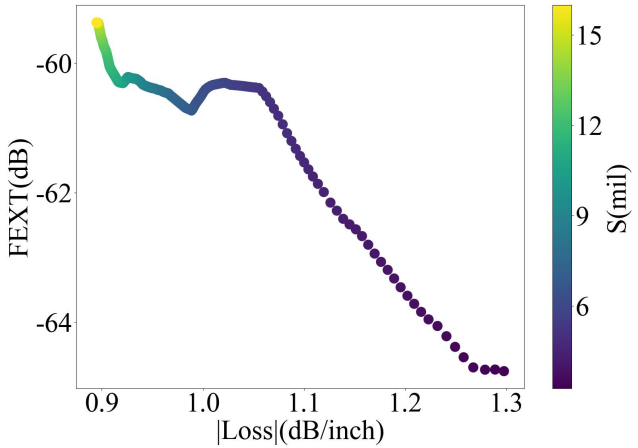
Impedance distribution



Trace-width distribution



Trace-spacing distribution



Stripline parameters

W	S	Hc	DKc	DFc	T	DKt	DFt
2~16	2~16	8	3.3	0.007	1. 3	3.3	0.007

Hp	DKp	DFp	R	D	E	Zd
10	3.3	0.007	-5	10	0.1	100

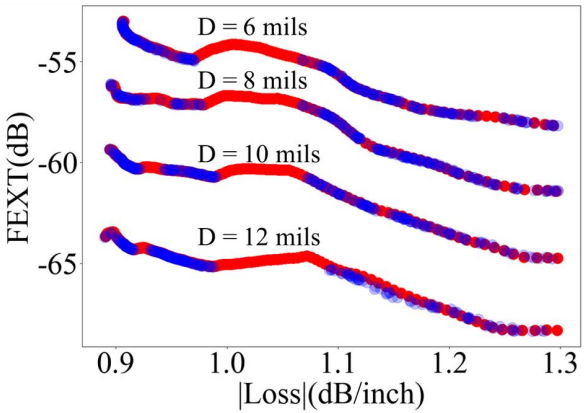
Engineering criteria
|Loss| at 16 GHz **≤ 1 dB/in**
FEXT at 16 GHz **≤ −40 dB**
Df = 0.007, Dk = 3.5
Hp and Hc: 2–10 mil

Optimization time
Proposed: **2 s**
NSGA-II: **330 s**

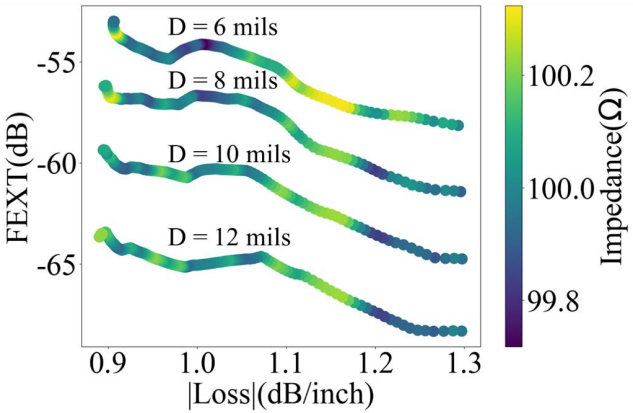
The proposed method optimizes W and S in 2 s

Single-Layer Optimization with D Swept

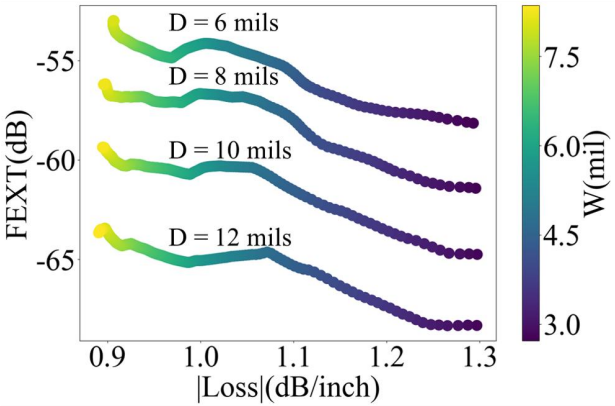
Comparison with NSGA-II



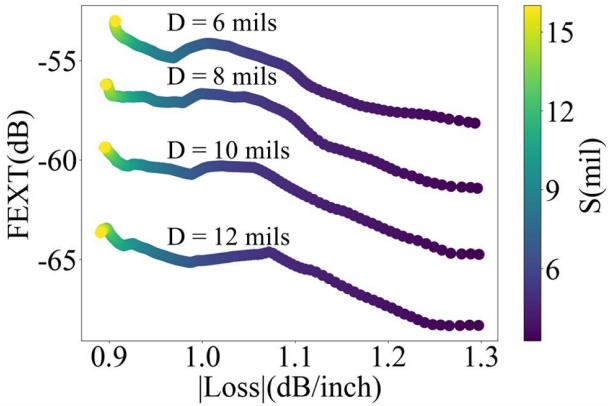
Impedance distribution



Trace-width distribution



Trace-spacing distribution



Physical effect
Larger D lowers FEXT
Loss changes little

Layout tradeoff
Larger D reduces coupling
and uses more area

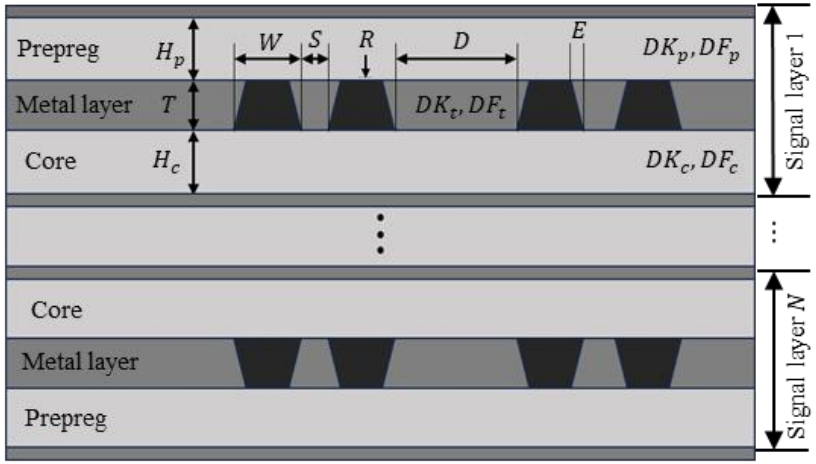
Select the appropriate tradeoff

Optimization time
Proposed: **2.5 s**
NSGA-II: **12 min**

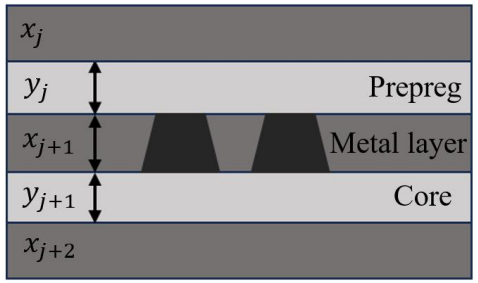
The proposed method jointly optimizes W, S, and D in 2.5 s

Multilayer Stack-Up Optimization

Multilayer interconnect



Layer type and thickness



Layer j: $x_j = 0$ for ground
$x_j = 1$ for signal
Dielectric thickness: y_j
L: total number of layers
N: number of signal layers

Signal-layer count equals N
Total height within tolerance
At most two signals in three layers
Symmetric layer arrangement
Symmetric dielectric thicknesses

Integer programming

$$\Sigma_j x_j = N$$
$$T - \Delta T \le \Sigma_j y_j \le T + \Delta T$$
$$x_j + x_{j+1} + x_{j+2} \le 2$$
$$x(j) = x(L - j - 1)$$
$$y(j) = y(L - j - 2)$$

	Layer type	Thickness
Casenumber		1
	Soldermas	0.5
1	TOP	1.9
Prepreg	PP	4.5
2	GND	1.3
Core	Core	3.5
3	INNER1	1.3
Prepreg	PP	7.5
4	GND	1.3
Core	Core	3.5
...	...	...
20	INNER10	1.3
Core	Core	3.5
21	GND	1.3
Prepreg	PP	4.5
22	BOTTOM	1.9
	Soldermas	0.5
	Total Hei	159.2

Integer programming determines the stack-up in about 3 s

Multilayer Interconnect Optimization Results

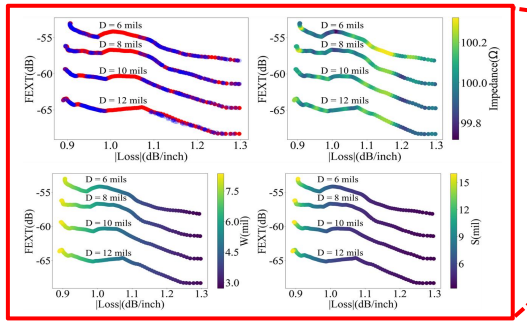
Input: user-defined parameters and targets

Parameter	value
Total number of board layers	24
Number of signal layers	10
Total stack-up height	160 mils
Stripline thickness	1.3 mils
Ground layer thickness	1.3 mils
SolderMask thickness	0.5 mils
Trace spacing (***S***)	5 – 7 mils
Desired differential impedance	100 Ohm
Impedance error	≤ 1 Ohm
Insertion loss	≥ -1.2 dB/inch
FEXT	≤ -60 dB

Output: optimized design
Layer types and dielectric thicknesses
Recommended W, S, D per signal layer
Impedance, loss, and FEXT
subject to user-defined constraints

Runtime advantage
Conventional search grows with variables
The proposed engine responds in seconds

Complete stack-up optimization



Optimization time
Proposed: **15 s**
NSGA-II: **44 min**

Complete multilayer optimization in seconds

layer	Layer name	Thickness (mil)	W, S, D (mil)	Z(Ω)	Loss (dB/inch)	FEXT (dB)
1	GND	1.3				
	PP	3				
2	INNER1	1.3	3.37, 6.70, 15.71	99.76	-1.19	-78.29
	Core	5				
3	GND	1.3				
	PP	20				
4	GND	1.3				
	Core	4				
5	INNER2	1.3	3.34, 6.00, 10.86	99.94	-1.19	-67.55
	PP	5				
6	GND	1.3				
	Core	5				
7	INNER3	1.3	3.35, 5.60, 10.86	99.76	-1.18	-66.30
	PP	5				
8	GND	1.3				
	Core	4.5				
9	INNER4	1.3	3.54, 6.85, 10.86	99.90	-1.17	-66.19
	PP	4				
10	GND	1.3				
	Core	4				
11	INNER5	1.3	3.47, 7.00, 10.86	99.94	-1.19	-67.16
	PP	4				
12	GND	1.3				
	Core	3				
13	GND	1.3				
	PP	4				
14	INNER6	1.3	3.47, 7.00, 10.86	99.94	-1.19	-67.16
	Core	4				
15	GND	1.3				
	PP	4				
16	INNER7	1.3	3.54, 6.85, 10.86	99.90	-1.17	-66.19
	Core	4.5				
17	GND	1.3				
	PP	5				
18	INNER8	1.3	3.35, 5.60, 10.86	99.76	-1.18	-66.30
	Core	5				
19	GND	1.3				
	PP	5				
20	INNER9	1.3	3.34, 6.00, 10.86	99.94	-1.19	-67.55
	Core	4				
21	GND	1.3				
	PP	20				
22	GND	1.3				
	Core	5				
23	INNER10	1.3	3.37, 6.70, 15.71	99.76	-1.19	-78.29
	PP	3				
24	GND	1.3				

Conclusions and Future Work

Conclusions

Transformer-driven modeling and multi-objective optimization **in seconds**
Variables: trace width W, trace spacing S, and pair distance D
Objectives: characteristic impedance, insertion loss, and FEXT
The method **maintains accuracy** while improving efficiency over NSGA-II
24-layer example: **15 s versus 44 min** for NSGA-II

Future work

Generalization across stripline designs and extension to microstrip structures
Direct optimization of **S-parameters or eye diagrams** using machine learning
Integration into chip signal-integrity **EDA tools**

Thank You

Questions and Discussion

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