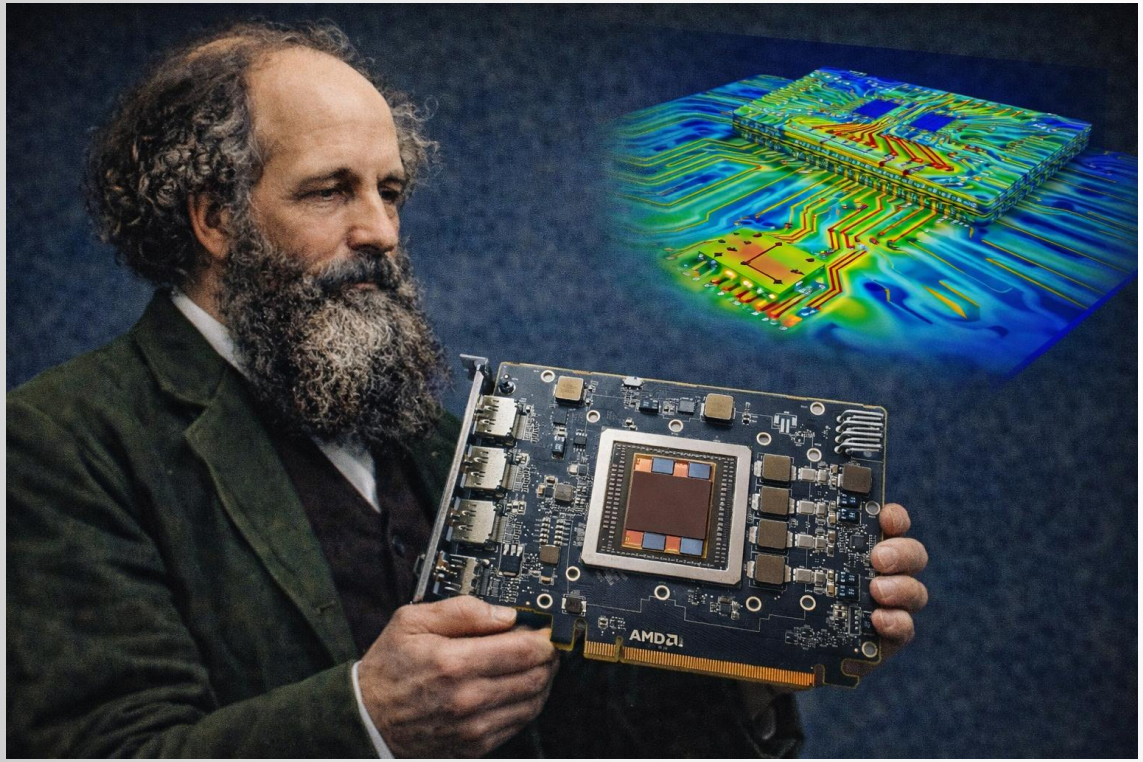
Automating the Bridge From EM Modeling to Circuit-Level SIPI Sign-off

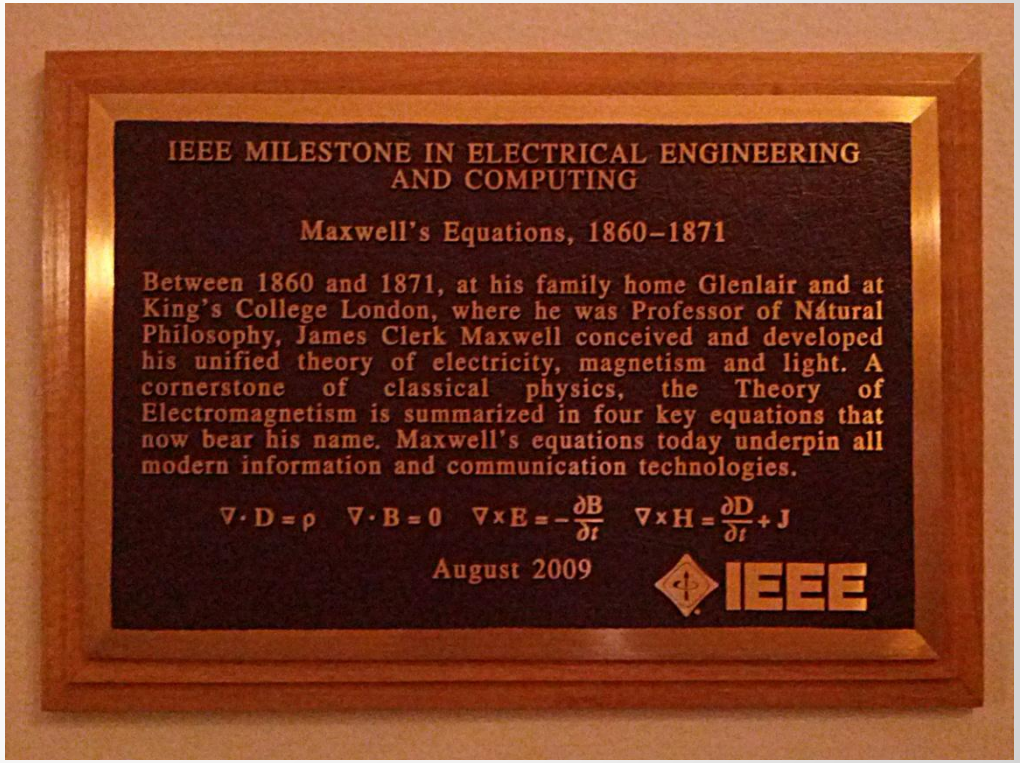
Hiroshi Matsuda, Hiroshi Ishikawa
Ji Zheng, Raj Raghuram
Aurora System Inc.

Hybrid Asian IBIS Summit – Japan, 2026
November 10, 2026

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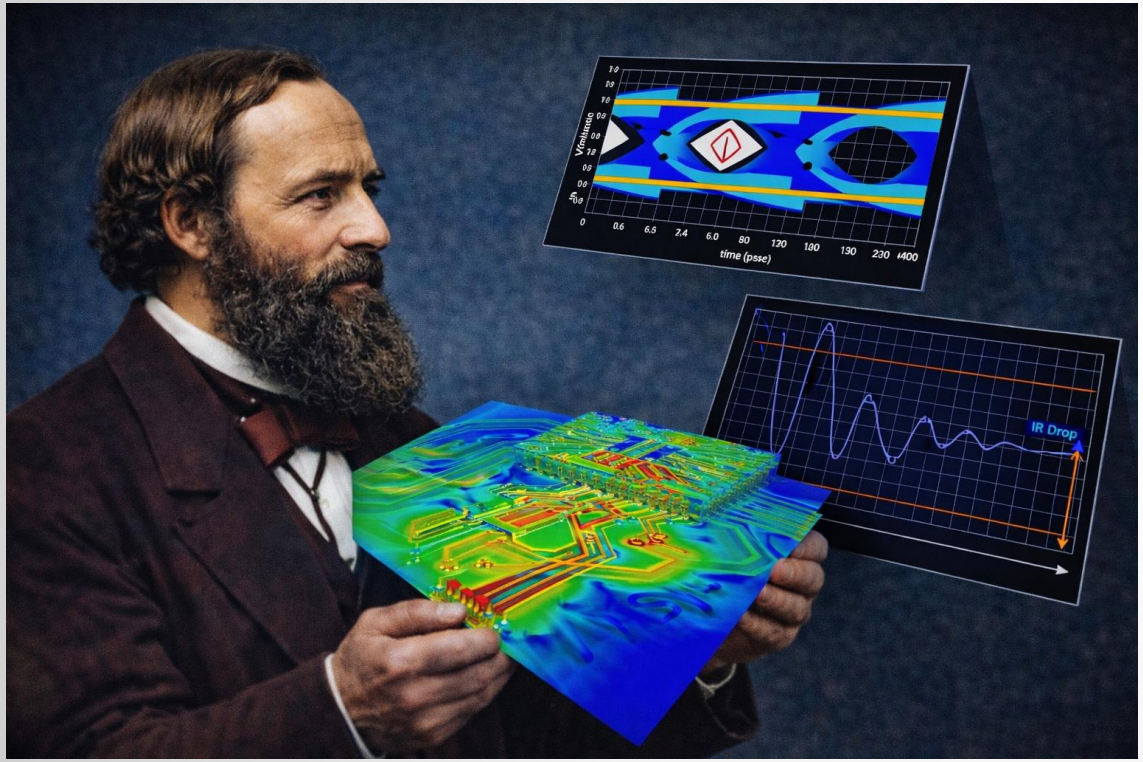
EM Modeling





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Circuit Simulation with EM Models





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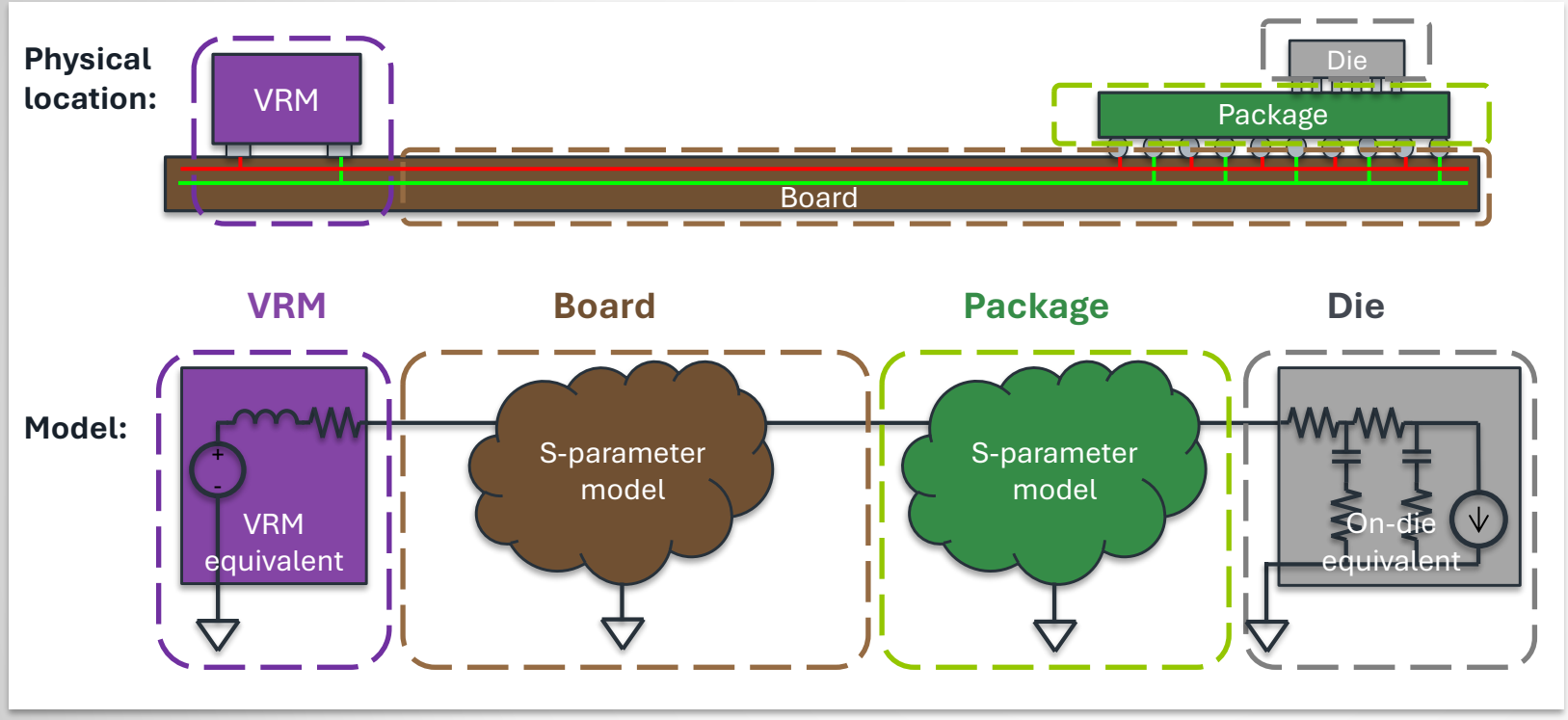
Introduction

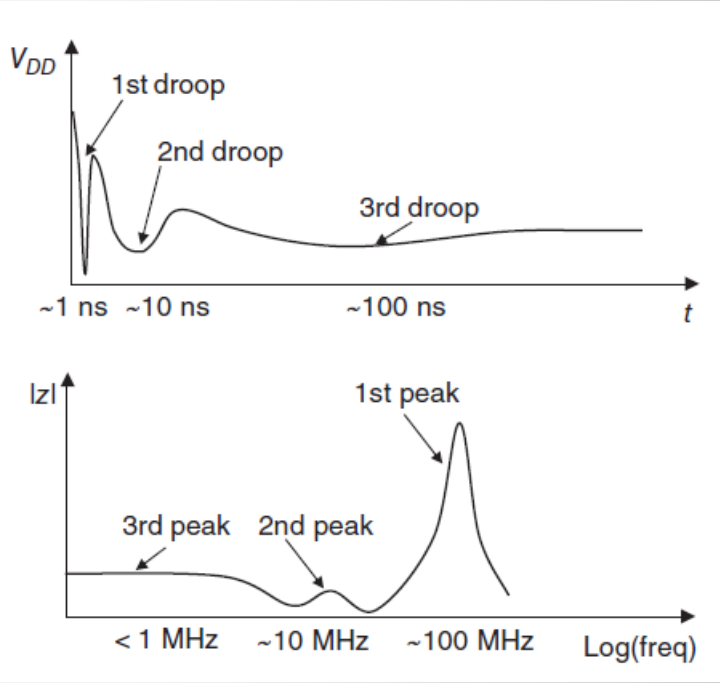
- Modern SI/PI flows rely on **EM extraction + circuit simulation**
- Engineers often assume **EM results are “plug-and-play”**
- In reality:
  - EM solvers and circuit simulators are based on **different physical assumptions**
  - Mismatches cause:
    - Wrong impedance, delay
    - Non-physical resonances
    - DC errors
    - Simulation instability
- Understanding these gaps prevents **model misuse**

Where the Gaps Are

- Ground node vs “0”
- DC and low frequency behavior
- S-parameter simulation
- Port vs. node, physics vs. abstraction
- And more ……

PDN End-To-End Simulation





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Die Model/CPM Ground

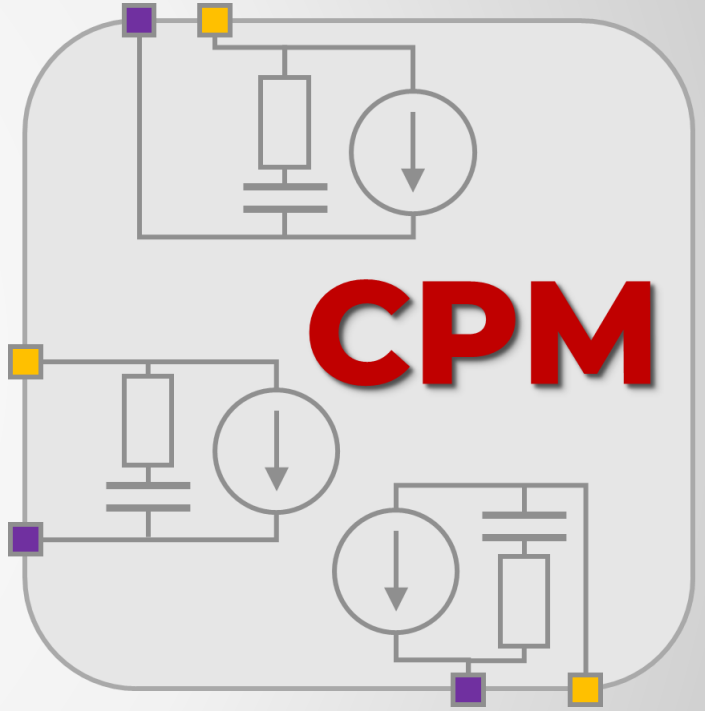
- The CPM ground net ”VSS” node is not SPICE “0” or “GND”

```
.SUBCKT PowerModel PAR_0_0_DVDD_DDTOP PAR_0_0_DVDD_PROC_B
…… PAR_0_0_DVSS
```

- The CPM can have “0” in the netlist depending on the options

```
* CPM Options:
* perform powermodel -nx 1 -ny 1 -no_afs -noglobal_gnd -repeat_current best -plocnames
```

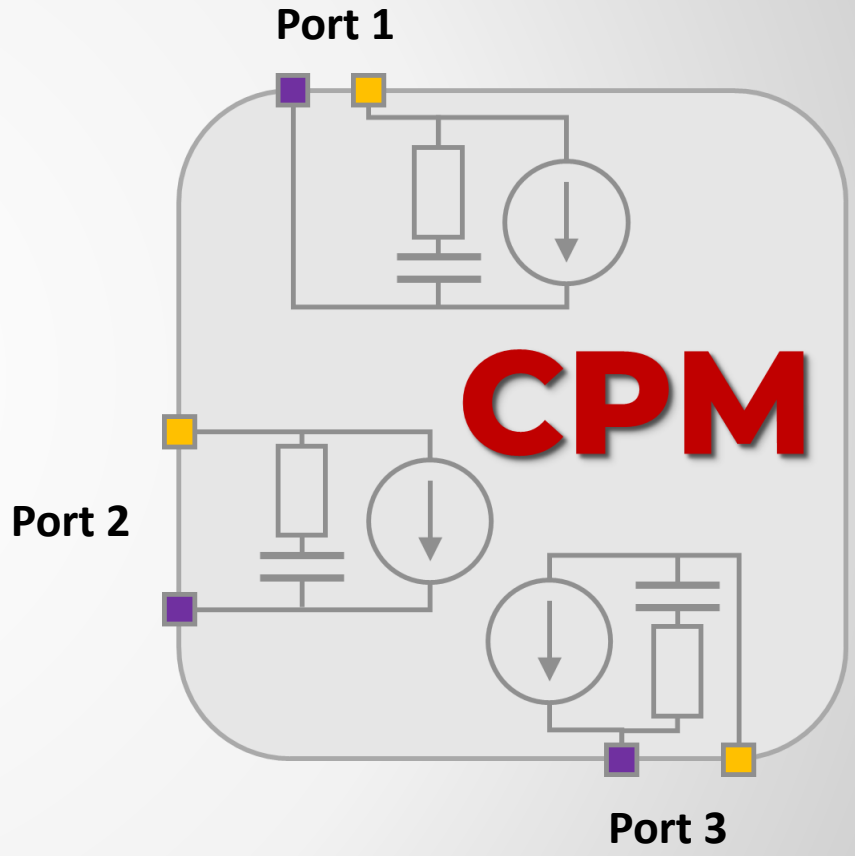
https://www.synopsys.com/implementation-and-signoff/signoff/redhawk-sc.html#6



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Bridge the “GND” Gap

- Transform node-based CPM to port-based CPM S-parameter model
- Connect transformed CPM to package and PCB S-parameters

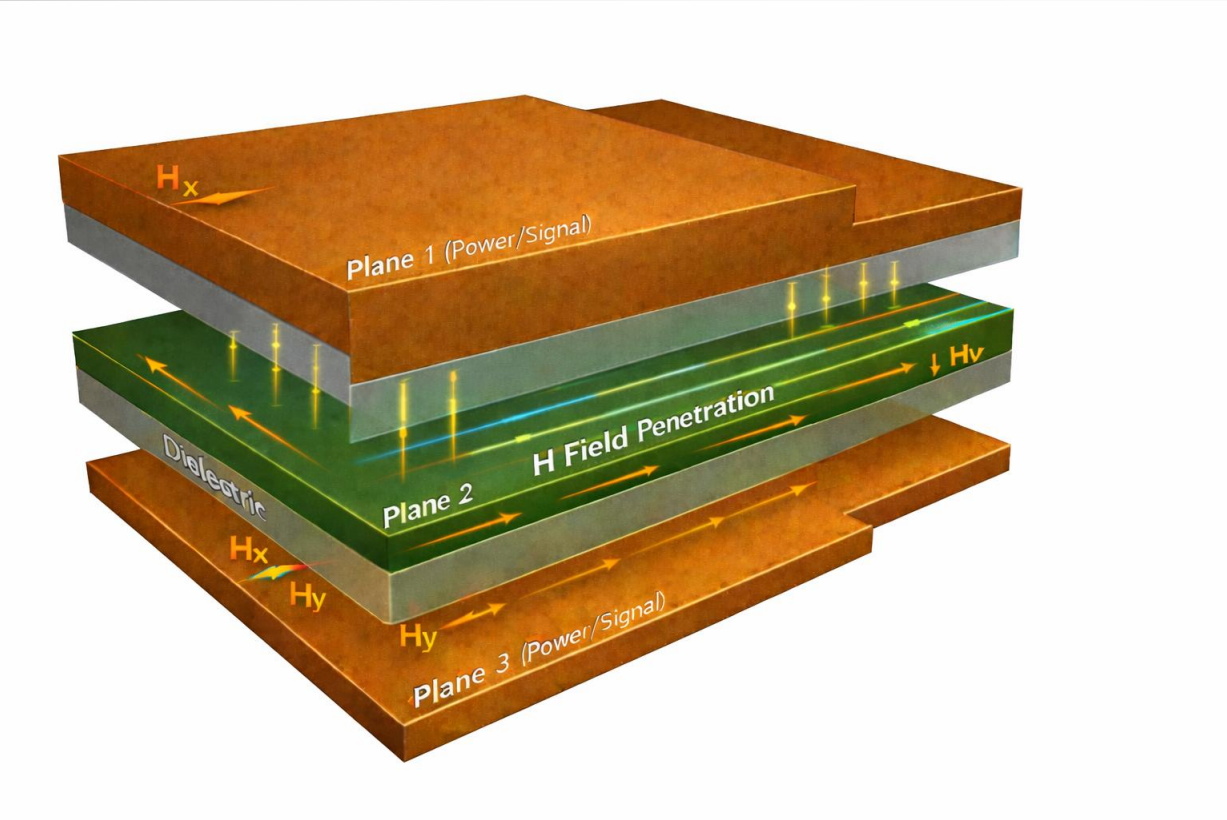


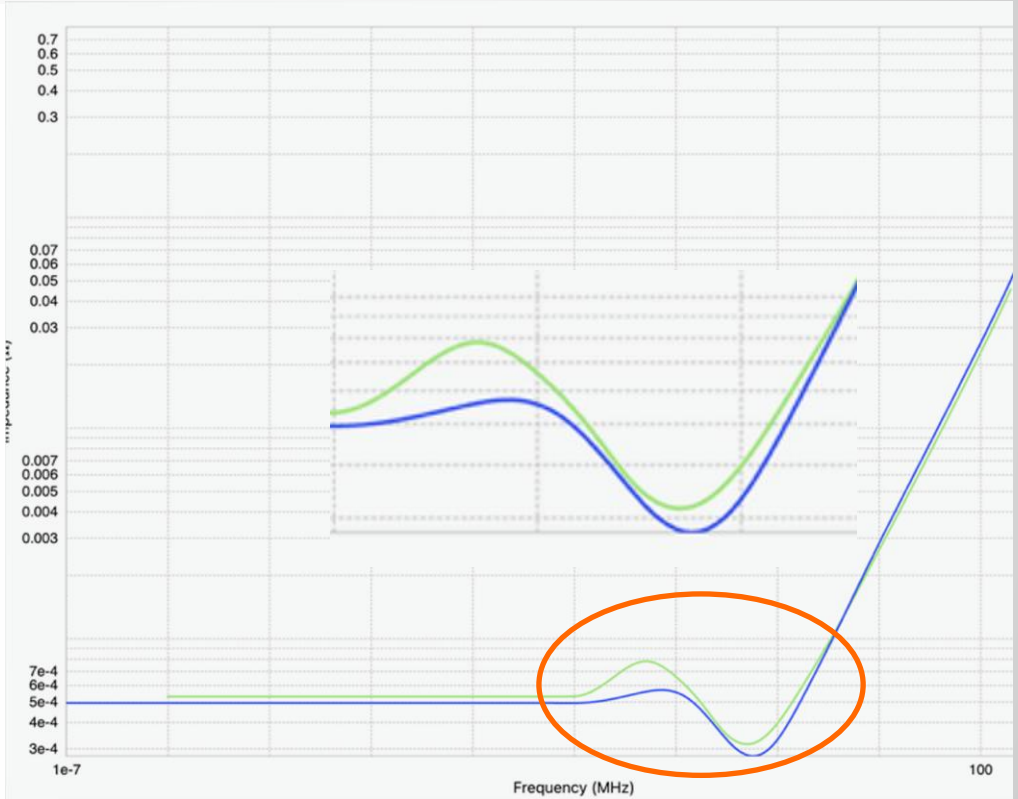
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DC / Low Frequency Gap

- Electric and magnetic fields **decouple**
- Terms involving ω vanish
- System matrix becomes **ill-conditioned**
- Small numerical errors dominate

Low Frequency Challenge in Hybrid EM Solver





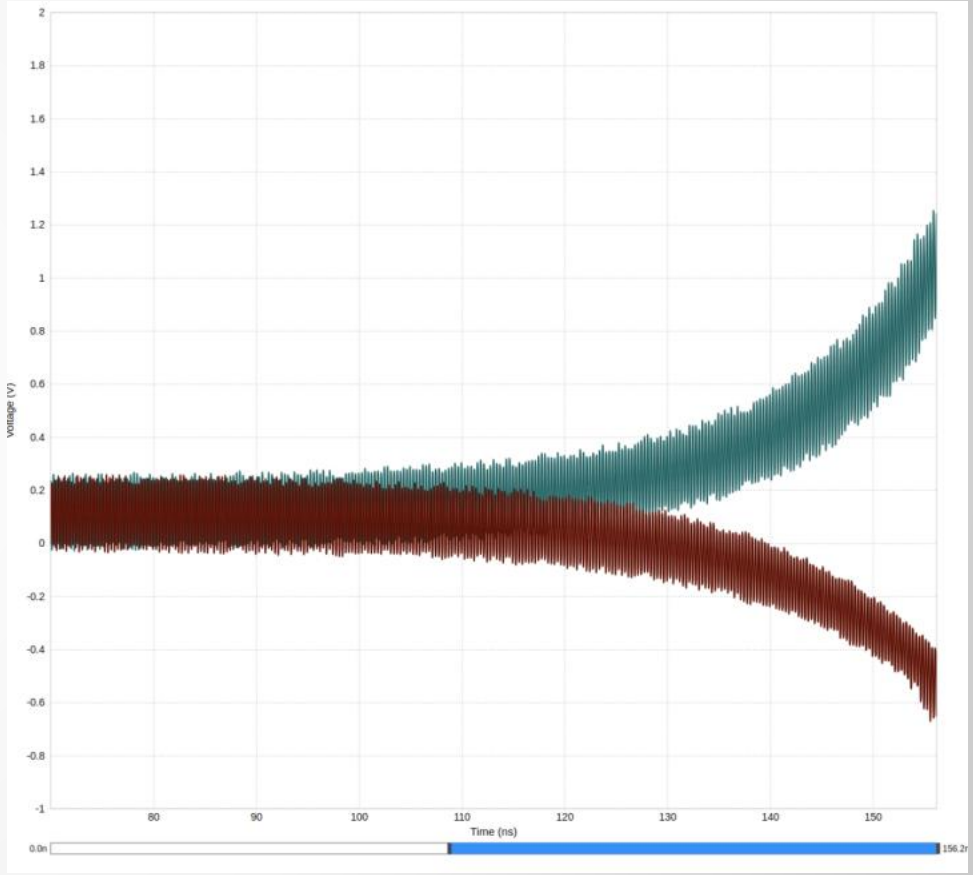
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Bridge the DC / Low Frequency Gap

- DC
  - Dedicated DC solution with static EM solver
- Low Frequency (1KHz ~ 1MHz)
  - Account for “Interplane” or “Intraplane” coupling
  - Approximation using DC point and higher frequency response through rational fitting and explicit constraints

Bridge the S-Parameter vs Time Domain Gap

- Limited bandwidth
- Passivity violations
- Scalability for larger number of ports
- Lack of physical insights such as delay etc.
- Causality violations



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Macro-Modeling/Fitting and Passivity

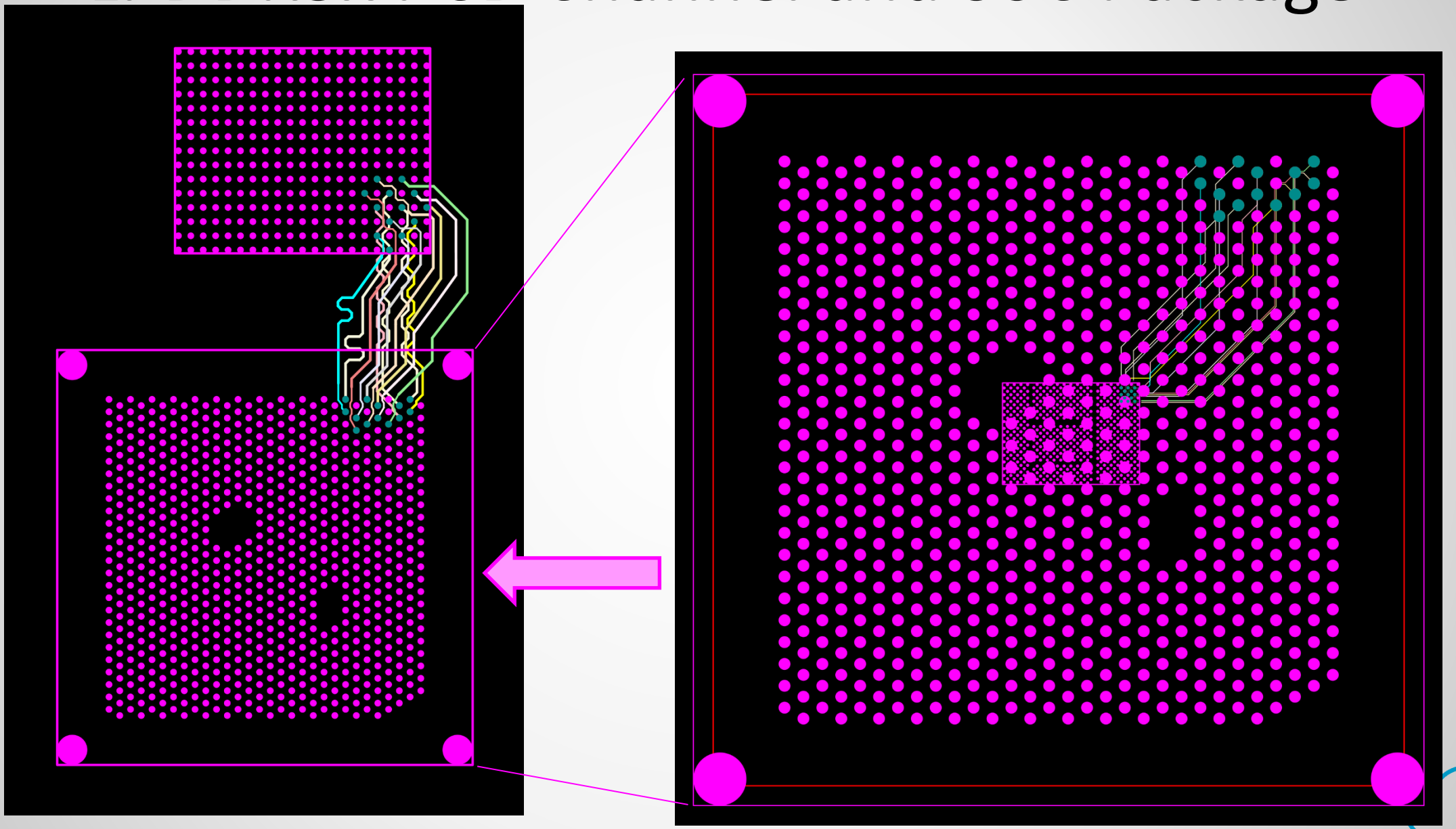
- Vector Fitting scales well
- Passivity enforcement is the bottleneck
- 150 ~ 200 port is the current practical limitation
- Possible side-effects of passivity enforcement
  - DC accuracy
  - Delay distortion

Application Example: LPDDR5

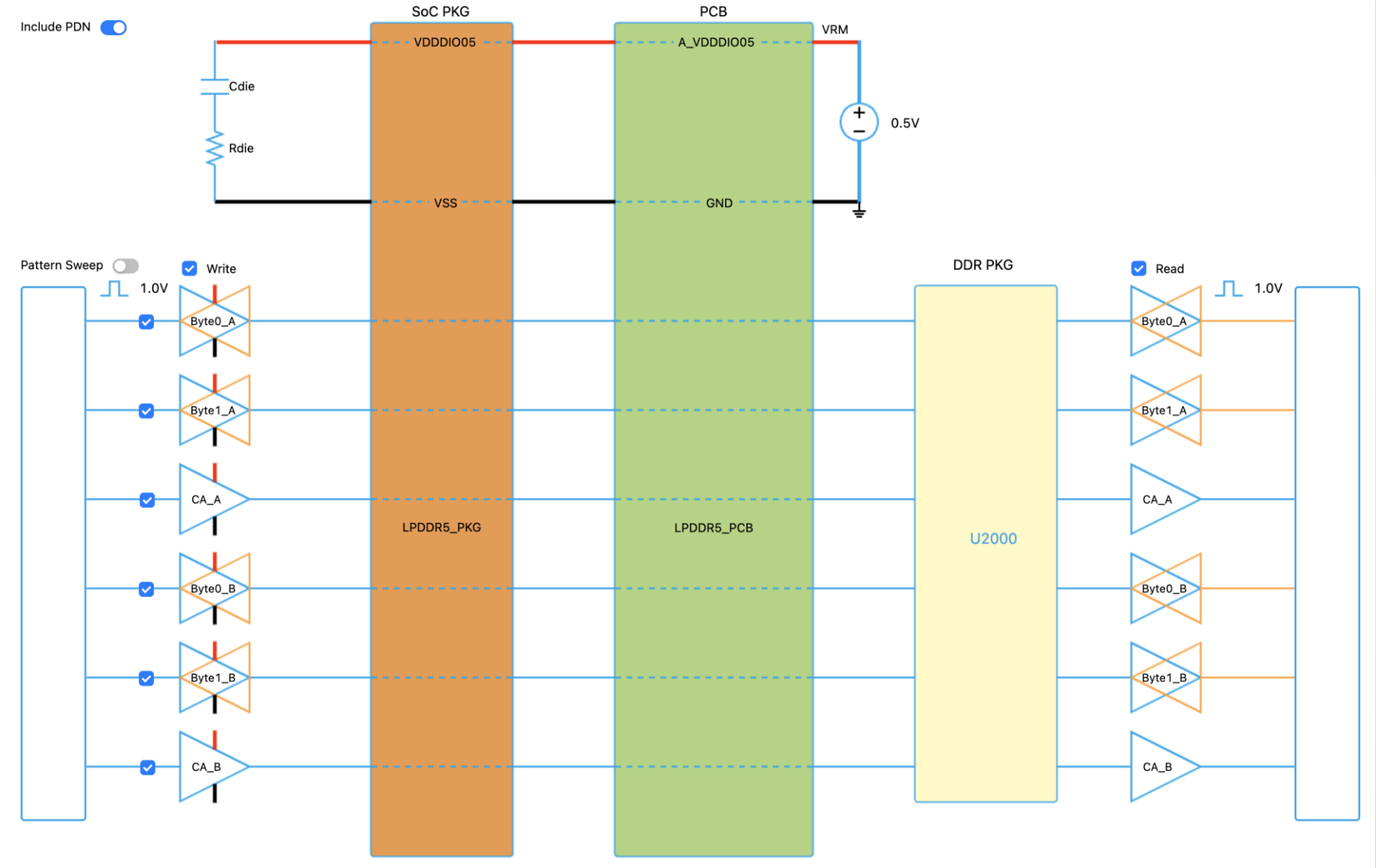
Bridging the gaps with automated flow using EM solver and circuit simulator

IBIS-AMI simulation

LPDDR5x PCB Channel and SoC Package

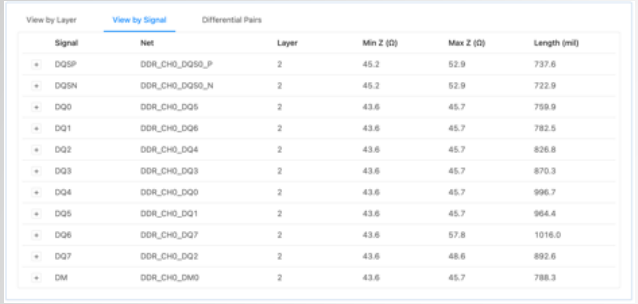


Automated SI Simulation flow with IBIS-AMI



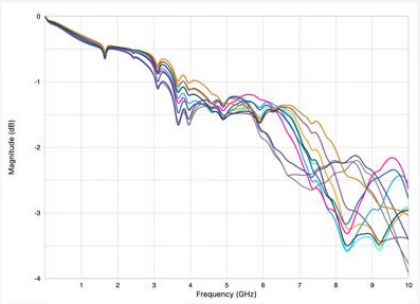
Aurora System

Results

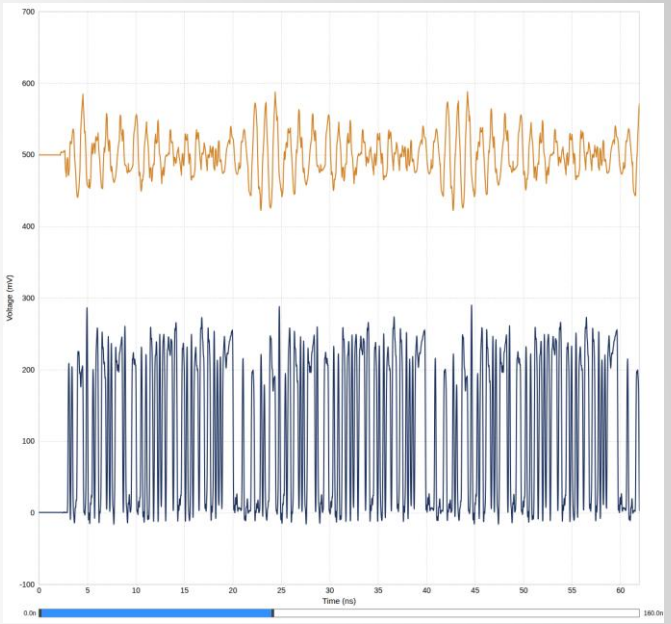

View by Layer | View by Signal | Differential Pairs

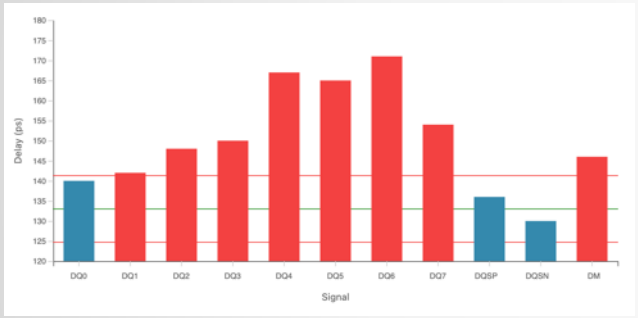
Signal	Net	Layer	Min Z (Ω)	Max Z (Ω)	Length (mil)
DQSP	DDR_CH0_DQS0_P	2	45.2	52.9	737.6
DQSN	DDR_CH0_DQS0_N	2	45.2	52.9	722.9
DQ0	DDR_CH0_DQ5	2	43.6	45.7	759.9
DQ1	DDR_CH0_DQ6	2	43.6	45.7	782.5
DQ2	DDR_CH0_DQ4	2	43.6	45.7	826.8
DQ3	DDR_CH0_DQ3	2	43.6	45.7	870.3
DQ4	DDR_CH0_DQ0	2	43.6	45.7	996.7
DQ5	DDR_CH0_DQ1	2	43.6	45.7	964.4
DQ6	DDR_CH0_DQ7	2	43.6	57.8	1016.0
DQ7	DDR_CH0_DQ2	2	43.6	48.6	892.6
DM	DDR_CH0_DM0	2	43.6	45.7	788.3

Characteristic Impedance

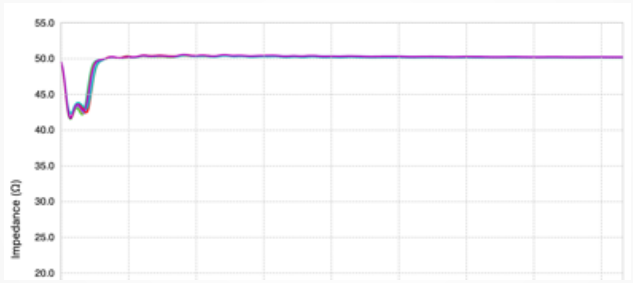


Channel S-parameters

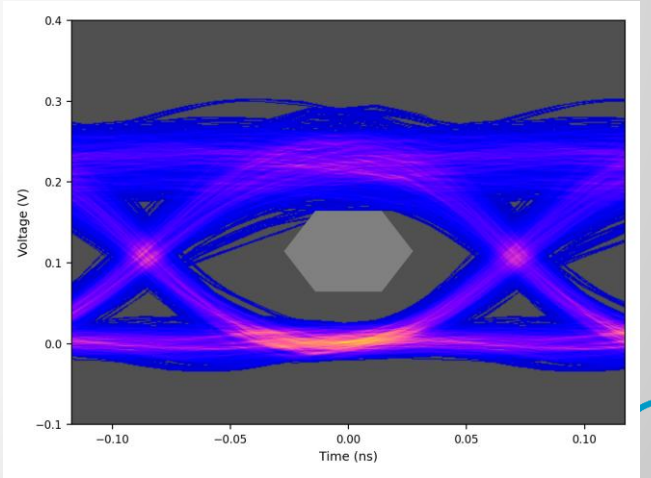


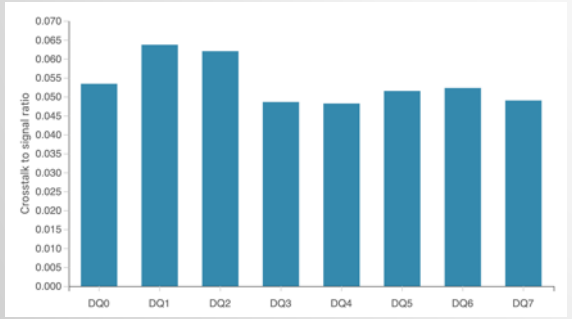


Delay and skew

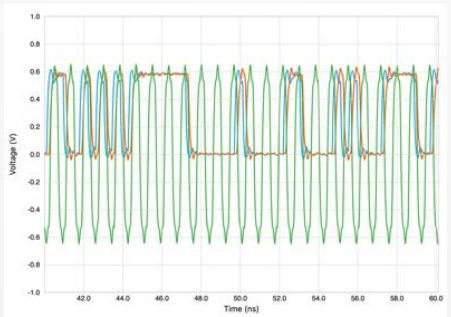


TDR





Crosstalk

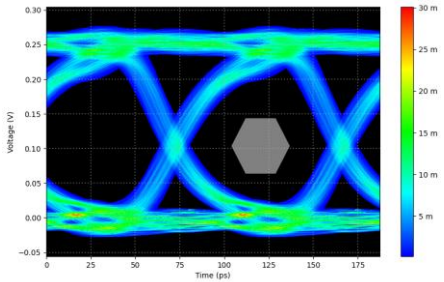


Transient voltage waveform

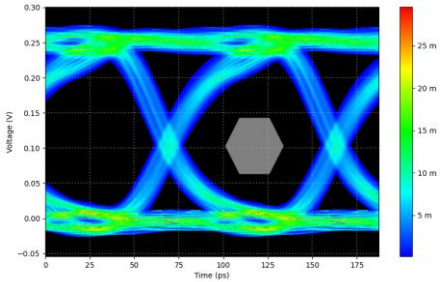
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LPDDR5 Compliance Report

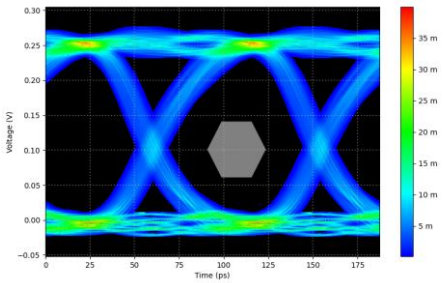
DQ8A



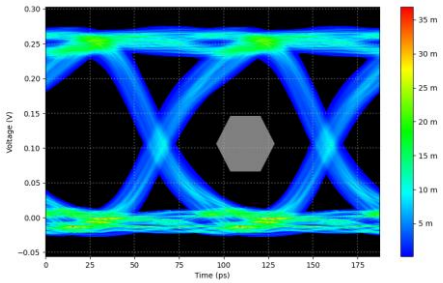
DQ9A



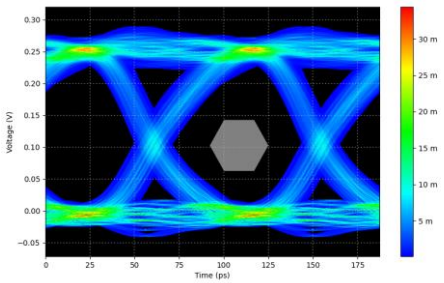
DQ10A



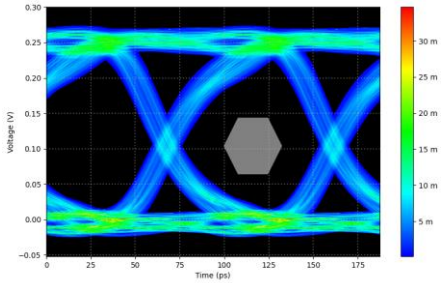
DQ11A



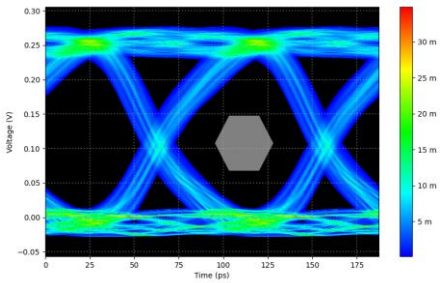
DQ12A



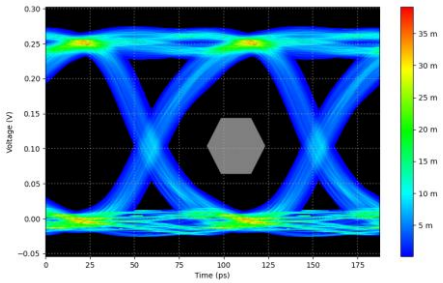
DQ13A



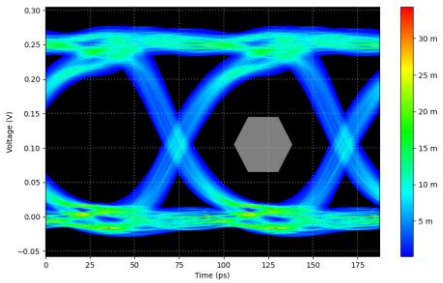
DQ14A



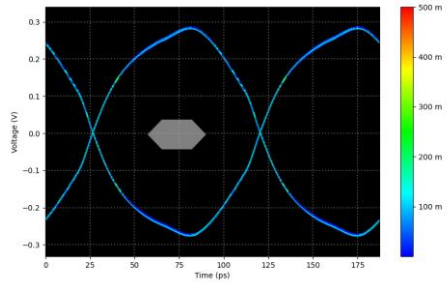
DQ15A



DM1A



WCK1A



Tolerance: 1e-20

	DQ8A	DQ9A	DQ10A	DQ11A	DQ12A	DQ13A	DQ14A	DQ15A	DM1A	WCK1A	Min	Max
Eye Width (ps)	77.8	78.2	76.1	76.7	72.8	77.6	75.0	75.9	77.6	93.8	72.8	78.2
Eye Height (mV)	193.5	207.7	223.9	216.5	213.3	211.8	217.2	220.1	189.4	551.7	189.4	223.9
Jitter (ps)	16.5	16.1	17.8	18.2	21.0	16.3	19.7	18.9	16.9	0.0	16.1	21.0
Top Margin (mV)	48.8	51.0	63.0	50.3	56.4	47.5	49.7	58.6	51.5	204.9	47.5	63.0
Bottom Margin (mV)	37.3	39.7	45.1	46.0	43.1	38.4	46.8	44.3	43.5	204.9	37.3	46.8
Setup Margin (ps)	21.4	21.7	21.3	20.8	18.8	21.4	19.4	21.6	21.6	30.7	18.8	21.7
Hold Margin (ps)	21.1	21.4	21.2	20.2	18.9	21.3	18.9	20.2	20.9	30.3	18.9	21.4

Summary

EM-to-Circuit Modeling Gaps:

- Ground node vs “0”
- DC and low frequency behavior
- S-parameter simulation
- Port vs. node, physics vs. abstraction

Understanding these gaps will achieve more accurate results.

High affinity with the automated flow.

Reference

Automating the Bridge From EM Modeling to Circuit-Level SIPI Sign-off

Ji Zheng, Raj Raghuram

Aurora System Inc.

Synopsys 2026 Signal & Power Integrity (SIPI) SIG Event

February 25, 2026