IBIS modeling of DDR2 in conjunction with linear channel analysis



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## **Overview**

- High performance source synchronous buses, including DDR2 are known to be susceptible to resonances
  - **—** Established solution is to add compensation capacitors
- It is difficult to demonstrate these resonances in traditional time domain SI simulators
  - Resonance only occurs with specific repeated bit sequences
- Linear channel analysis can identify the resonances but has limitations in its ability to determine if they are harmful
  - DDR2 drivers exhibit non-linearity's which may affect characteristics such as overshoot
- This paper describes the early results of our analysis of resonances in DDR2 buses using of both tradition circuit simulation using IBIS 4.2 models and linear channel analysis





# **Analysis Steps**

- 1. Extract DDR2 Address net from layout
  - **Example has motherboard, 2 DDR2 modules and connectors**
- 2. Measure pulse response of the net using standard circuit simulation
  - **IBIS 4.2 driver and receiver models**
  - Simulating multiple pulses allows the degree of non-linearity to be determined
- 3. Linear channel analysis
  - Determine worst case bit sequence
  - Create eye diagram with linearized drivers and receivers
- 4. **Standard circuit simulation using worst case bit sequence** 
  - Create eye diagram without linearization





### 1. DDR2 address net extracted from layout



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GREAR



# 2. Full non-linear simulation to establish pulse response



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## **3. Linear Channel Analysis**



#### Eye Diagram



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### 4. Full Non-linear simulation using Worst Case Stimulus



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### **Further Work**

- This paper is based on the early results of this investigation into resonances on DDR2 buses
- We plan to further examine the detailed affects of channel layouts, connector characteristics and the optimization of compensation capacitors





