CYBERNET SYSTEMS CO., LTD.

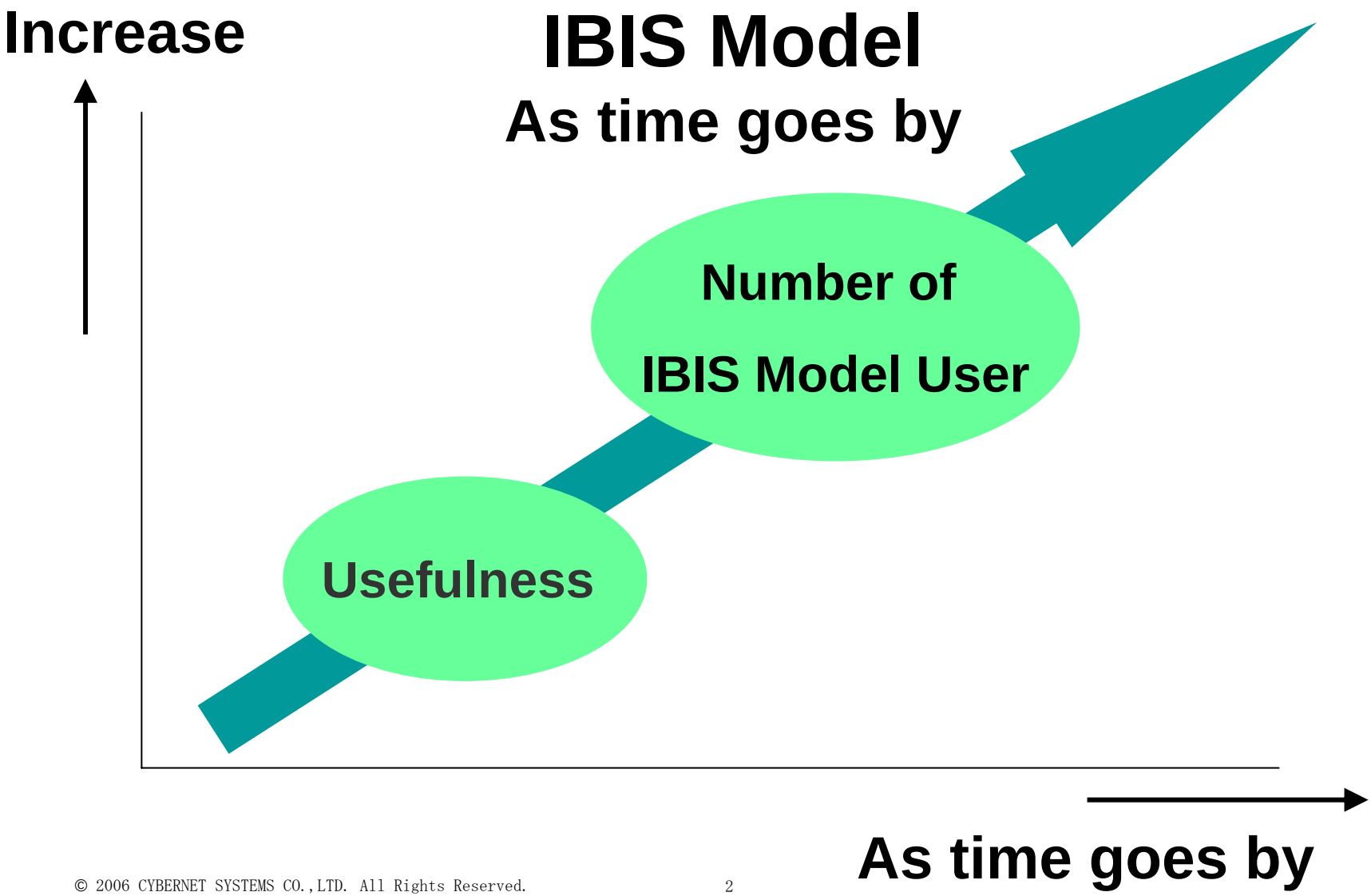
IBIS Model Engineering for SI Simulation

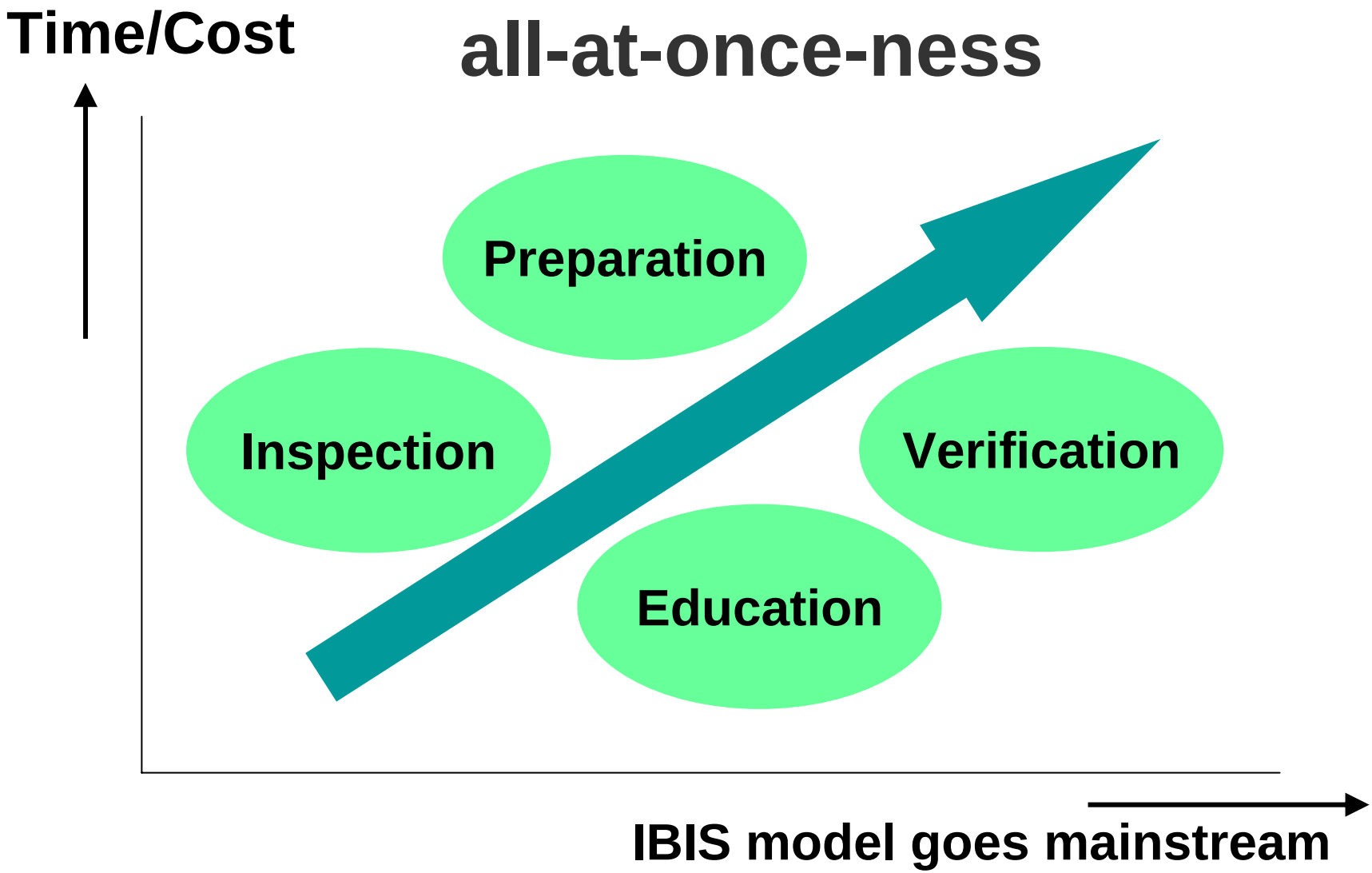
Asian IBIS Summit (CHINA), October 27, 2006

Kazuhiko Kusunoki
k-kusu@cybernet.co.jp

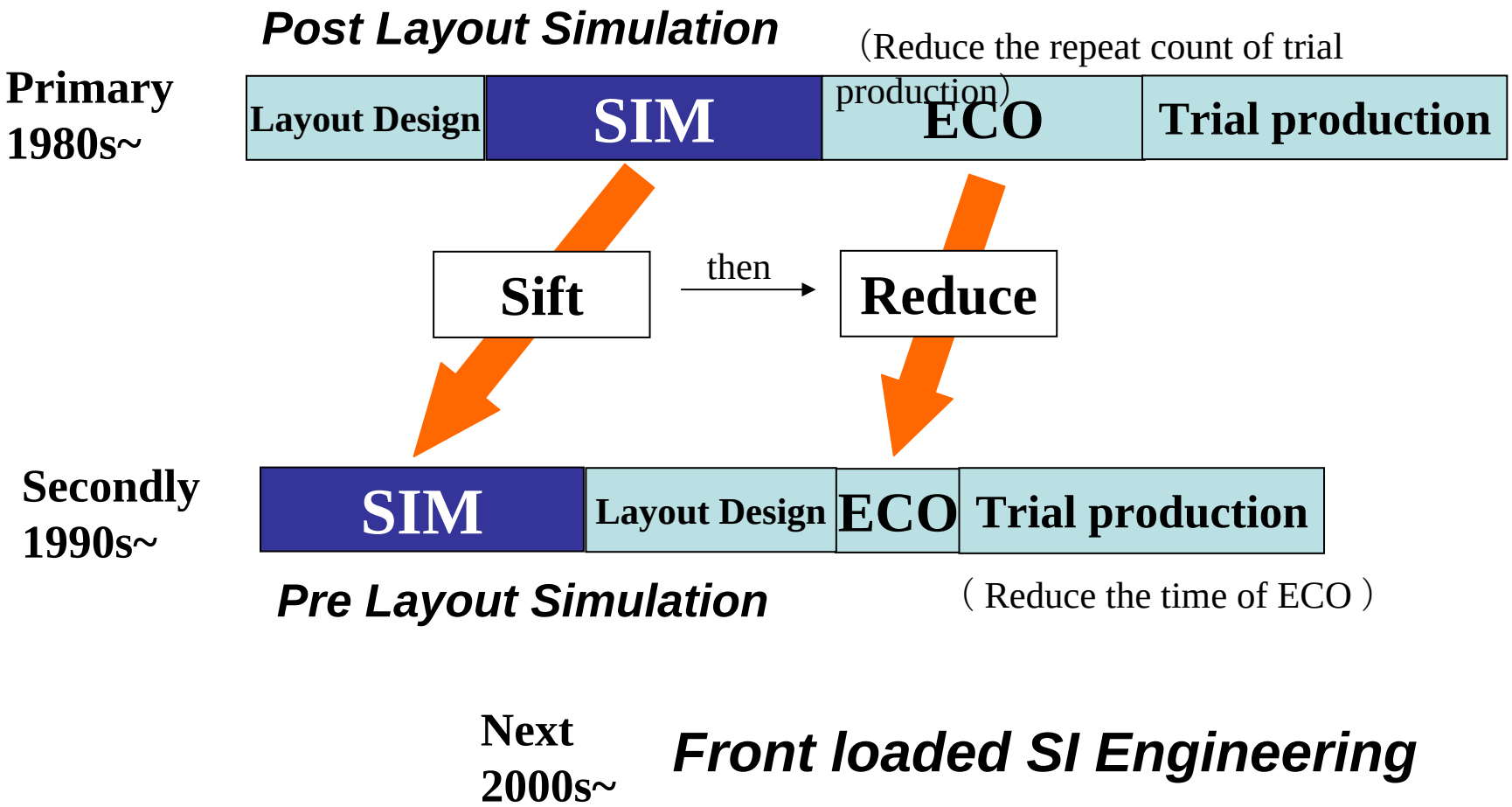
IBIS Model

As time goes by

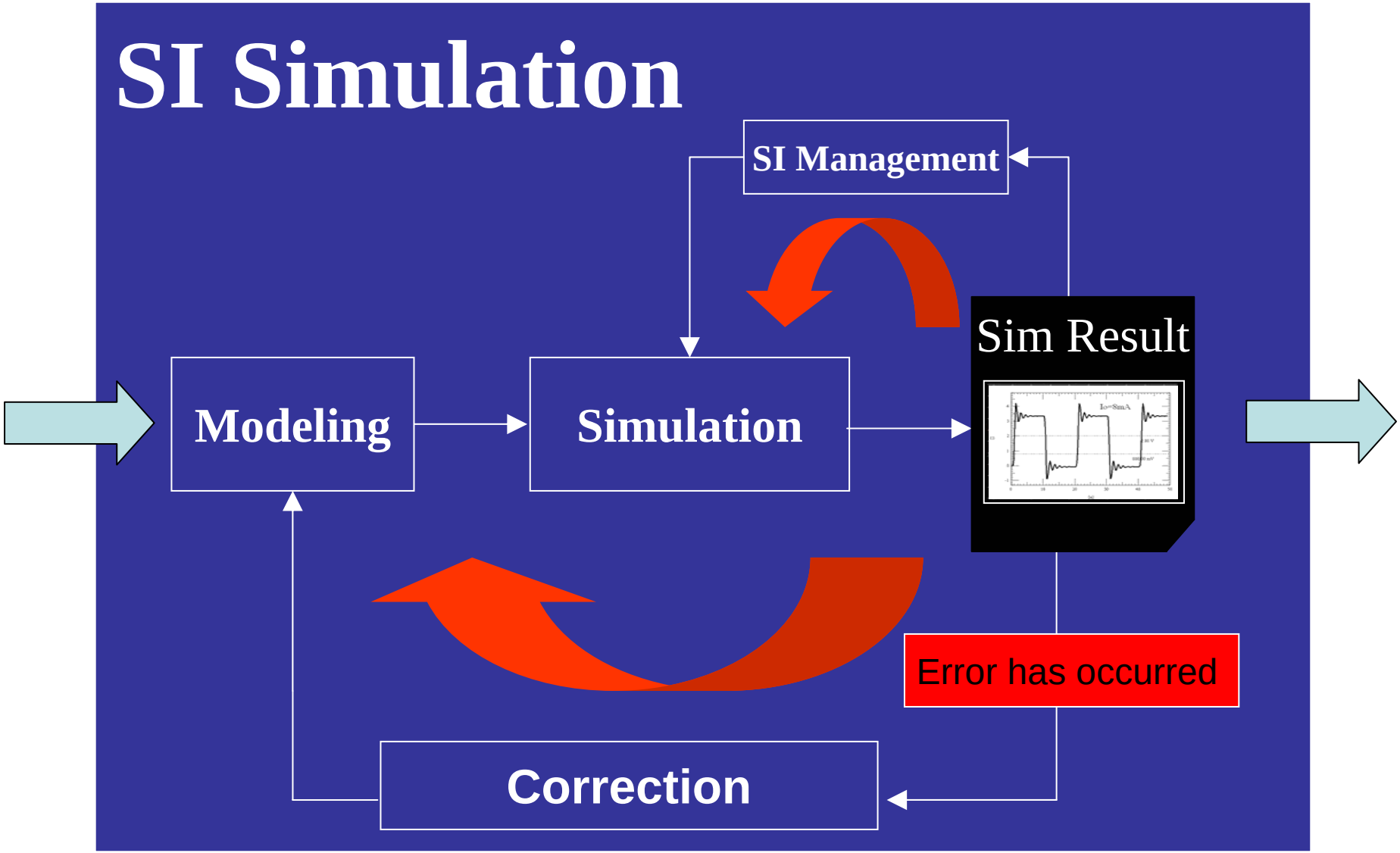




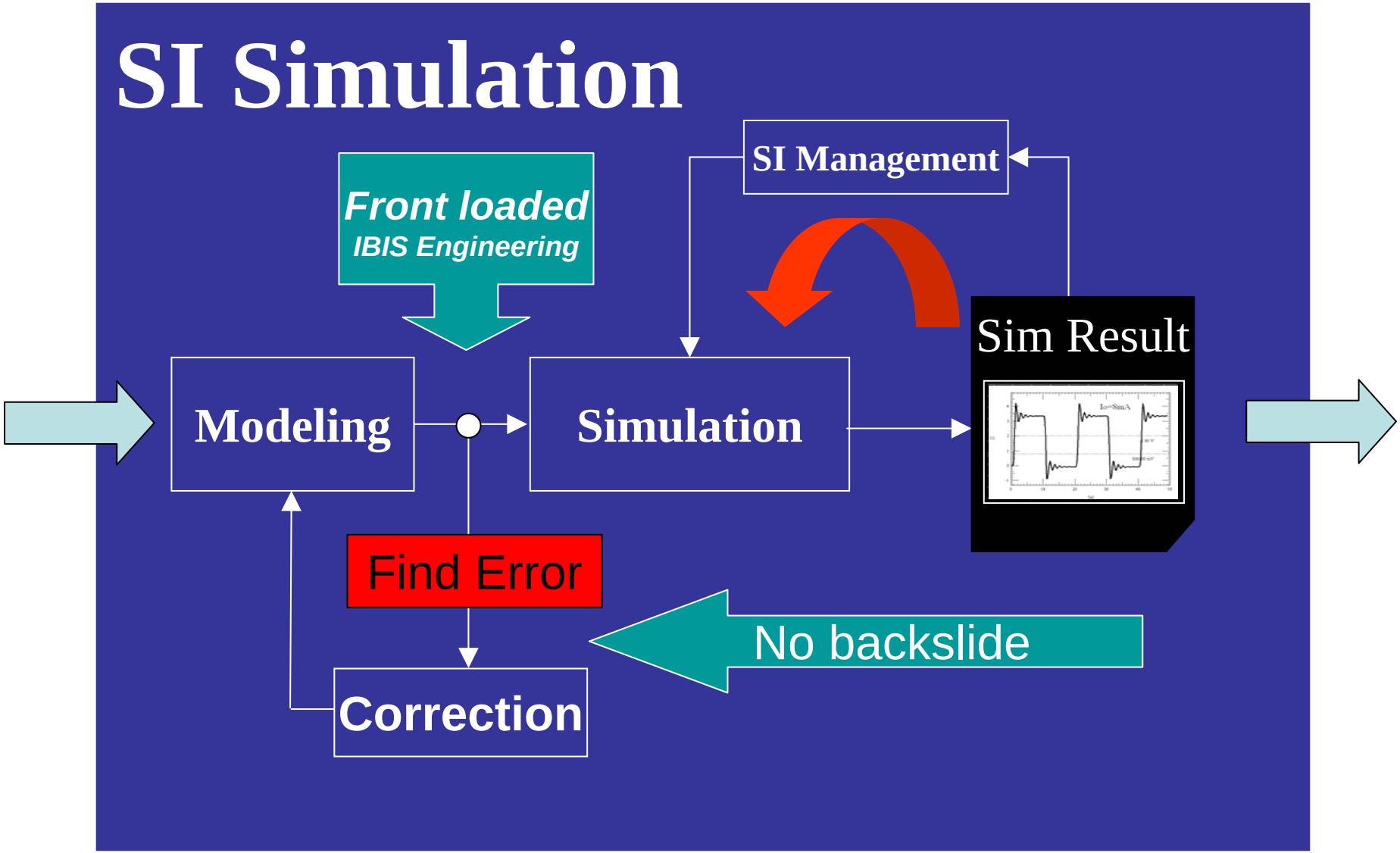
Challenge to the SI simulation Engineering of PCB Design



SI Simulation



SI Simulation



IBIS model Engineering as Front loaded SI Engineering

To minimized the time of SI simulation

Modeling	SIM

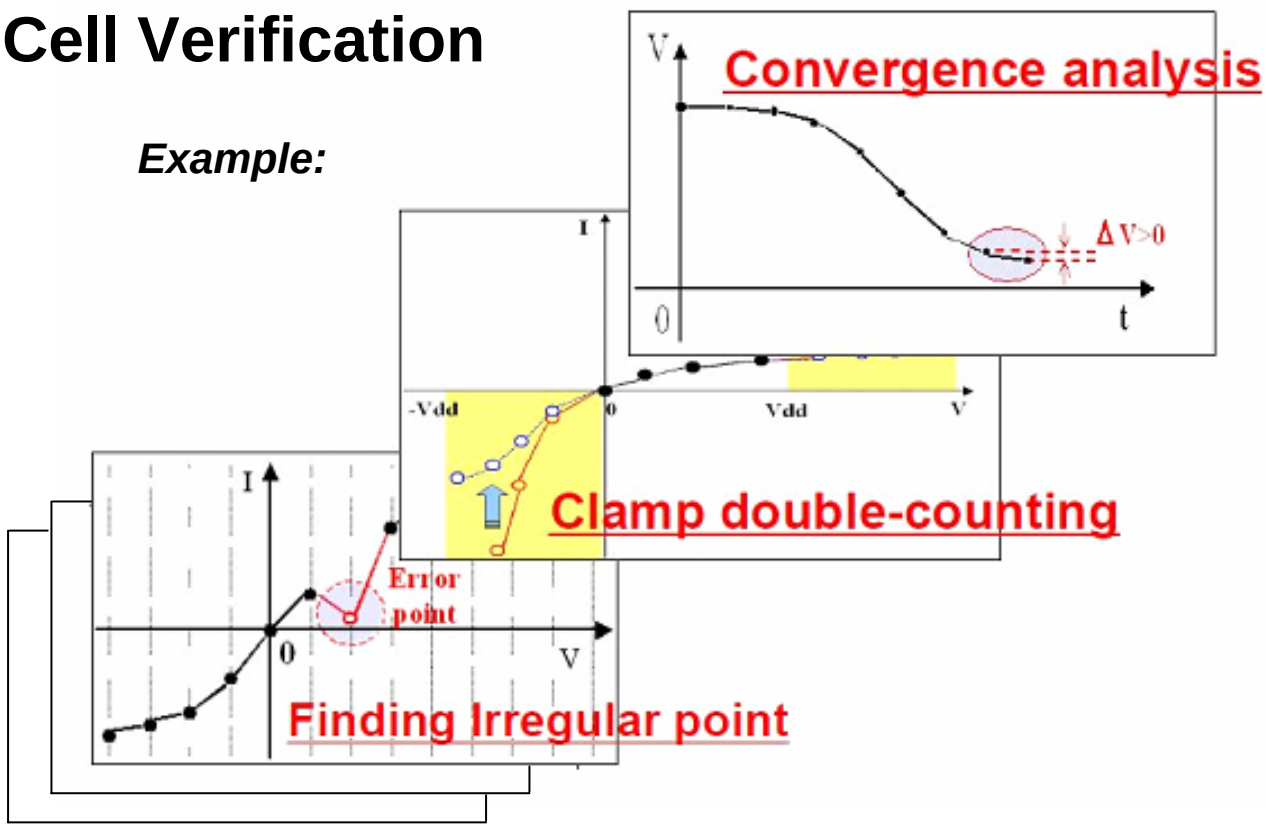
- •Incoming inspection for IBIS Model
  - •Check IBIS Model
  - •Verification IBIS Model
  - •Correction IBIS Model
- •Prepare IBIS Model
- •Tune IBIS Model

Make decisions on SI view

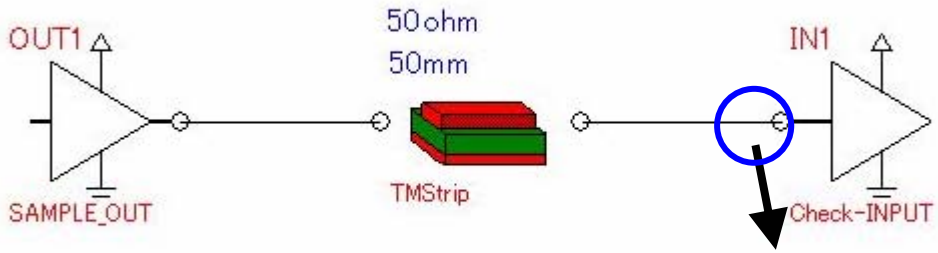
Incoming inspection for IBIS Model

- **Syntax Check**
- **I/O Cell Verification**

Example:



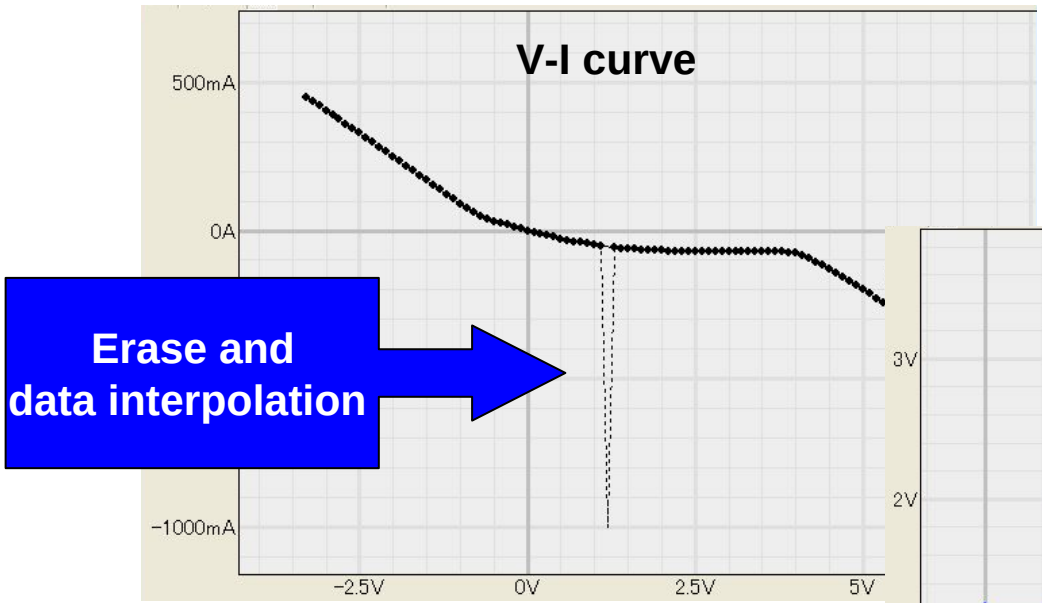
•Verification IBIS Model



Test circuit for IBIS Verification

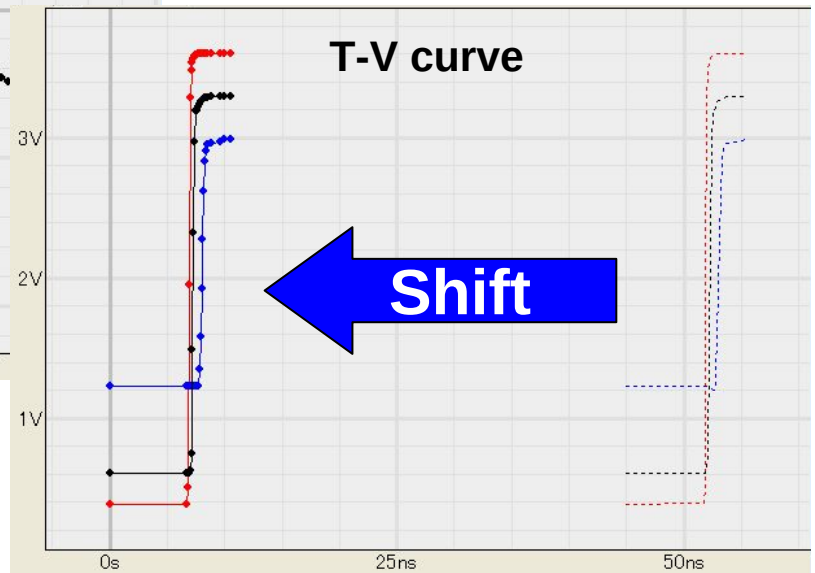
Example:

•Correction IBIS Model



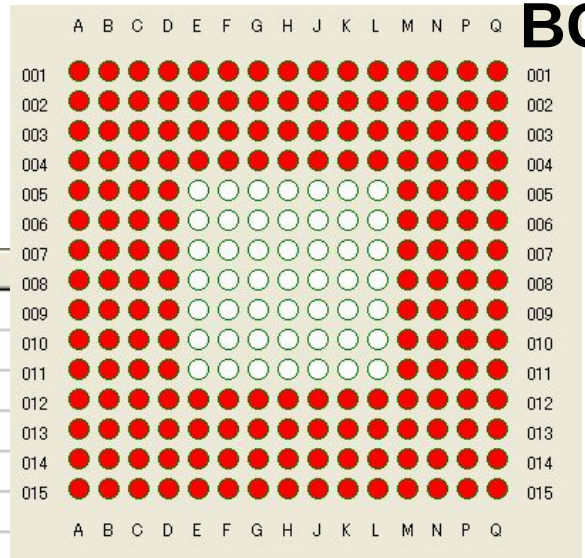
Erase and data interpolation

Example:



Shift

•Prepare IBIS Model



BGA

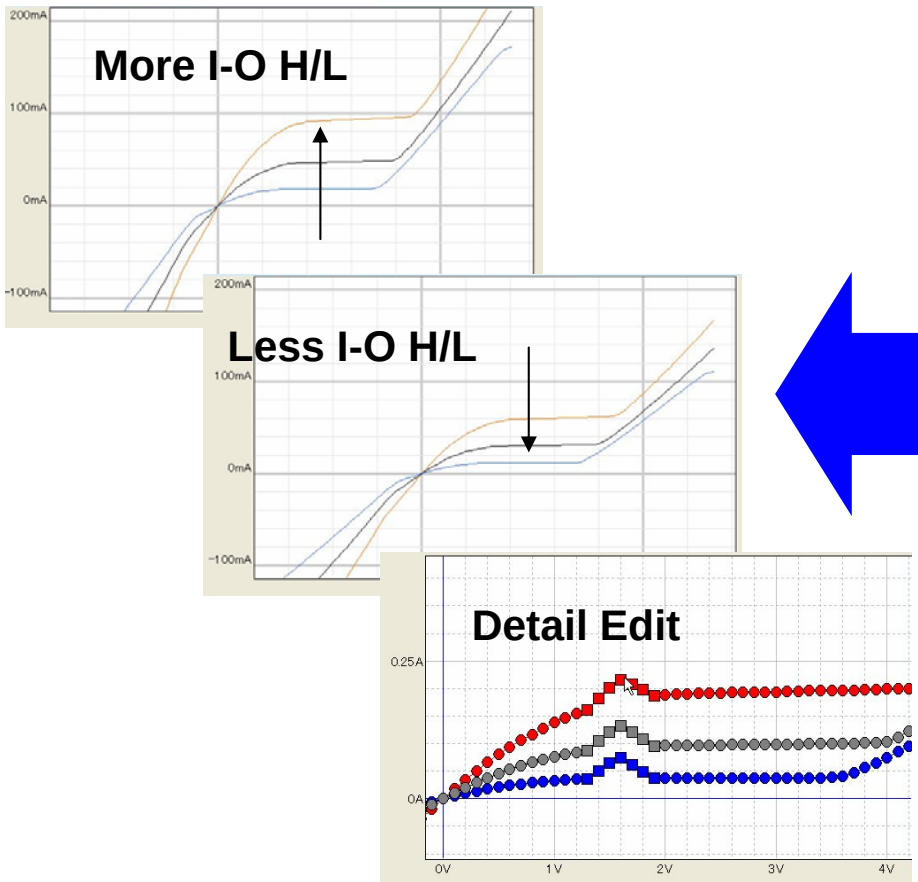
Pin/Signal/Model Assign

Pin#	Signal	Model	R_pin	L_pin
A001				
A002		EDA77244A_IN		
A003		EDA77244A_IN		
A004		EDA77244A_IN		
A005		EDA77244A_IN		
A006		EDA77244A_IN		
A007		EDA77244A_IN		
A008		GND		
A009		POWER		
A010		NC		
A011		EDA77244A_OUT		
A012		EDA77244A_OUT		
A013		EDA77244A_OUT		
A014		EDA77244A_OUT		
A015		EDA77244A_OUT		
B001		EDA77244A_OUT		
B002				
B003				

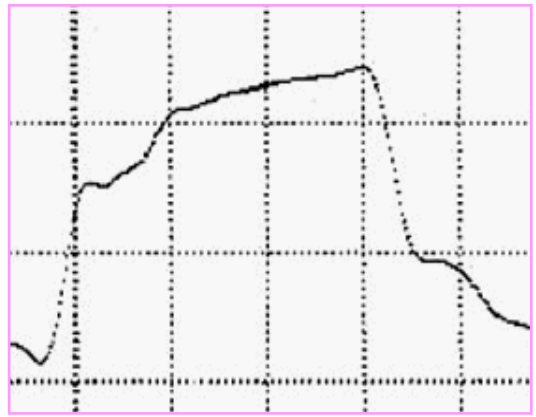
	1	2	3	4	5	6	7	8	9	10	11	12
A	1	44	43	42	41	40	39	38	37	36	35	34
B	2	45	80	79	78	77	76	75	74	73	72	33
C	3	46	81	108	107	106	105	104	103	102	71	32
D	4	47	82	109	128	127	126	125	124	101	70	31
E	5	48	83	110	129	140	139	138	123	100	69	30
F	6	49	84	111	130	141	144	137	122	99	68	29
G	7	50	85	112	131	142	143	136	121	98	67	28
H	8	51	86	113	132	133	134	135	120	97	66	27
J	9	52	87	114	115	116	117	118	119	96	65	26
K	10	53	88	89	90	91	92	93	94	95	64	25
L	11	54	55	56	57	58	59	60	61	62	63	24
M	12	13	14	15	16	17	18	19	20	21	22	23

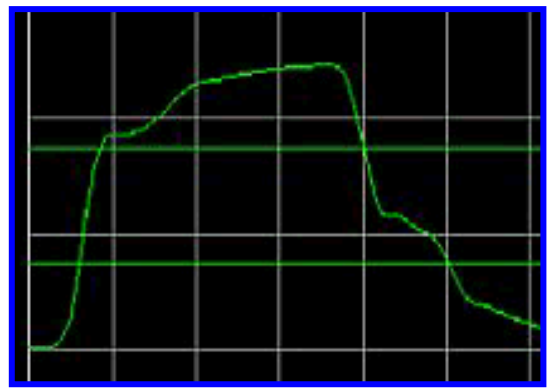
Spiral pin number location

•Tune IBIS Model



Real and Virtual Wave





Comparison-data for the best result

What the SI Electronics whiz does for IBIS?

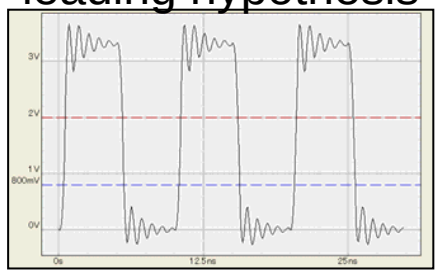
Schematic

IBIS Model

SI view

IBIS model looks good.
Need series termination
Topology should be Daisy

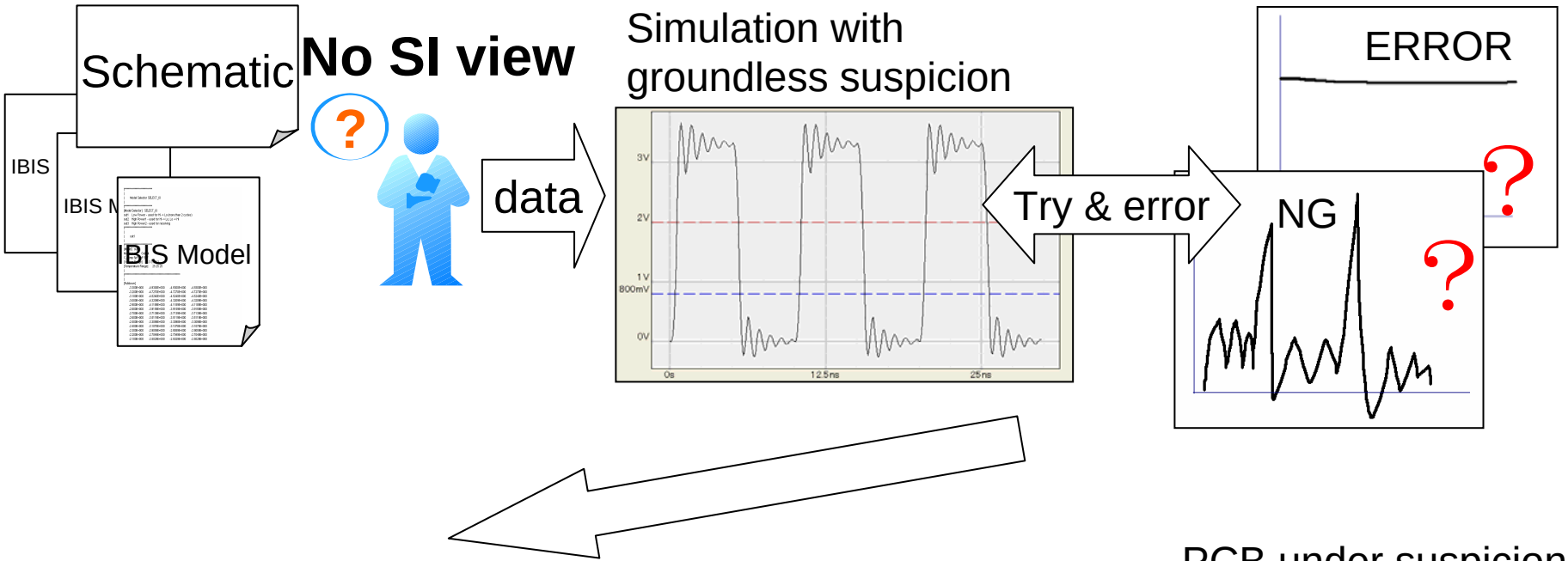
Simulation with leading hypothesis



Engineering instruction to Layout designer

Keep the space of place for series resistor in advance

What the Non SI Electronics whiz may do?

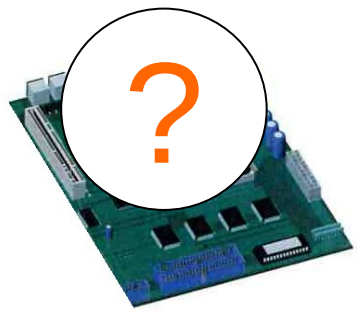


Engineering instruction to Layout designer

Keep the space of place for series resistor <u>if it's possible</u>

Result

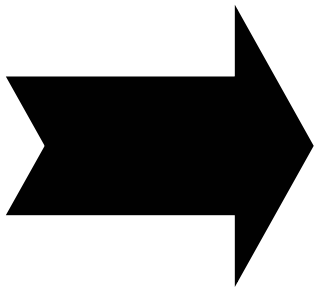
PCB under suspicion

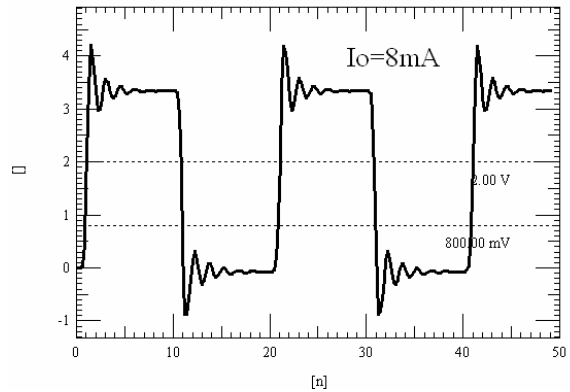


IBIS model Engineering as Front loaded SI Engineering

IBIS Model

```
|*****************************
[Model]   A
Model_type      I/O
Polarity        Non-Inverting
Enable          Active-Low
Vinl = 0.66V
Vinh = 2.00V
C_comp 2.55pF 1.18pF 3.91pF
[Voltage Range] 3.3V 3.0V 3.6V
[Power Clamp Reference] 3.3V 3.0V 3.6V
[GND Clamp Reference] 0.0V 0.0V 0.0V
[Pullup Reference] 3.3V 3.0V 3.6V
[Pulldown Reference] 0.0V 0.0V 0.0V
[Temperature Range] 49.0 125.0 -20.0
|
|*************************************************
|
[Pulldown]
       -3.300E+00       -2.7539E-01       -2.2720E-01       -3.4332E-
       -3.200E+00       -2.6889E-01       -2.2122E-01       -3.3549E-
       -3.100E+00       -2.6192E-01       -2.1499E-01       -3.2720E
```

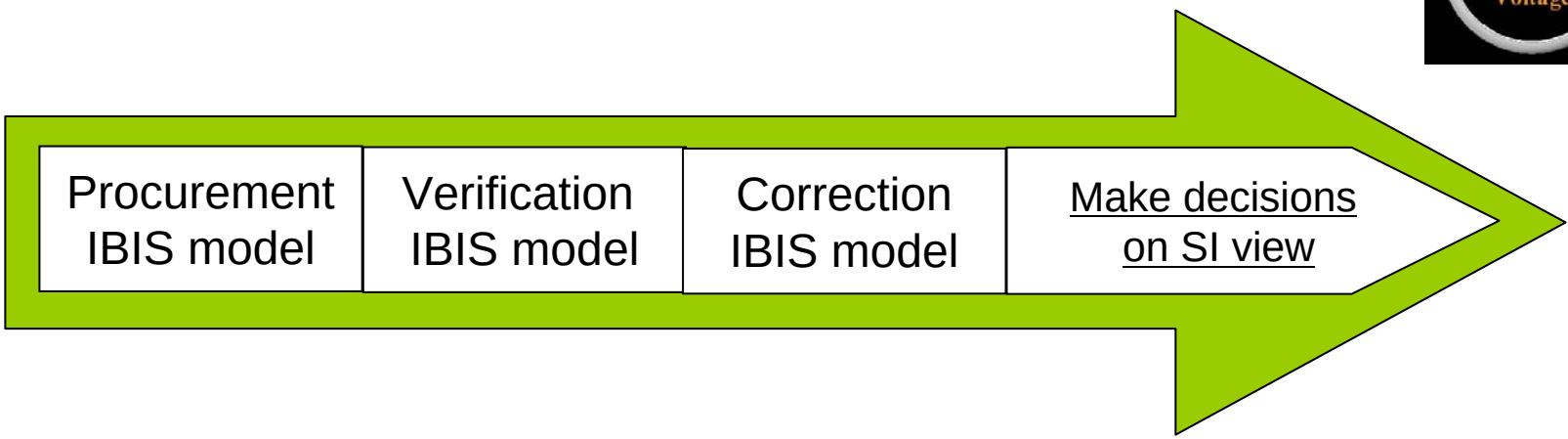




Predict Signal Wave from IBIS Model

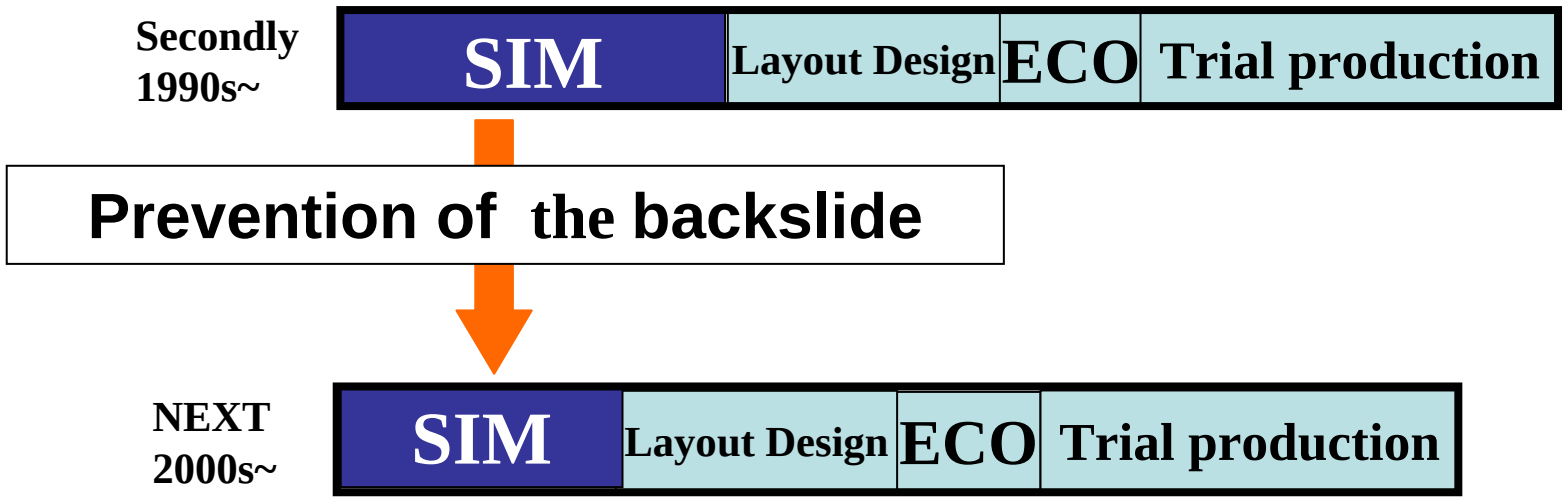
IBIS model Engineering as Front loaded SI Engineering

- Take a look (evaluate a symptom） of Output Current
- Take a look (evaluate a symptom） of Rise/Fall Speed
- Take a look (evaluate a symptom） of Signal amplitude
  - Trend prediction for Routing Topology, Cross Talk ,etc



To minimized the time of SI simulation

Pre Layout Simulation

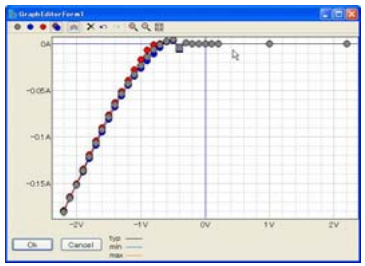


Front loaded SI Engineering

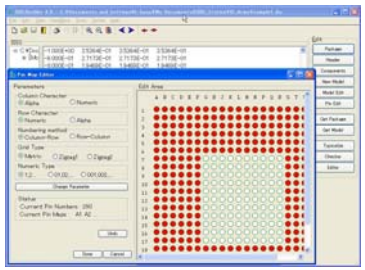
As far in advance as possible

(Reduce the time of SIM)

Usefulness & Comfortable

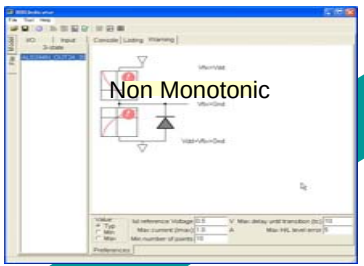


Adjustment

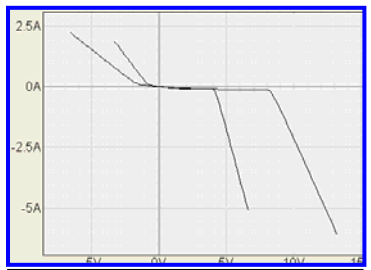


Pin Grid Assign

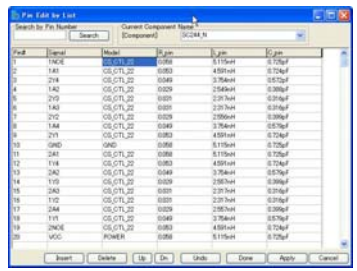
Creative Engineering imagination comes into practical use



Verification



Compare

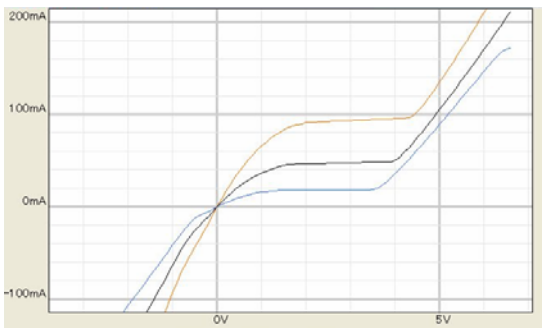


Model/Pin Assign

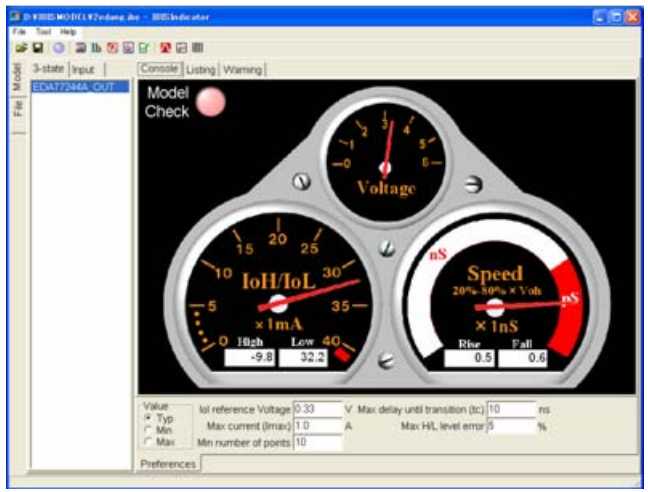
IBIS model goes mainstream

Make IBIS more comfortable

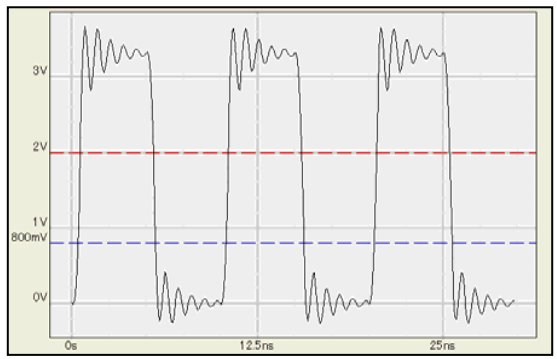
使IBIS使用更方便



Tune



Indicate



Verify