IBIS Model Engineering for SI Simulation
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As time goes by

Number of IBIS Model User

Usefulness

Increase
IBIS model goes mainstream

Time/Cost → all-at-once-ness

- Preparation
- Inspection
- Verification
- Education
Challenge to the SI simulation Engineering of PCB Design

Post Layout Simulation

Primary 1980s~

- Layout Design
- SIM
- ECO
- Trial production

(Reduce the repeat count of trial production)

Sift then Reduce

Secondly 1990s~

Pre Layout Simulation

- SIM
- Layout Design
- ECO
- Trial production

(Reduce the time of ECO)

Next 2000s~

Front loaded SI Engineering
SI Simulation

1. Modeling → Simulation
2. Simulation → Correction
3. Correction → SI Management
4. SI Management → Sim Result
5. Sim Result → Error has occurred
6. Error has occurred → Correction
7. Correction → SI Management

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SI Simulation

**Front loaded IBIS Engineering**

- Modeling
- Simulation
- Find Error
- Correction

- Sim Result
- SI Management

No backslide
**IBIS model Engineering as Front loaded SI Engineering**

To minimized the time of SI simulation

- **Modeling**
  - Incoming inspection for IBIS Model
    - Check IBIS Model
    - Verification IBIS Model
    - Correction IBIS Model
  - Prepare IBIS Model
  - Tune IBIS Model
  
  Make decisions on SI view
Incoming inspection for IBIS Model

• Syntax Check
• I/O Cell Verification

Example:

- Convergence analysis
- Clamp double-counting
- Finding Irregular point
• Verification IBIS Model

Test circuit for IBIS Verification

Example:
• Correction IBIS Model

Example:

Erase and data interpolation

Shift
• Prepare IBIS Model

Pin/Signal/Model Assign

<table>
<thead>
<tr>
<th>Pin#</th>
<th>Signal</th>
<th>Model</th>
<th>R_pin</th>
<th>L_pin</th>
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<tr>
<td>B003</td>
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</table>

BGA

Spiral pin number location
• Tune IBIS Model

More I-O H/L

Less I-O H/L

Detail Edit

Real and Virtual Wave

Comparison-data for the best result
What the SI Electronics whiz does for IBIS?

- IBIS model looks good. Need series termination. Topology should be Daisy.
- Simulation with leading hypothesis.
- Engineering instruction to Layout designer.
- Keep the space of place for series resistor in advance.
What the Non SI Electronics whiz may do?

Schematic

No SI view

IBIS Model

Simulation with groundless suspicion

Try & error

Error

NG

Result

PCB under suspicion

Engineering instruction to Layout designer

Keep the space of place for series resistor if it’s possible
**IBIS Model Engineering as Front loaded SI Engineering**

### IBIS Model

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tbody>
<tr>
<td>Model Type</td>
<td>I/O</td>
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<td>Polarity</td>
<td>Non-Inverting</td>
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<td>Enable</td>
<td>Active-Low</td>
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<tr>
<td>Vinl</td>
<td>0.66 V</td>
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<tr>
<td>Vinh</td>
<td>2.00 V</td>
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<tr>
<td>CComp 2.55pF</td>
<td>1.18pF 3.91pF</td>
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<tr>
<td>Voltage Range</td>
<td>3.3V 3.0V 3.6V</td>
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<tr>
<td>Power Clamp Reference</td>
<td>3.3V 3.0V 3.6V</td>
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<tr>
<td>GND Clamp Reference</td>
<td>0.0V 0.0V 0.0V</td>
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<tr>
<td>Pullup Reference</td>
<td>3.3V 3.0V 3.6V</td>
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<tr>
<td>Pulldown Reference</td>
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</table>

**Predict Signal Wave from IBIS Model**
IBIS model Engineering as Front loaded SI Engineering

- Take a look (evaluate a symptom) of Output Current
- Take a look (evaluate a symptom) of Rise/Fall Speed
- Take a look (evaluate a symptom) of Signal amplitude

- Trend prediction for Routing Topology, Cross Talk, etc.
To minimized the time of SI simulation

Pre Layout Simulation

Secondly 1990s~

Prevention of the backslide

NEXT 2000s~

Front loaded SI Engineering
As far in advance as possible

(Reduce the time of SIM)
IBIS model goes mainstream

Creative Engineering imagination comes into practical use

Usefulness & Comfortable

Adjustment

Pin Grid Assign

Verification

Compare

Model/Pin Assign

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Make IBIS more comfortable

使IBIS使用更方便

Tune

Indicate

Verify