ODT, Pre-Emphasis, and Speed

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On-Die Terminations (ODT)

- Model the device structure
- More details on “DEC” (Deviate, Extrapolate, Calculate) process:
  - http://www.eda.org/pub/ibis/summits/sep05/ross2.pdf
Four ODTs With Same Total I-V

1. [Gnd Clamp] (1.2 V, 50 Ω)
2. [Power Clamp] (0.6 V, 50 Ω)
3. “Clip and Extend” (both clamps clipped)
4. “DEC” (75 Ω, 150 Ω)
Real “50 Ω” ODT Choices

1. I-V in [Gnd Clamp]
2. I-V in [Power Clamp]
3. “Clip and Extend” 52.8 Ω
4. “DEC” 94.2 Ω, 120 Ω

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Pre-emphasis

• Add [Driver Schedule] to match the device structure

• Examples:
  – 2-tap current mode logic (CML) 1-bit delay (de-emphasis) structure
  – Kickers for internal logic controlled boosts (and adjusted waveform delays)
CML Structure using IBIS Open_drain Models and Connected by [Diff Pin]

- **Top-level**
  - ODT [Power Clamp]
  - MAIN [Pulldown]
    - Extracted waveforms with ODT & 50 Ω
    - Pre-emphasis = 0
  - [Driver Schedule]
- **MAIN [Pulldown]**
  - Scaled waveforms
- **BOOST [Pulldown]**
  - Scaled waveforms
Actual SPICE Configuration with Differential Control

IN+  Input bit pattern + TX+

IN-  + MAIN + TX-

Inverse 1-bit delays

[Driver Schedule]

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<tr>
<th>Model_name</th>
<th>Rise_on_dly</th>
<th>Rise_off_dly</th>
<th>Fall_on_dly</th>
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<td>NA</td>
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<tr>
<td>BOOST</td>
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<td>0.47059ns</td>
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### Different Typ-Min-Max Kicker Times (Internal Logic Control Kickers)

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<th>Model_name</th>
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![Diagrams of PMOS_OS, MAIN_TOTEM, and NMOS_OD]

![Graph of time vs. voltage for PMOS_OS, MAIN_TOTEM, and NMOS_OD]
# Speed – How Fast Is IBIS?

- World’s fastest published IBIS model:

```
[IBIS Ver] 1.1
[File Name] fastest.ibs
[File Rev] 0
[Date] October 27, 2006
[Component] Worlds_Fastest_Model
[Manufacturer] Teraspeed Consulting Group

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1.0E-100 V, 50 Ω driver

1.0E-109 s ramps
Conclusion

• How fast is IBIS?
  – “As fast as you are smart”

• How accurate is IBIS?
  – Configure IBIS to match device structure for best accuracy
  – IBIS is as accurate as you are smart