

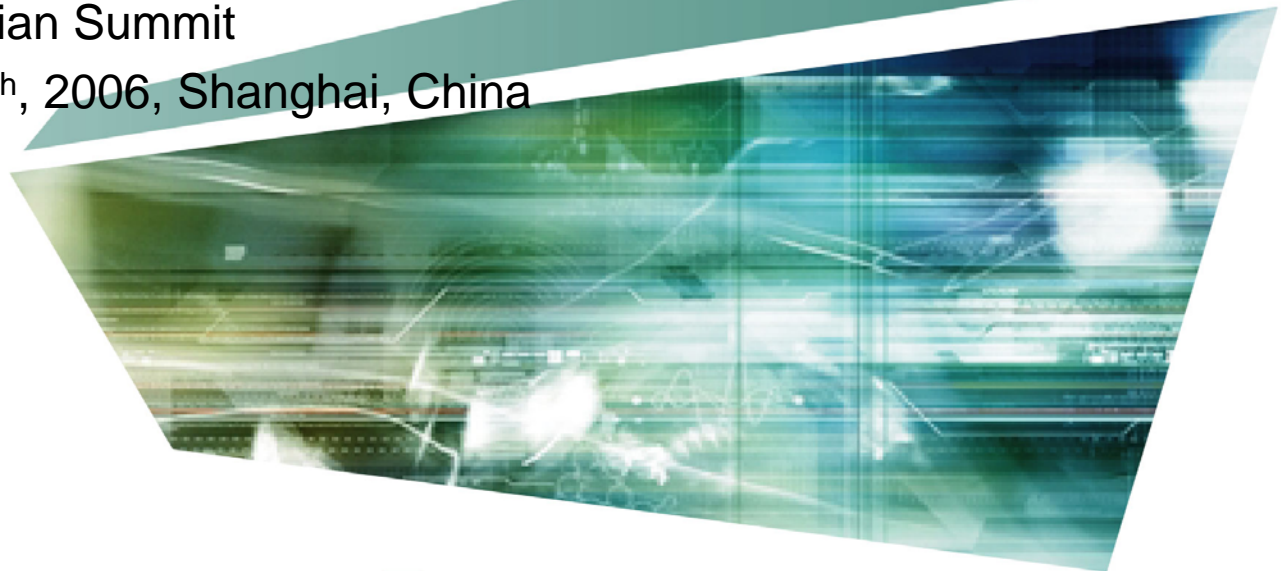
Case Study: Spice Macromodeling for PCI Express using IBIS 4.2

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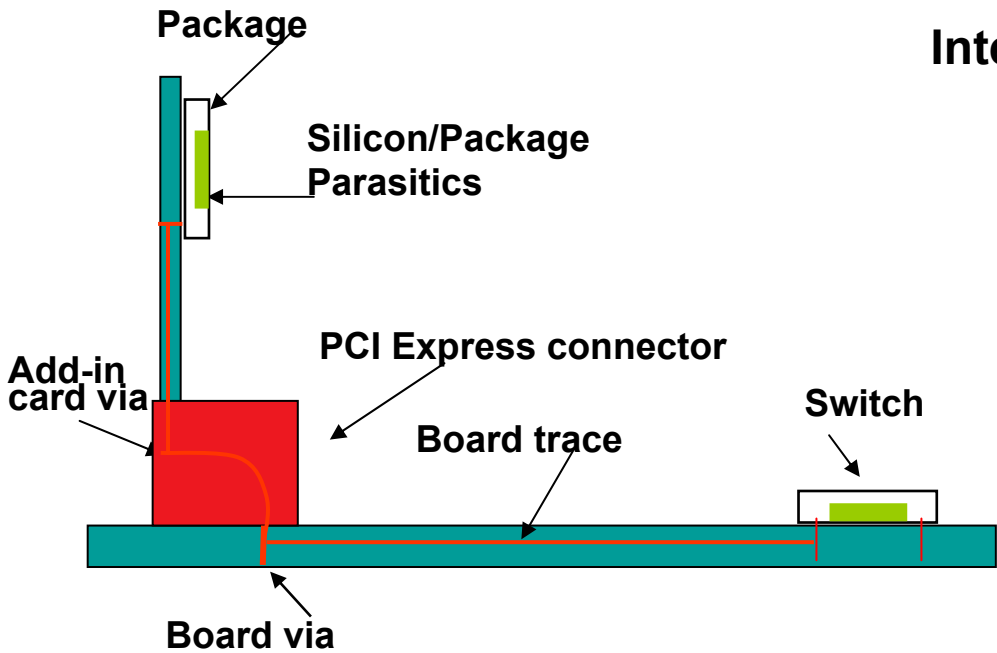
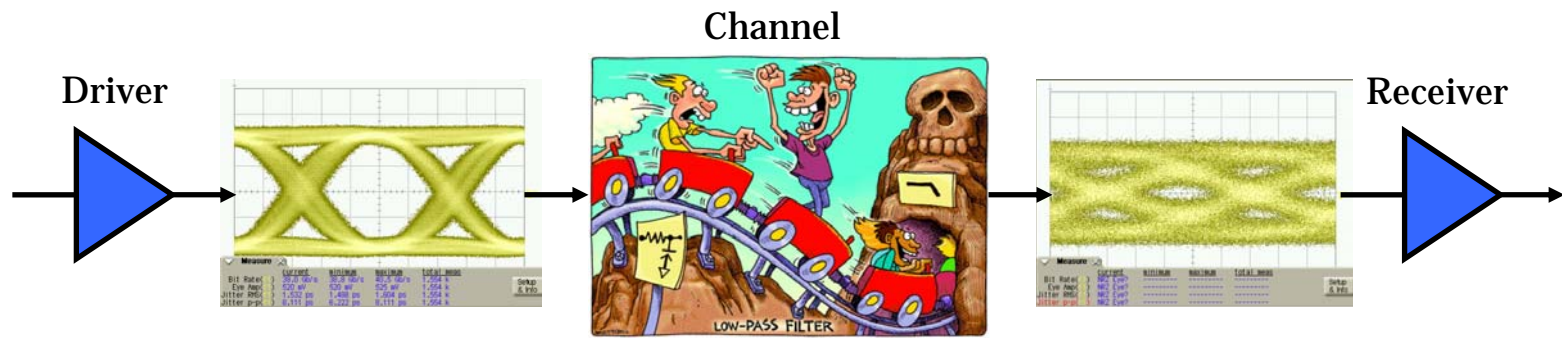
Outline



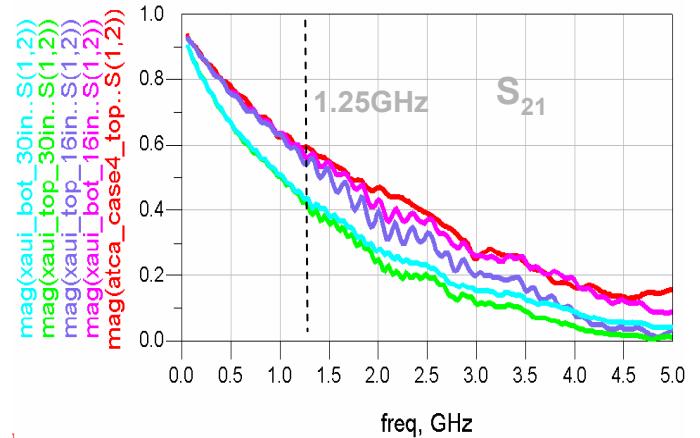
PCI Express Serial Link

- Macromodeling Steps
- IBIS 4.2 Spice Macromodeling
- Validations and Optimizations
- Conclusions

The PCI Express Environment



Inter Symbol Interference/Attenuation

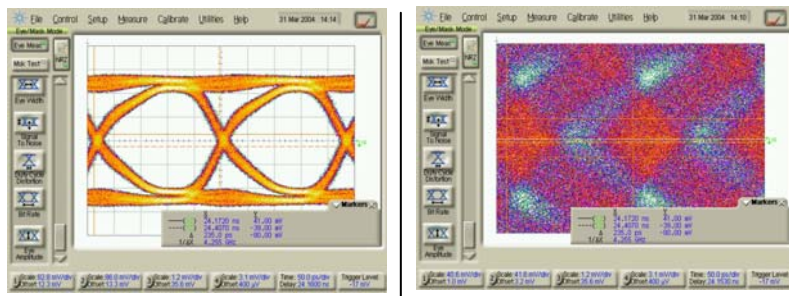


Low Pass Filter

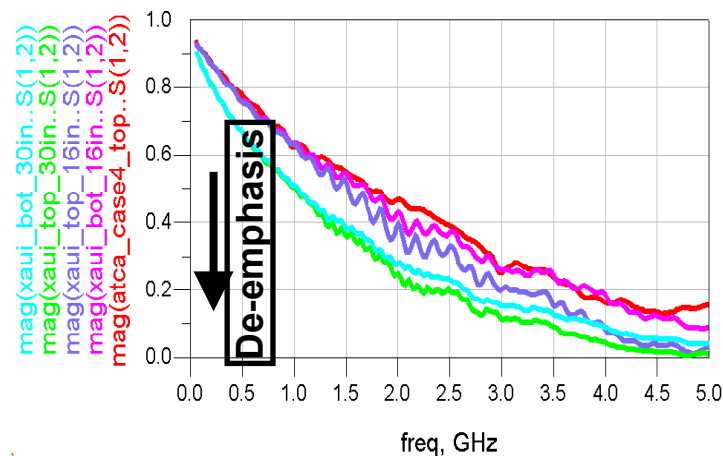
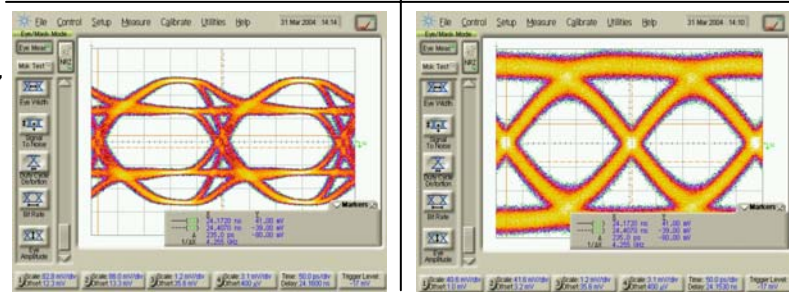
Overcoming ISI using Transmit Equalization (De-Emphasis)

Transmitter > 40" FR4 < At Receiver

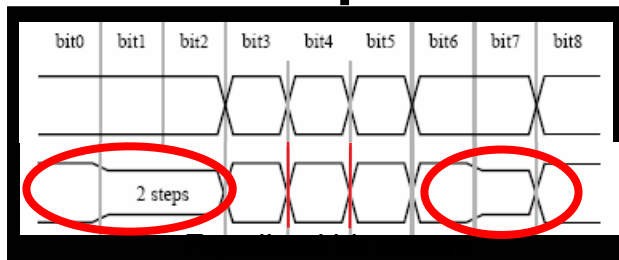
2.5Gbps, PRBS⁷
No Eq.



2.5 Gbps PRBS⁷
-3.5 dB Eq.



Transmit Equalization




PCI-Exp Features (Example)

EQ Control = 4 bit wide DEq bits
Swing Control = 4 bit wide DTx, & HI/LO DRV bits

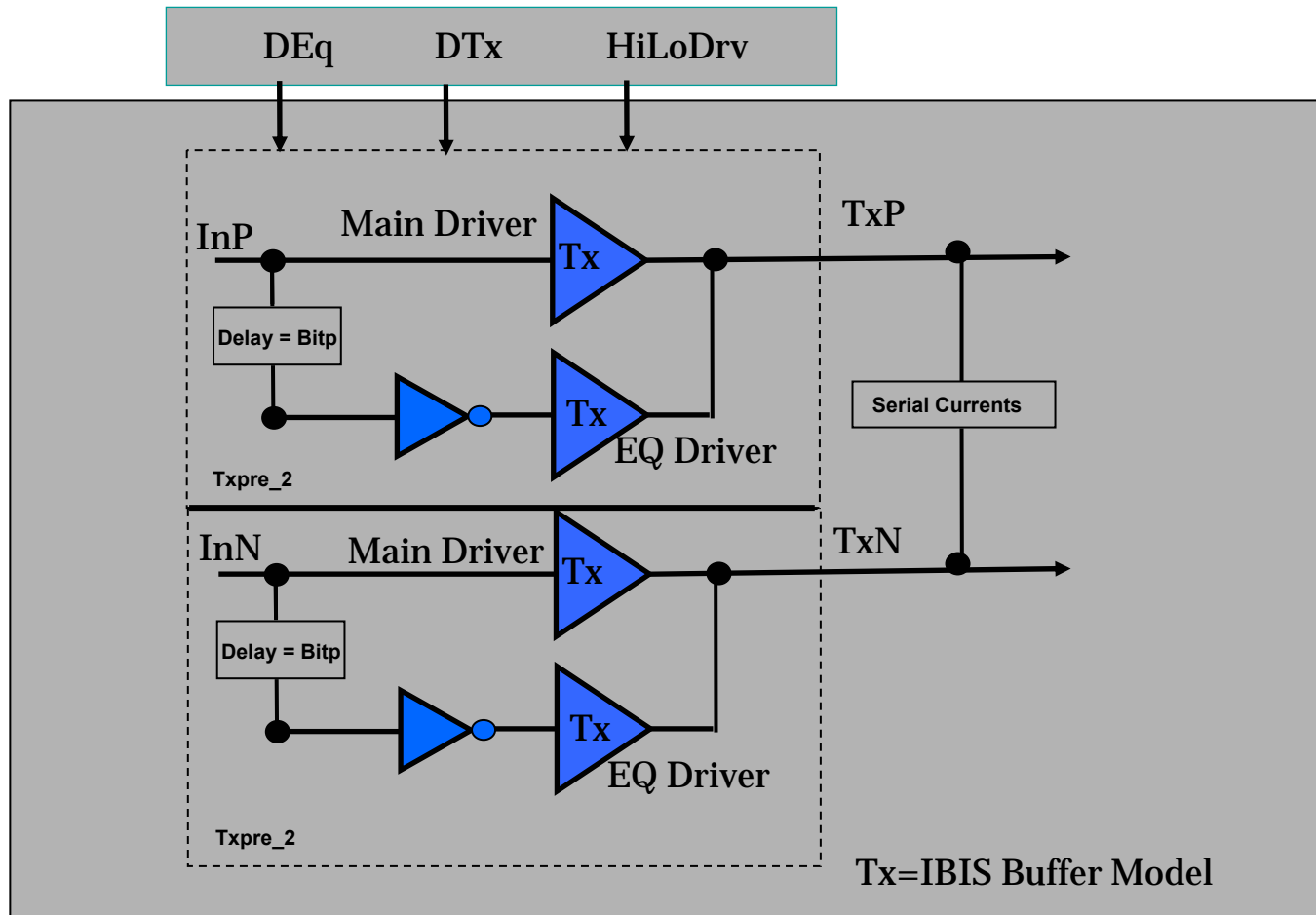


Outline

- PCI Express Serial Link
-  Macromodeling Steps
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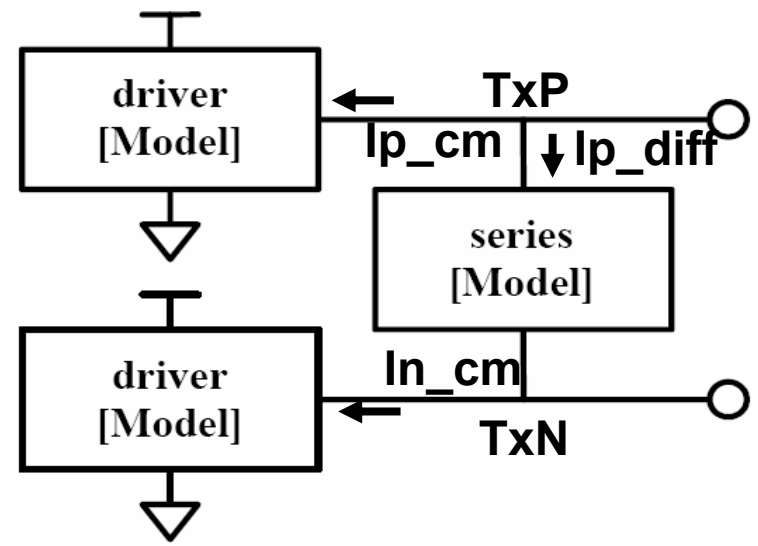
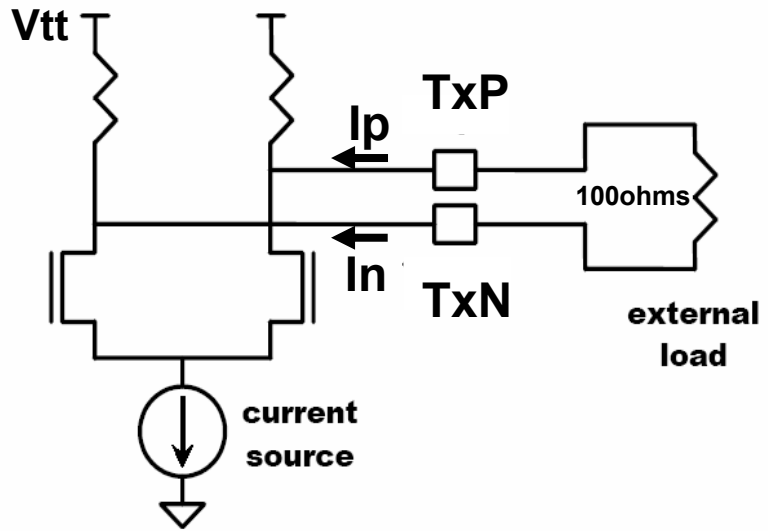
Macromodeling Steps

- Understanding Structures



Macromodeling Steps

- True Differential Pair IBIS Models Extraction

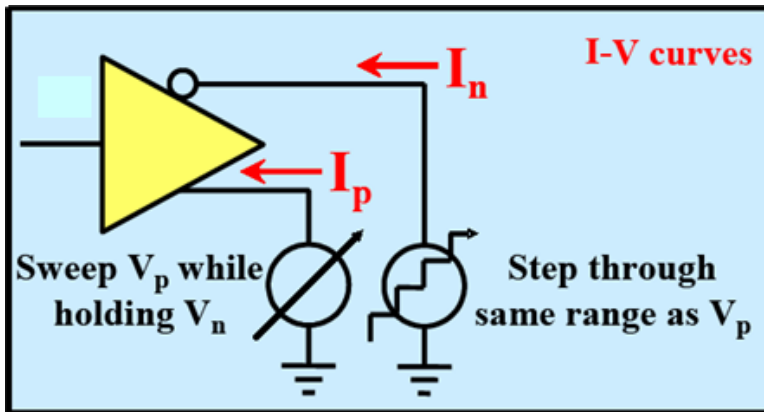


- Common Mode I-V Tables
 - Pull-up
 - Pull-Down
 - Clamp to represent R_{term}
- Differential Model
 - Non linear Series Mosfet Representation
 - Linear Resistor Representation

- V-t Table
 - Recommended to have 2 sets of curve for each TxP and TxN
 - 1)Low -High 2)High-Low
- C_{Comp}/C_{diff}
 - Represents C of transistors, die pads and on-chip interconnects. It does not include pkg C

Macromodeling Steps

- Extracting Common and differential Mode Currents

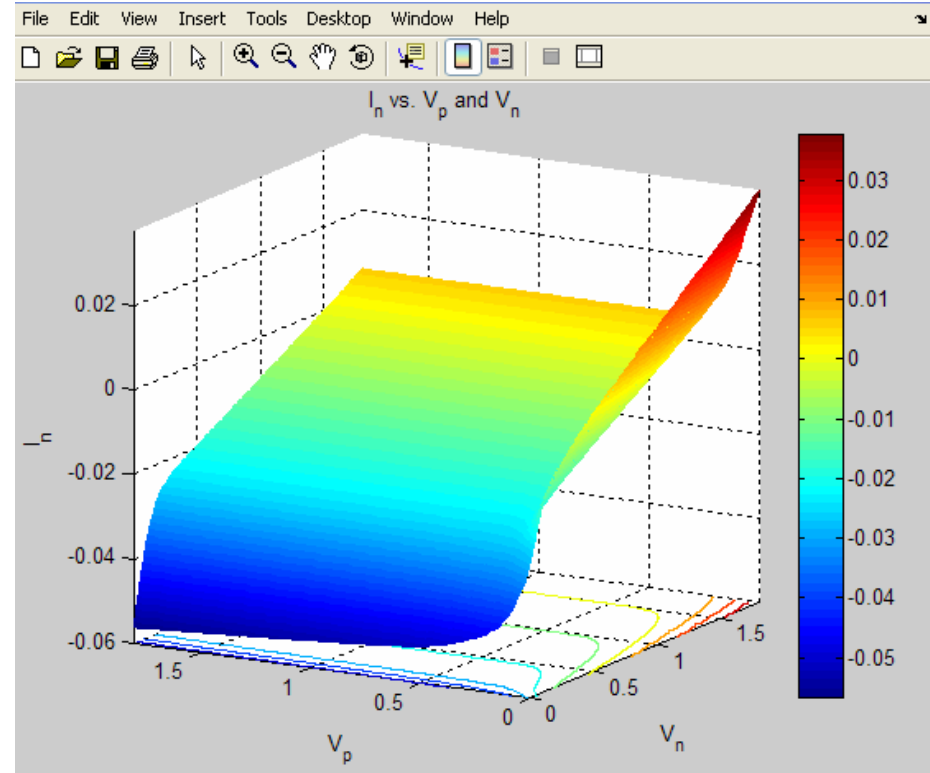
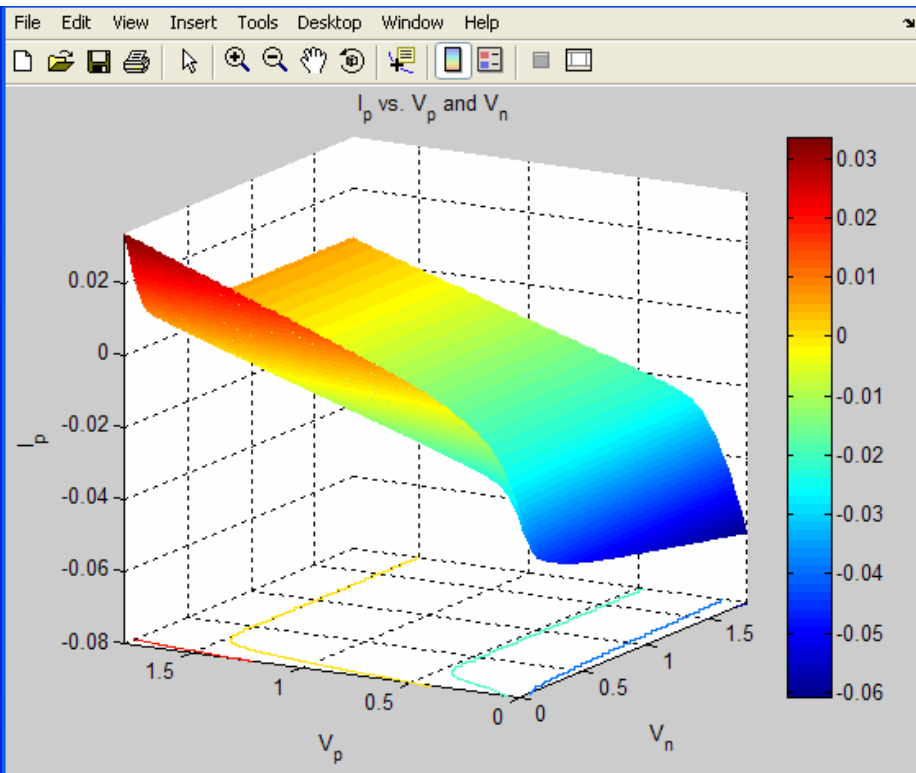


- Pull up and Pull Down Common Mode and differential Mode Current
 - $V_p = V_n$ we are measuring common mode current
 - When $V_p \neq V_n$, we are measuring common + differential currents
 - To get the differential current, we need to subtract the common mode current

- I-V Table Extraction for Clamp Data & On-Die Termination
 - One way to include on-die termination is to use superposition and add the termination currents to the diode currents in the clamp sections
 - Clamps are always active in an IBIS model, regardless of whether the buffer is driving or receiving.

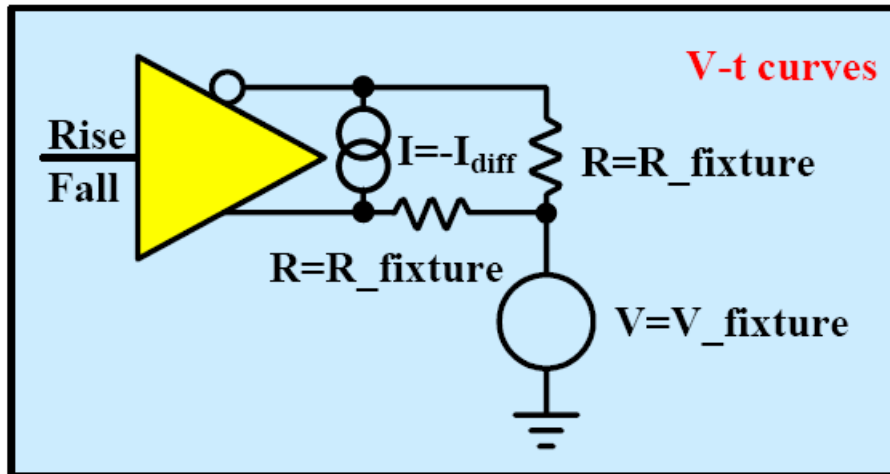
Macromodeling Steps

- In & Ip Surface Plots of Total Current



Macromodeling Steps

- V-t Data Extraction



V-t Table

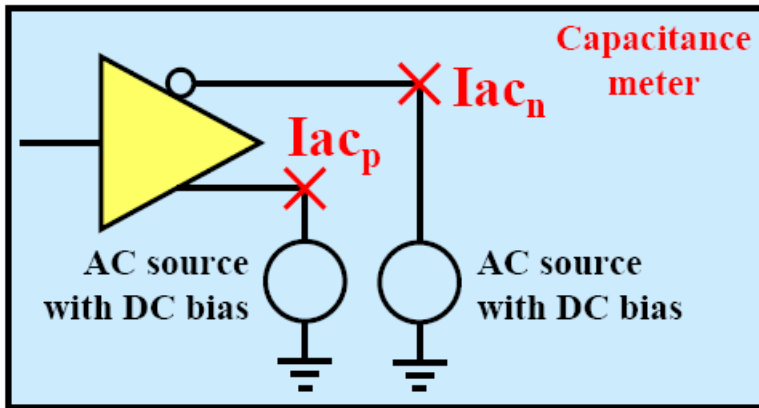
$V_{\text{fixture}} = 0V$

$V_{\text{fixture}} = 1.8V$

$R_{\text{fixture}} =$

Typical load of 50 ohms

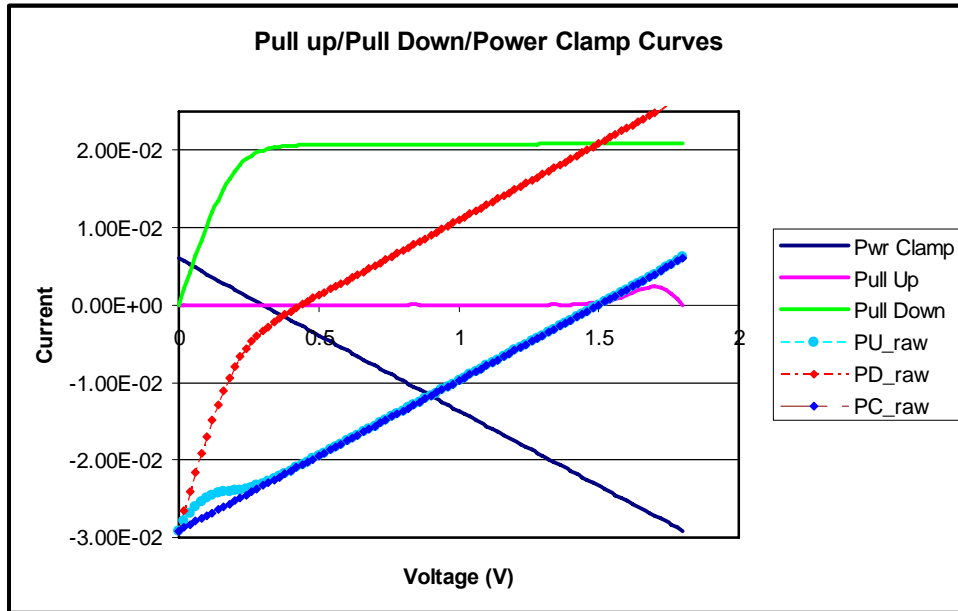
Pad Capacitance: Common and differential Ccomp



- Run frequency domain simulations (.AC) with the above circuit
 - Give one of the AC sources 0 V AC amplitude (makes it a DC source)
 - Give the other AC source a small AC amplitude (1 mV)
 - Give both of the sources an appropriate DC bias
- Calculate capacitance using:
$$C = \text{Im}(I) / (2\pi f * \text{Amplitude})$$
 - For Ccommon use the current of the “DC” source
 - For Cdiff use the current of “AC” source minus “DC” source
- Repeat everything at different DC bias voltages

Macromodeling Steps

- Pull Up, Pull Down and Clamp Curves



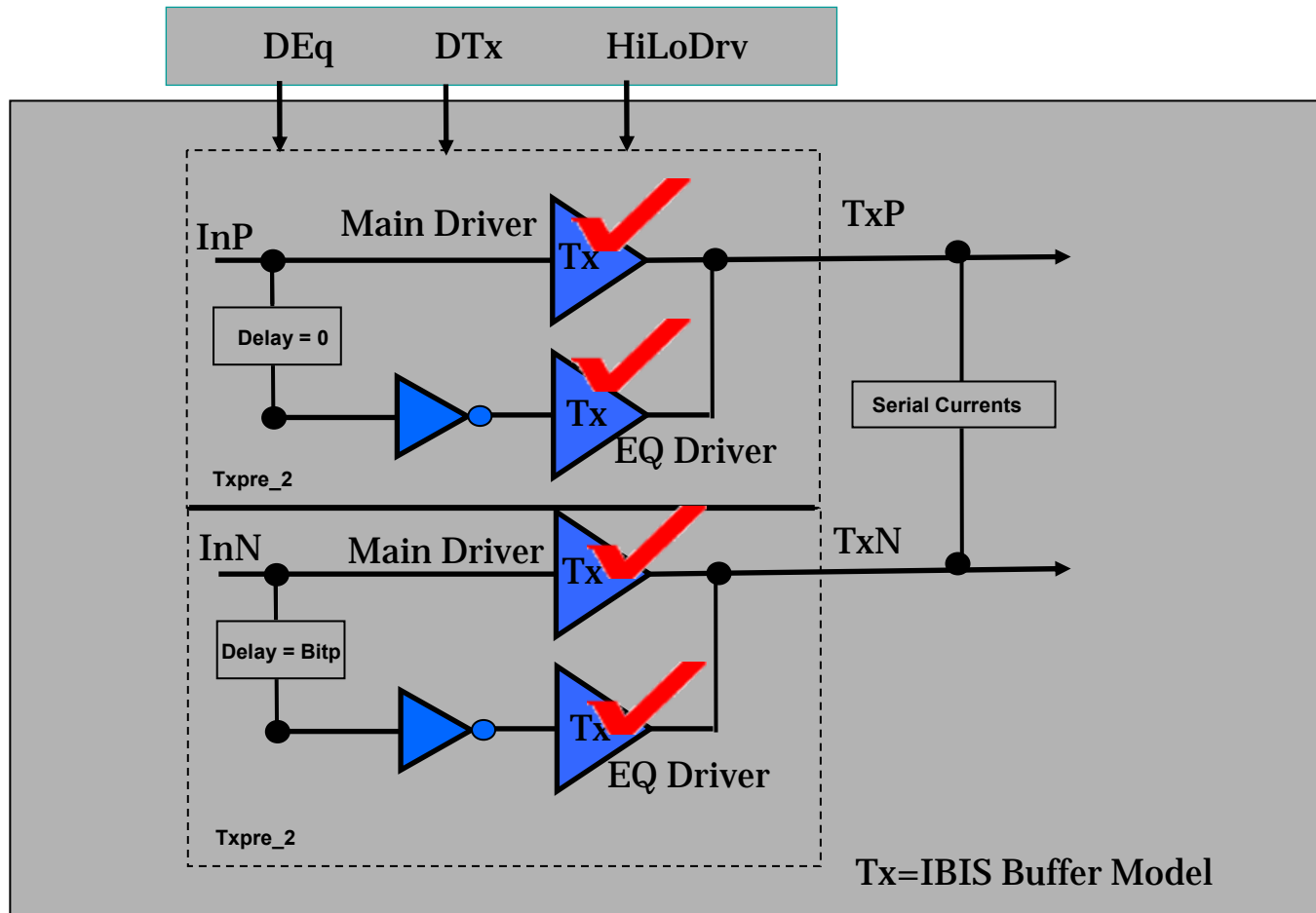
```

*****
|          PULL UP Data          |
|*****|
|[Pullup]                       |
|Voltage      I(typ)           I(min)      I(max)      |
|1.8          -2.34E-05        NA           NA           |
|1.78         8.32E-04         NA           NA           |
|1.76         1.47E-03         NA           NA           |
|...          |
|...          |
|0.04         3.47E-06         NA           NA           |
|0.02         8.07E-06         NA           NA           |
|0            7.00E-06         NA           NA           |
|*****|
|          PULL DOWN Data        |
|*****|
|[Pulldown]                      |
|Voltage      I(typ)           I(min)      I(max)      |
|1.8          2.09E-02         NA           NA           |
|1.78         2.09E-02         NA           NA           |
|1.76         2.09E-02         NA           NA           |
|...          |
|...          |
|0.04         4.31E-03         NA           NA           |
|0.02         2.19E-03         NA           NA           |
|0            0.00E+00         NA           NA           |
|[GND Clamp]                      |
| Voltage      I(typ)           I(min)      I(max)      |
|0.0000       0.00000000e+000   NA           NA           |
|1.8000       0.00000000e+000   NA           NA           |
|[POWER Clamp]                      |
| Voltage      I(typ)           I(min)      I(max)      |
|1.8          -2.91E-02         NA           NA           |
|1.78         -2.87E-02         NA           NA           |
|...          |
|...          |
|0.04         5.27E-03         NA           NA           |
|0.02         5.70E-03         NA           NA           |
|0            6.14E-03         NA           NA           |

```

Macromodeling Steps

- Understanding Structures



Separating the differential mode current

- The off-diagonal current values represent the sum of the common and differential mode currents
- To obtain the differential mode currents alone, “normalize” the surface so that its diagonal values become zero
 - Subtract the common mode component from the surface and use it for the Series [Model]’s [R Series], [Series Current], [Series MOSFET], etc... keywords
 - If the surface is linear (flat) [R Series] is sufficient
 - Otherwise use the [Series Current] or [Series MOSFET] keywords
 - Slice the surface along the necessary voltage value(s) to satisfy the syntax requirement of the IBIS keyword used



page 11

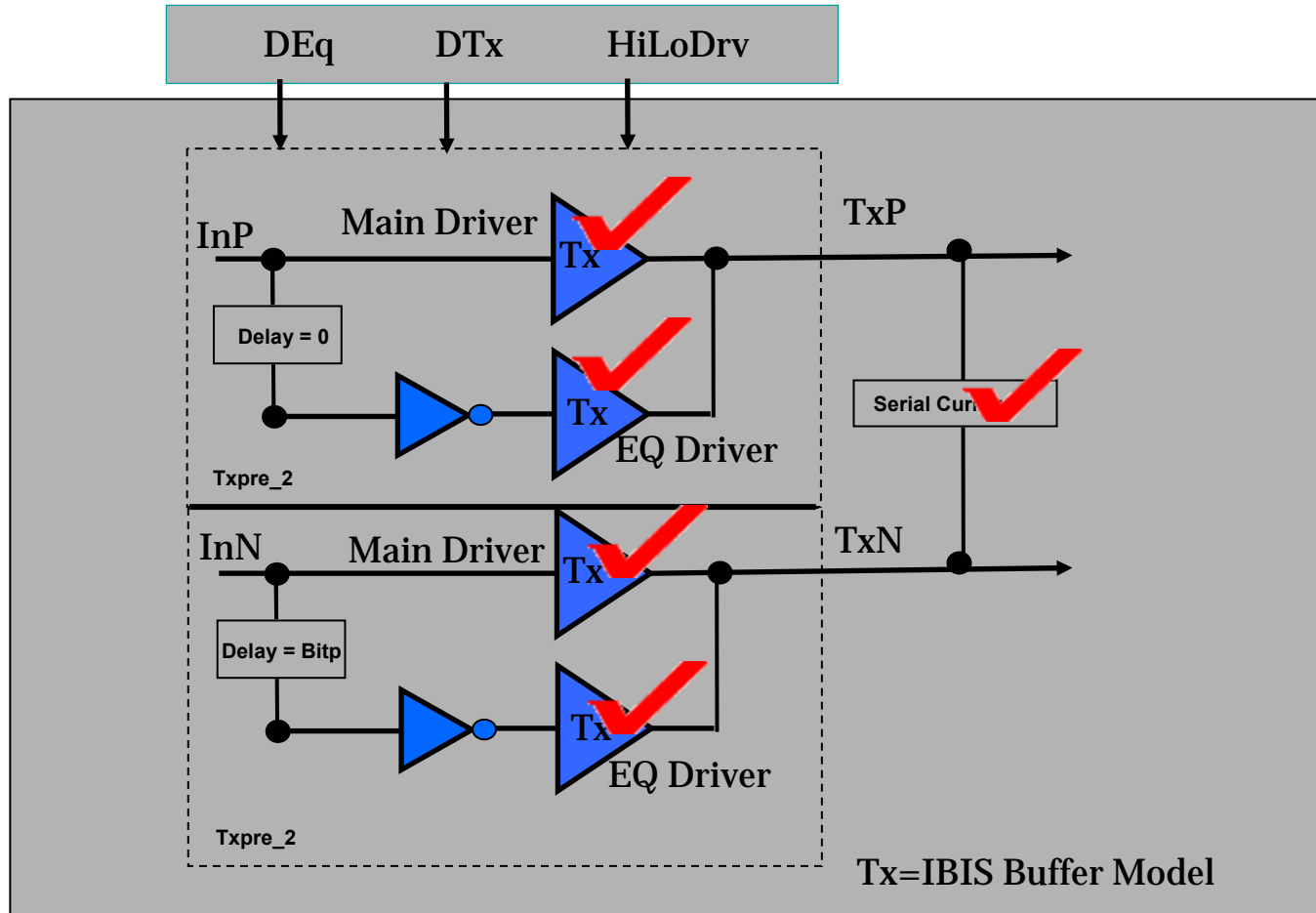


*Slide from Arpad Muranyi's
true diffpair modeling
IBIS Summit 2003*

```
[Series Pin Mapping] pin_2 model_name function_table_group
1                2      s_mosfet      1
|
|
[Series Switch Groups]
On 1 /
|
|
[Model]          s_mosfet
Model_type       Series_switch
Polarity         Non-Inverting
Enable           Active-High
|
|
C_comp           0      0      0
|
|
[Voltage Range] 1.8v  NA      NA
|
|
[On]
|
|
*****
Series MOSFET I-V Table
*****
|
|
Voltage          I (typ)          I (typ)          I (typ)
|
|
[series MOSFET]
Vds=0.1V
0.0000          8.8610e-7A          8.8610e-7A          8.8610e-7A
0.0100          8.9280e-7A          8.9280e-7A          8.9280e-7A
0.0200          8.8890e-7A          8.8890e-7A          8.8890e-7A
0.0300          8.9270e-7A          8.9270e-7A          8.9270e-7A
0.0400          8.8740e-7A          8.8740e-7A          8.8740e-7A
0.0500          8.8930e-7A          8.8930e-7A          8.8930e-7A
0.0600          8.8420e-7A          8.8420e-7A          8.8420e-7A
0.0700          8.8540e-7A          8.8540e-7A          8.8540e-7A
0.0800          8.8180e-7A          8.8180e-7A          8.8180e-7A
0.0900          8.8350e-7A          8.8350e-7A          8.8350e-7A
0.1000          8.8190e-7A          8.8190e-7A          8.8190e-7A
0.1100          8.8440e-7A          8.8440e-7A          8.8440e-7A
0.1200          8.8480e-7A          8.8480e-7A          8.8480e-7A
0.1300          8.8790e-7A          8.8790e-7A          8.8790e-7A
0.1400          8.8950e-7A          8.8950e-7A          8.8950e-7A
0.1500          8.9310e-7A          8.9310e-7A          8.9310e-7A
0.1600          8.9520e-7A          8.9520e-7A          8.9520e-7A
0.1700          8.9890e-7A          8.9890e-7A          8.9890e-7A
0.1800          9.0130e-7A          9.0130e-7A          9.0130e-7A
0.1900          9.0530e-7A          9.0530e-7A          9.0530e-7A
```

Macromodeling Steps

- Understanding Structures



Macromodeling Steps

- Coefficient table for HiLoDrv, DEq and DTx

* coefficient to control the current source

```
.param ctrlcoef='if(hilodrv == 0) (1.00)
+ elseif(hilodrv == 1) (0.50)
+ elseif(hilodrv == 2) (1.4) else(1)‘.....
+.....
```

* coefficient to control dtx bits

```
.param dtxcoef='if(dtx == 0) (1)
+ elseif(dtx == 1) (1.05)
+ elseif(dtx == 2) (1.1)
+ elseif(dtx == 8) (0.6).....
+ .....
```

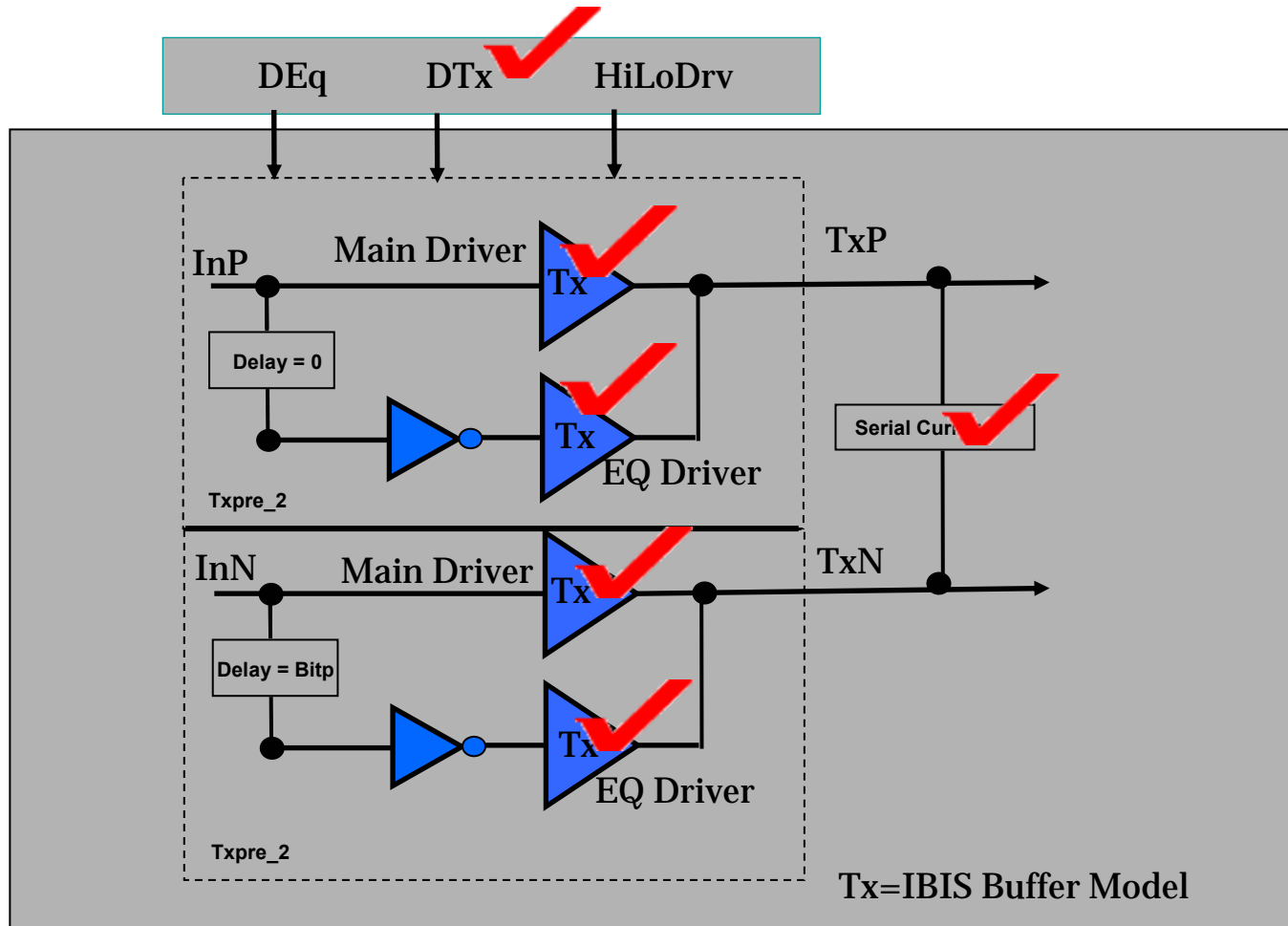
* coefficient to control the eq bits

```
.param deqcoef='if(deq == 0) (1.0)
+ elseif(deq == 1) (0.96)
+ elseif(deq == 2) (0.92)
+ elseif(deq == 3) (0.88)
+ elseif(deq == 4) (0.84).....
+.....
```

HSpice is capable for this circuit.

Macromodeling Steps

- Understanding Structures



Macromodeling Steps

- Output Block Example

```
.subckt txpre_2 nvdd out ngnd in en  
+ bitp=400p inv0=0 inv1=1  
+ cf0=1 cf1=0 scale=1 padcap=1.2p ampctrl=1
```

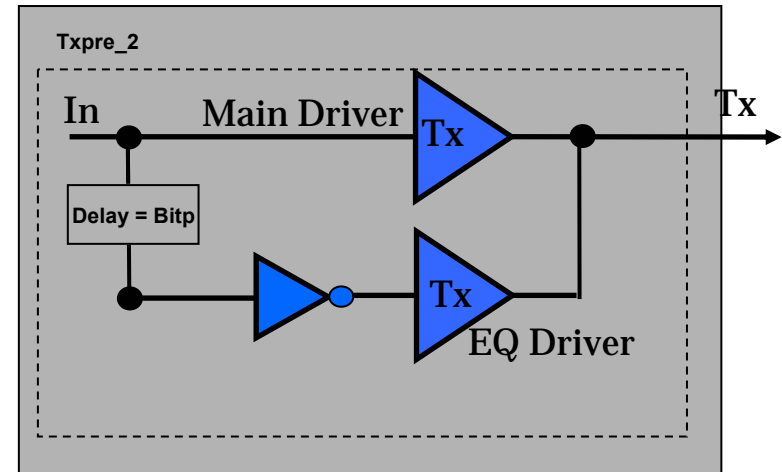
* Here are the subcircuit calls for the tap inputs

```
xin0 in0 in ngnd delayin inv=inv0  
xin1 in1 in ngnd delayin inv='inv1' del='bitp'
```

```
xtx0 nvdd out ngnd in0 en tx sclpux='scale*cf0*ampctrl' sclpdx='scale*cf0*ampctrl'  
xtx1 nvdd out ngnd in1 en tx sclpux='scale*cf1*ampctrl' sclpdx='scale*cf1*ampctrl'
```

* This is the subcircuit definition for tx, used for the taps.

```
.subckt tx nvdd out ngnd in en sclpux=1 sclpdx=1  
bdrvrv nvdd out ngnd in en Model=BUFF File=ibis_file  
+ VIScale_pullup='sclpux'  
+ VIScale_pulldown='sclpdx'  
.ends tx
```



HSpice is capable for this circuit.

Macromodeling Steps

- P & N Pins

* P side driver subcircuit call

```
xp nvdd outp ngnd in en txpre_2 BUFF=BUFF ibis_file=ibis_file  
+ bitp=bitp inv0=inv0 inv1=inv1  
+ scale=scale  
+ cf0=cf0  
+ cf1=cf1  
+ rt=rt  
+ ampctrl=ampctrl
```

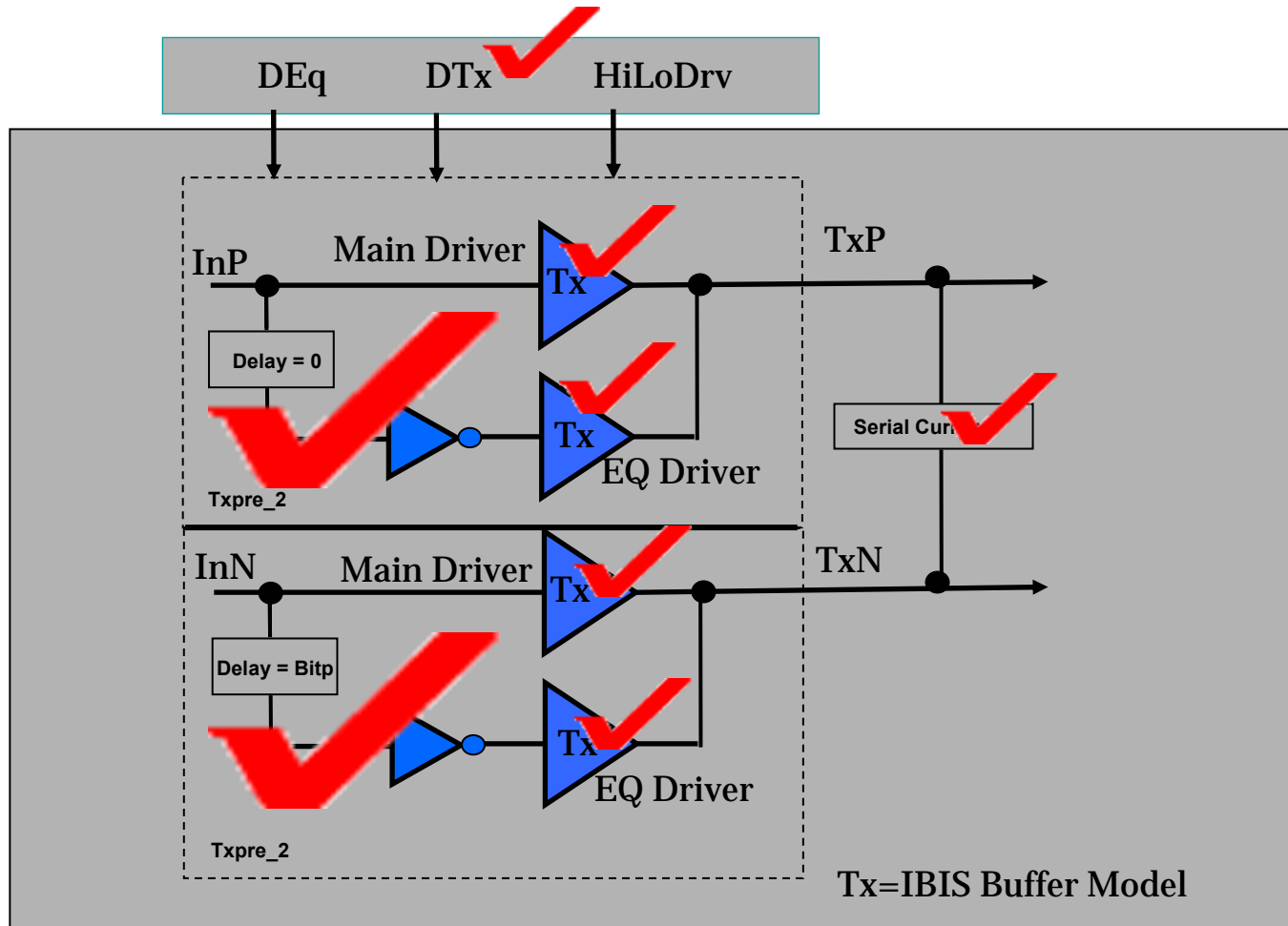
* N side driver subcircuit call

```
xn nvdd outn ngnd inn en txpre_2 BUFF=BUFF ibis_file=ibis_file  
+ bitp=bitp inv0=inv0 inv1=inv1  
+ scale=scale  
+ cf0=cf0  
+ cf1=cf1  
+ rt=rt  
+ ampctrl=ampctrl
```

HS spice is capable for this circuit.


Macromodeling Steps

- Understanding Structures





Outline

- PCI Express Serial Link
- Macromodeling Steps
-  IBIS 4.2 Spice Macromodeling
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Wrap into IBIS 4.2

```
|*****
[IBIS Ver]      4.2
[File Name]    pcie_rs2314.ibs
[File Rev]     1.0
[Date]         4/7/2006
[Source]       Converted from PCIe Macromodel
[Notes]
[Disclaimer]
[Copyright]    Copyright 2006,
|*****
[Component]    rs2314_tx
[Manufacturer] ABC Inc.
[Package]
|
|          typ          min          max
R_pkg      0.001         0.001         0.001
L_pkg      1e-013       1e-013       1e-013
C_pkg      1e-015       1e-015       1e-015
|*****
[PIN]  signal_name  model_name  R_pin  L_pin  C_pin
|
A1     txoutp      pcie_behav  0.086  4.3e-009  0.72e-012
B1     txoutn      pcie_behav  0.086  4.3e-009  0.72e-012
Base   test_single  behav_base
|*****
[Diff Pin]  inv_pin  vdiff  tdelay_typ  tdelay_min  tdelay_max
A1          B1     200mv    0           0           0
|
|*****
[Model] pcie_behav
| need to use *_diff for ture differential pair models
Model_type Output_diff
|
Ref diff = 100
```

Wrap into IBIS 4.2

```

*****
[Model] pcie_behav
| need to use *_diff for ture differential pair models
Model_type Output_diff
|
Rref_diff = 100
|
| Other model subparameters are optional
|
|          typ    min    max
[Voltage Range]  1.5    1.5    1.5
|
[Ramp]
dV/dt_r    300mV/95ps    240mV/80ps    360mV/110ps
dV/dt_f    300mV/95ps    240mV/80ps    360mV/110ps
|
[External Model]
Language SPICE
|
| Corner corner_name file_name      circuit_name (.subckt name)
| specify the corners
Corner    Typ      pcie.spc      pcie_behav
Corner    Min      pcie.spc      pcie_behav
Corner    Max      pcie.spc      pcie_behav
|
| Parameter definitions
| prefix BUFF will be traded as buffer model setting.
Parameters BUFF=behav_base
|
| all regular paramters are here. Change them for different settings
Parameters bitp=400p
Parameters scale=1.60
Parameters rt=50
Parameters dtx=5
Parameters deq=3
Parameters hilodrv=0
|
| Ports List of port names (in same order as in SPICE)
|
Ports    A_puref    A_signal_pos    A_pdref    my_drive
Ports    A_pcref    A_gcref    A_signal_neg
|
| D_to_A d_port    port1      port2      vlow    vhigh    trise    tfall    corner_name
D_to_A    D_drive    my_drive    A_pdref    0.0    1.0    95p    95p    Typ
D_to_A    D_drive    my_drive    A_pdref    0.0    1.0    80p    80p    Min
D_to_A    D_drive    my_drive    A_pdref    0.0    1.0    110p    110p    Max
| D_to_A will be used as escale my_drive 3 v=[vhigh - vlow]*v[D_drive]+vlow
| trise and tfall will be the ramping data
|
| no A_to_D required
|
[End External Model]

```


```

*****
Model behav_base
Your base IBIS model
*****
[Model]          behav_base
Model_type      Output
Polarity        Non-Inverting
Vmeas = 1.5V
Cref = 0pf
Rref = 50
|
C_comp          0.1pF          0.1pF          0.1pF
|
[Temperature Range]  25.00          110.00          0
[Voltage Range]     1.5V          1.5V          1.5V
|
[Pulldown]
| voltage      I (typ)          I (min)          I (max)
-1.50000000    -0.15536276    -1.7720580e-01    -1.5186892e-01
-1.49550000    -0.15460042    -1.7637204e-01    -1.5124756e-01
-1.44600000    -0.14637165    -1.6724147e-01    -1.4492167e-01
-1.39200000    -0.13770218    -1.5736305e-01    -1.3870920e-01
-1.34250000    -0.13024052    -1.4840655e-01    -1.3352144e-01
-1.29300000    -0.12349249    -1.3957303e-01    -1.2863052e-01
-1.24800000    -0.11808127    -1.3167686e-01    -1.2429165e-01
|
-1.19800000    -0.11277202    -1.2377569e-01    -1.1945283e-01
-1.14800000    -0.10746276    -1.1587452e-01    -1.1445396e-01
-1.09800000    -0.10215350    -1.0797335e-01    -1.0945509e-01
-1.04800000    -0.09684424    -0.9997218e-01    -1.0445622e-01
-0.99800000    -0.09153498    -0.9197101e-01    -0.9945735e-01
-0.94800000    -0.08622572    -0.8396984e-01    -0.9445848e-01
-0.89800000    -0.08091646    -0.7596867e-01    -0.8945961e-01
-0.84800000    -0.07560720    -0.6796750e-01    -0.8446074e-01
-0.79800000    -0.07029794    -0.5996633e-01    -0.7946187e-01
-0.74800000    -0.06498868    -0.5196516e-01    -0.7446300e-01
-0.69800000    -0.05967942    -0.4396400e-01    -0.6946413e-01
-0.64800000    -0.05437016    -0.3596283e-01    -0.6446526e-01
-0.59800000    -0.04906090    -0.2796166e-01    -0.5946639e-01
-0.54800000    -0.04375164    -0.1996050e-01    -0.5446752e-01
-0.49800000    -0.03844238    -0.1195933e-01    -0.4946865e-01
-0.44800000    -0.03313312    -0.0395816e-01    -0.4446978e-01
-0.39800000    -0.02782386    -0.0595700e-01    -0.3947091e-01
-0.34800000    -0.02251460    -0.0795583e-01    -0.3447204e-01
-0.29800000    -0.01720534    -0.0995466e-01    -0.2947317e-01
-0.24800000    -0.01189608    -0.1195350e-01    -0.2447430e-01
-0.19800000    -0.00658682    -0.1395233e-01    -0.1947543e-01
-0.14800000    -0.00127756    -0.1595116e-01    -0.1447656e-01
-0.09800000    -0.00394368    -0.1795000e-01    -0.0947769e-01
-0.04800000    -0.00760980    -0.1994883e-01    -0.0447882e-01
-0.00000000    -0.01127592    -0.2194766e-01    -0.0047995e-01
|
[Ramp]
| variable      typ          min          max
dV/dt_r        300mV/95ps    240mV/80ps    360mV/110ps
dV/dt_f        300mV/95ps    240mV/80ps    360mV/110ps
R_load = 50.00
|
| End [Model] pcie_behav_base
*****

```

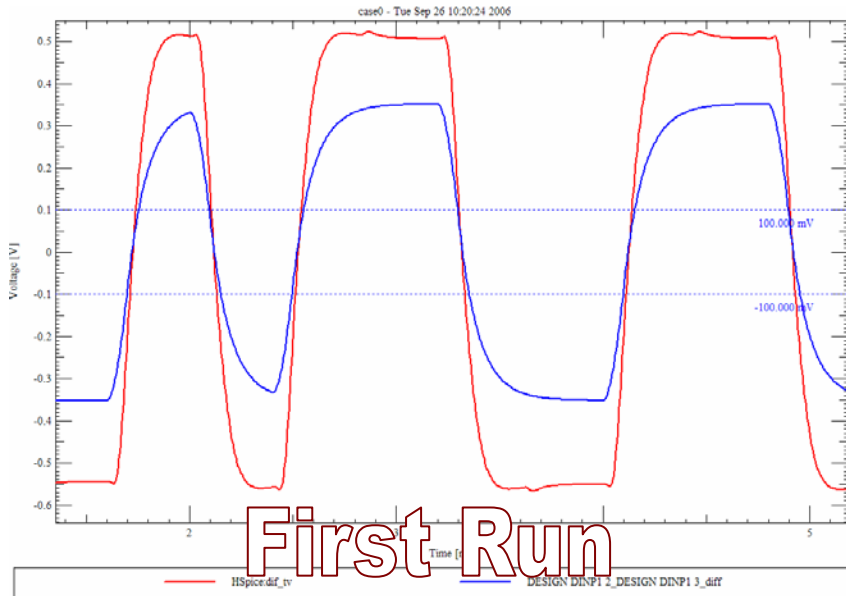


Outline

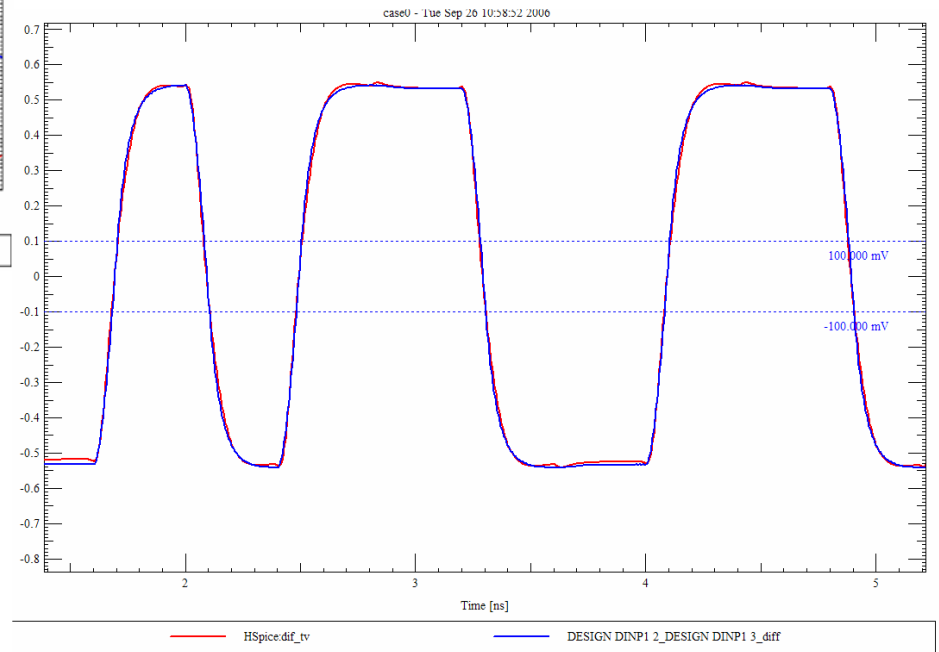
- PCI Express Serial Link
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Validations and Optimizations

- $DEq = 0$, $DTx = 0$, $HiLoDrv = 0$

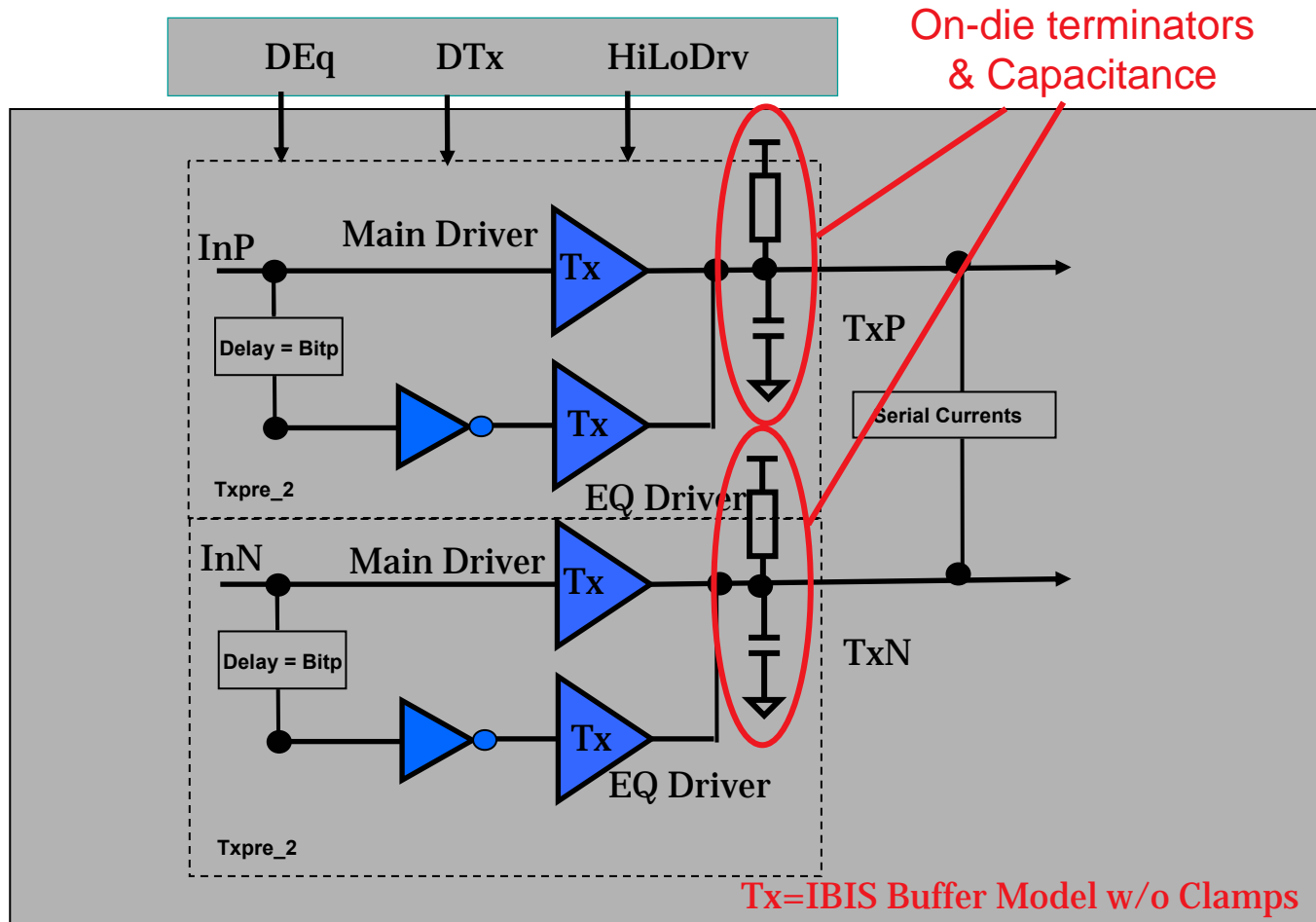


- Use combined die capacitor instead of C_{comp} in IBIS model
- Use combined on-die terminator instead of clamps
- Adjust DEq and DTx initial levels



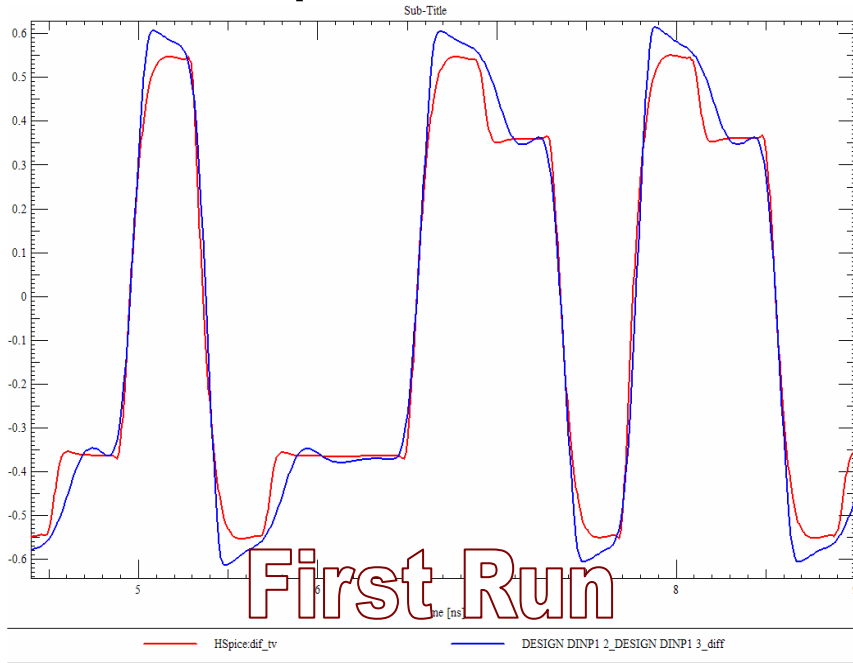
Macromodeling Steps

- Understanding Structures

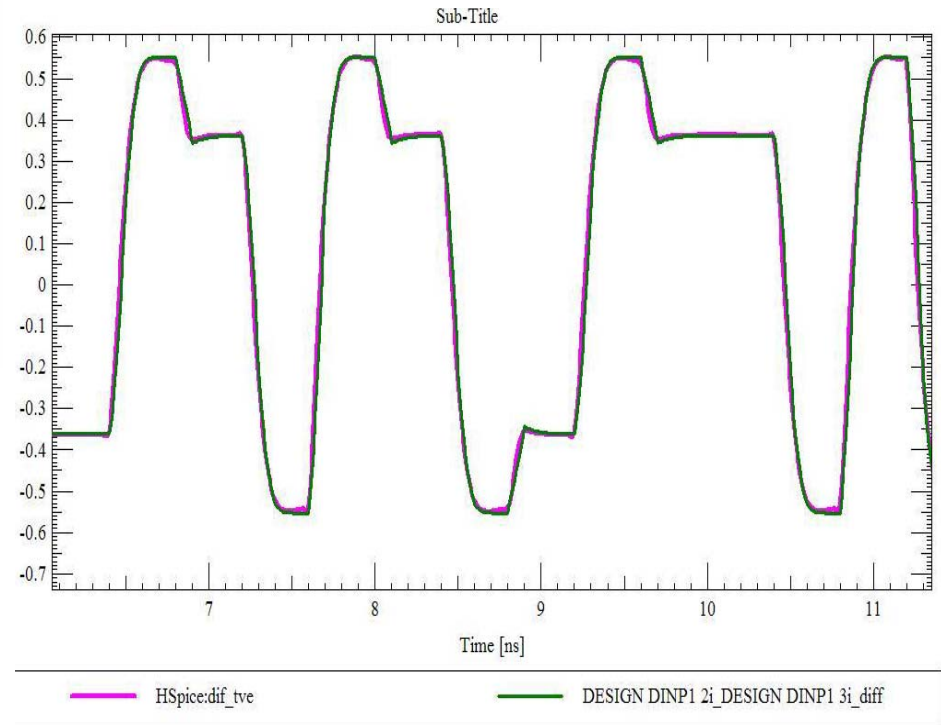


Validations and Optimizations

- DEq = 8, DTx = 0, HiLoDrv = 0

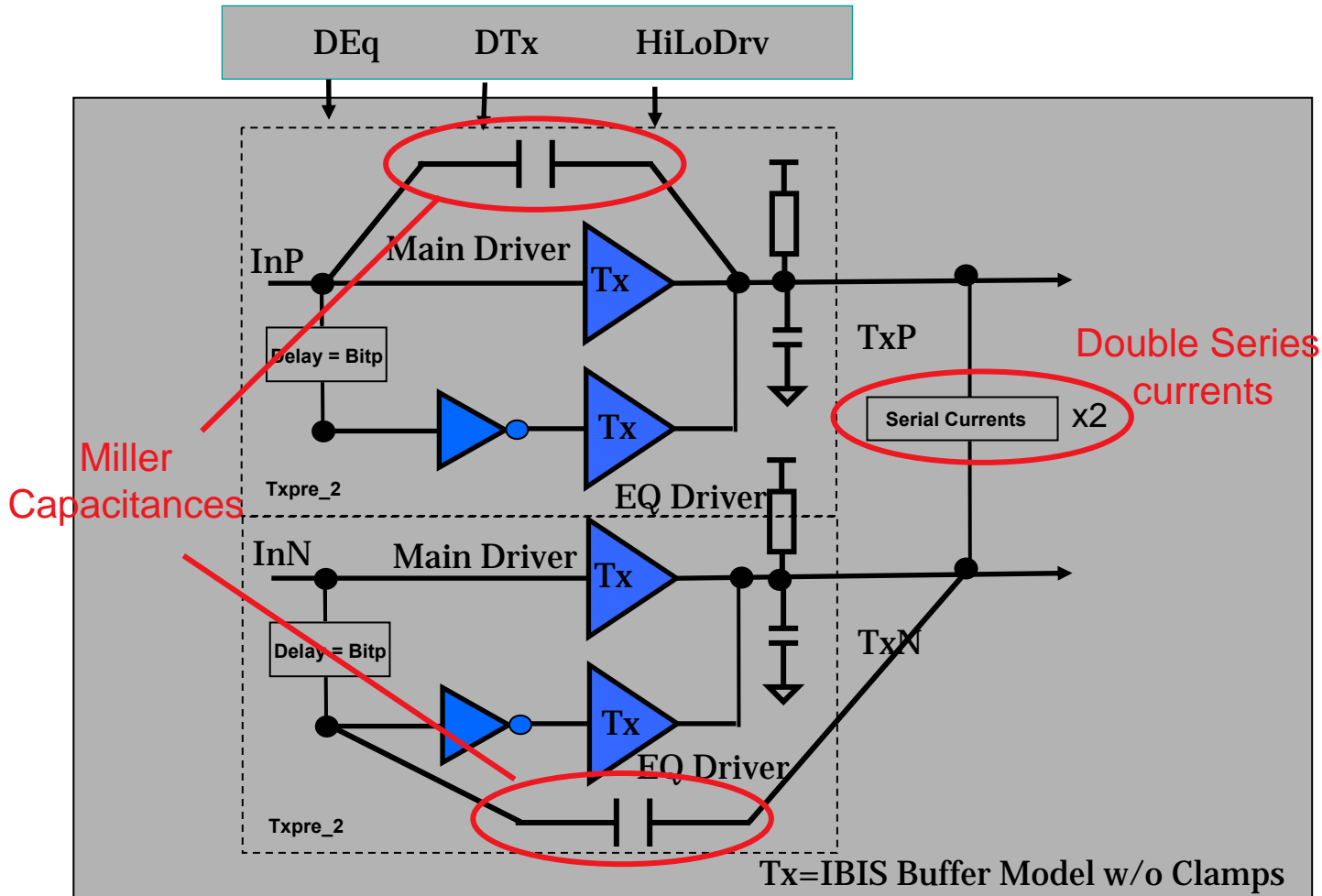


- Added one more series_switch on parallel
- Added Miller Capacitances

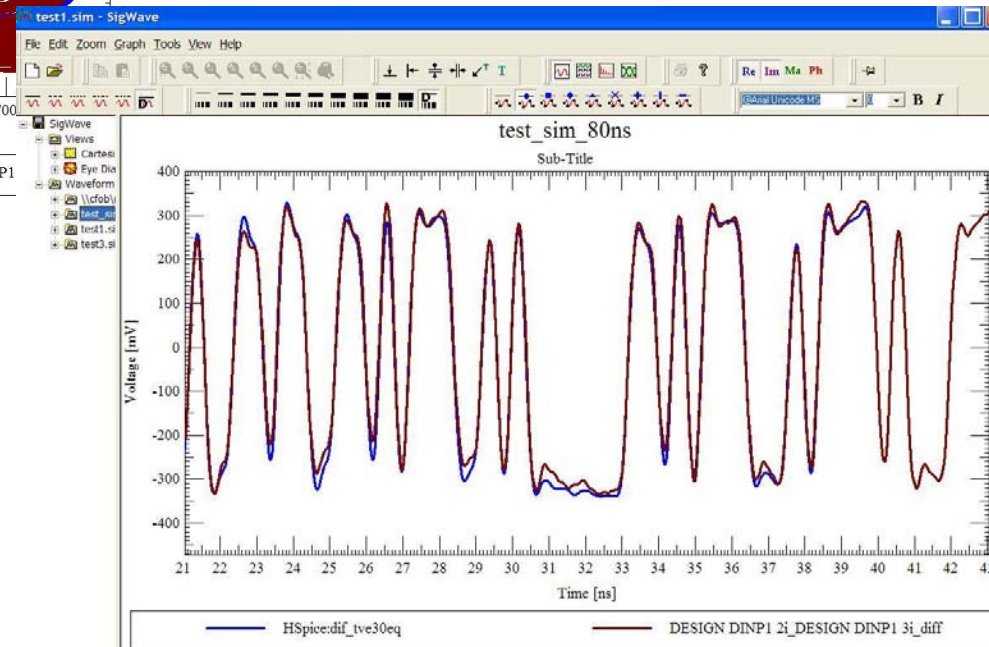
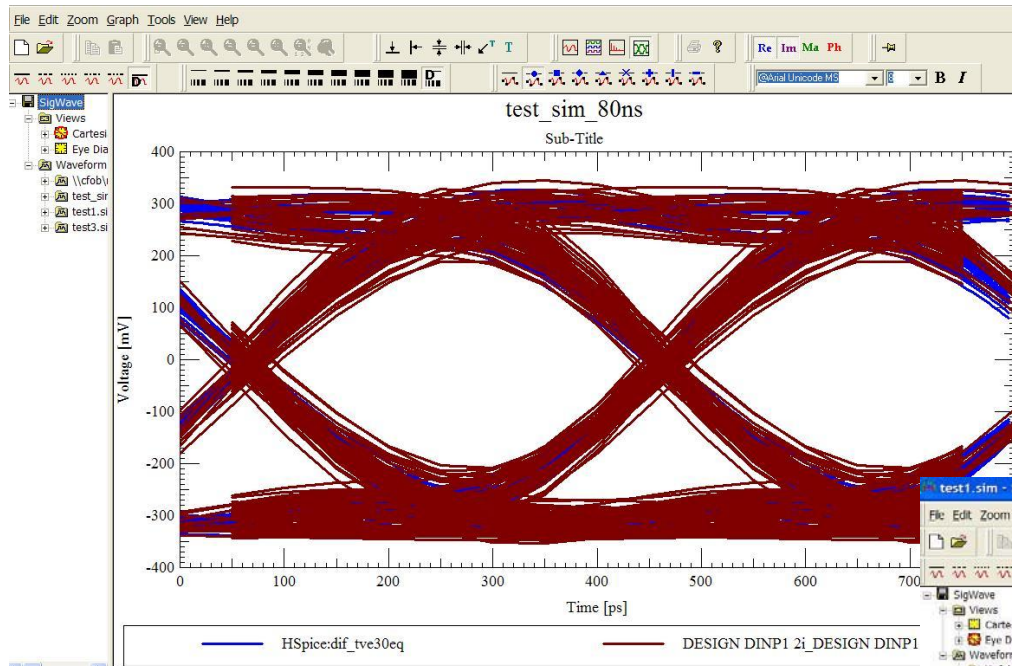


Macromodeling Steps

- Understanding Structures




Simulation Results 30" Backplane



Simulation Time (WinXp, 2.1GHz CPU, 2GB RAM)		
IBIS Macromodels		Transistor Models
PCB SI (3000 bits)	HSpice (2000 bits)	HSpice (2000bits)
12mins.	7mins.	1.5 hrs



Outline

- PCI Express 3.125 Gbps Serial Link
- Macromodeling Steps
- IBIS 4.2 Spice Macromodeling
- Validations and Optimizations
-  Conclusions

Conclusions

- Spice Macromodeling using IBIS 4.2 [External Model] is accurate and much faster than transistor-level models
- Spice Macromodeling is durable and can work on existing Spice simulators
 - Understanding the structure is the key
- IBIS future enhancement requests
 - Open IBIS for other commercial Spice simulators
 - Spice [External Model] needs to pass Parameters too
 - “Self-containing” IBIS Buffer from [External Model] is required for Spice Macromodeling. (Some commercial Spice simulators have this capability already)



Thank You!

- Acknowledgements / References
 - CDNLive Silicon Valley Paper from Nirmal Jain @Rambus
 - IBIS Summit 2003, True Diffpair Modeling, Arpad Muranyi @Intel
 - IBIS Cookbook