Case Study: Spice Macromodeling for PCI Express using IBIS 4.2

Lance Wang
Email: lwang@cadence.com
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Outline

- PCI Express Serial Link
  - Macromodeling Steps
  - IBIS 4.2 Spice Macromodeling
  - Validations and Optimizations
  - Conclusions
The PCI Express Environment

Driver -> Channel -> Receiver

- Add-in card via
- Board via
- Package
- Silicon/Package Parasitics
- PCI Express connector
- Board trace
- Switch

Inter Symbol Interference/Attenuation

Low Pass Filter

1.25GHz
Overcoming ISI using Transmit Equalization (De-Emphasis)

Transmitter > 40” FR4 < At Receiver

2.5Gbps, PRBS\(^7\) No Eq.

2.5 Gbps PRBS\(^7\) -3.5 dB Eq.

Transmit Equalization

PCI-Exp Features (Example)

EQ Control = 4 bit wide DEq bits
Swing Control = 4 bit wide DTx, & HI/LO DRV bits
Outline

• PCI Express Serial Link
• Macromodeling Steps
  • IBIS 4.2 Spice Macromodeling
  • Validations and Optimizations
  • Conclusions
Macromodeling Steps  
- Understanding Structures
Macromodeling Steps
- True Differential Pair IBIS Models Extraction

- Common Mode I-V Tables
  - Pull-up
  - Pull-Down
  - Clamp to represent Rterm
- Differential Model
  - Non linear Series Mosfet Representation
  - Linear Resistor Representation

- V-t Table
  - Recommended to have 2 sets of curve for each TxP and TxN
    - 1)Low –High 2)High-Low
- C_Comp/Cdiff
  - Represents C of transistors, die pads and on-chip interconnects. It does not include pkg C
Macromodeling Steps
- Extracting Common and differential Mode Currents

- Pull up and Pull Down Common Mode and differential Mode Current
  - $V_p = V_n$ we are measuring common mode current
  - When $V_p \neq V_n$, we are measuring common + differential currents
  - To get the differential current, we need to subtract the common mode current

- I-V Table Extraction for Clamp Data & On-Die Termination
  - One way to include on-die termination is to use superposition and add the termination currents to the diode currents in the clamp sections
  - Clamps are always active in an IBIS model, regardless of whether the buffer is driving or receiving.
Macromodeling Steps
- In & Ip Surface Plots of Total Current
Macromodeling Steps
- V-t Data Extraction

V-t Table
V_fixture = 0V
V_fixture = 1.8V
R_fixture=
Typical load of 50 ohms
Pad Capacitance: Common and differential Ccomp

- Run frequency domain simulations (.AC) with the above circuit
  - Give one of the AC sources 0 V AC amplitude (makes it a DC source)
  - Give the other AC source a small AC amplitude (1 mV)
  - Give both of the sources an appropriate DC bias
- Calculate capacitance using:
  \[ C = \frac{\text{Im}(I)}{2\pi f \times \text{Amplitude}} \]
  - For \( C_{\text{common}} \) use the current of the “DC” source
  - For \( C_{\text{diff}} \) use the current of “AC” source minus “DC” source
- Repeat everything at different DC bias voltages
Macromodeling Steps
- Pull Up, Pull Down and Clamp Curves

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<thead>
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<th>Voltage</th>
<th>I(typ)</th>
<th>I(min)</th>
<th>I(max)</th>
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<td>1.78</td>
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<tr>
<td>1.76</td>
<td>2.09E-02</td>
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<tr>
<td>0.04</td>
<td>4.31E-03</td>
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<td>2.19E-03</td>
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<tr>
<td>1.78</td>
<td>-2.87E-02</td>
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<tr>
<td>0.04</td>
<td>5.27E-03</td>
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<td>0.02</td>
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<td>6.14E-03</td>
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Macromodeling Steps
- Understanding Structures

DEq  DTx  HiLoDrv

InP  Main Driver  Tx  TxP
  Delay = 0
  Txpre_2

InN  Main Driver  Tx  TxN
  Delay = Bitp
  Txpre_2

EQ Driver

Tx=IBIS Buffer Model
Separating the differential mode current

• The off-diagonal current values represent the sum of the common and differential mode currents

• To obtain the differential mode currents alone, “normalize” the surface so that its diagonal values become zero
  – Subtract the common mode component from the surface and use it for the Series [Model]’s [R Series], [Series Current], [Series MOSFET], etc… keywords
  – If the surface is linear (flat) [R Series] is sufficient
  – Otherwise use the [Series Current] or [Series MOSFET] keywords
  – Slice the surface along the necessary voltage value(s) to satisfy the syntax requirement of the IBIS keyword used
Macromodeling Steps
- Understanding Structures

**Macromodeling Steps**

- Understanding Structures

**Main Driver**
- EQ Driver
- Delay = Bitp
- Serial Current

**Tx=IBIS Buffer Model**

- DEq
- DTx
- HiLoDrv

**Diagram**

- InP
- Main Driver
- Txpre_2
- Delay = 0

- InN
- Main Driver
- Txpre_2
- Delay = Bitp

- TxP
- TxN

- TX
Macromodeling Steps
- Coefficient table for HiLoDrv, DEq and DTx

* coefficient to control the current source
.param ctrlcoef='if(hilodrv == 0) (1.00)
+ elseif(hilodrv == 1) (0.50)
+ elseif(hilodrv == 2) (1.4) else(1)‘…….
+…….

* coefficient to control dtx bits
.param dtxcoef='if(dtx == 0) (1)
+ elseif(dtx == 1) (1.05)
+ elseif(dtx == 2) (1.1)
+ elseif(dtx == 8) (0.6)………
+…………

* coefficient to control the eq bits
.param deqcoef='if(deq == 0) (1.0)
+ elseif(deq == 1) (0.96)
+ elseif(deq == 2) (0.92)
+ elseif(deq == 3) (0.88)
+ elseif(deq == 4) (0.84)…….
+…….

HSpice is capable for this circuit.
Macromodeling Steps
- Understanding Structures

- Main Driver
- EQ Driver

DEq, DTx, HiLoDrv

TxP

InP

Delay = 0

Txpre_2

Tx

EQ Driver

Serial Current

TxN

InN

Delay = Bitp

Txpre_2

Tx

EQ Driver

Tx=IBIS Buffer Model
Macromodeling Steps
- Output Block Example

.subckt txpre_2 nvdd out ngnd in en
+ bitp=400p inv0=0 inv1=1
+ cf0=1 cf1=0 scale=1 padcap=1.2p ampctrl=1

* Here are the subcircuit calls for the tap inputs
xin0 in0 in ngnd delayin inv=inv0
xin1 in1 in ngnd delayin inv='inv1' del='bitp'

xtx0 nvdd out ngnd in0 en tx sclpux='scale*cf0*ampctrl' sclpdx='scale*cf0*ampctrl'
xtx1 nvdd out ngnd in1 en tx sclpux='scale*cf1*ampctrl' sclpdx='scale*cf1*ampctrl'

* This is the subcircuit definition for tx, used for the taps.
.subckt tx nvdd out ngnd in en sclpux=1 sclpdx=1
bdrv nvdd out ngnd in en Model=BUFF File=ibis_file
+ VIScale_pullup='sclpux'
+ VIScale_pulldown='sclpdx'
.ends tx

HSpice is capable for this circuit.
Macromodeling Steps
- P & N Pins

* P side driver subcircuit call
xp nvdd outp ngnd in en txpre_2 BUFF=BUFF ibis_file=ibis_file
+ bitp=bitp inv0=inv0 inv1=inv1
+ scale=scale
+ cf0=cf0
+ cf1=cf1
+ rt=rt
+ ampctrl=ampctrl

* N side driver subcircuit call
xn nvdd outn ngnd inn en txpre_2 BUFF=BUFF ibis_file=ibis_file
+ bitp=bitp inv0=inv0 inv1=inv1
+ scale=scale
+ cf0=cf0
+ cf1=cf1
+ rt=rt
+ ampctrl=ampctrl

HSpice is capable for this circuit.
Macromodeling Steps
- Understanding Structures

Main Driver

DEq

DTx

HiLoDrv

TxP

Serial Currents

Tx=IBIS Buffer Model
Outline

- PCI Express Serial Link
- Macromodeling Steps
- IBIS 4.2 Spice Macromodeling
  - Validations and Optimizations
  - Conclusions
Wrap into IBIS 4.2

```
[IBIS Ver] 4.2
[File Name] pcie_rs2314.ibs
[File Rev] 1.0
[Date] 4/7/2006
[Source] Converted from PCIe Macromodel
[Notes]  
[Disclaimer]  
[Copyright] Copyright 2006,
[Component] rs2314_tx
[Manufacturer] ABC Inc.

<table>
<thead>
<tr>
<th></th>
<th>typ</th>
<th>min</th>
<th>max</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_pkg</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
</tr>
<tr>
<td>L_pkg</td>
<td>1e-013</td>
<td>1e-013</td>
<td>1e-013</td>
</tr>
<tr>
<td>C_pkg</td>
<td>1e-015</td>
<td>1e-015</td>
<td>1e-015</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PIN</th>
<th>signal_name</th>
<th>model_name</th>
<th>R_pin</th>
<th>L_pin</th>
<th>C_pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>txoutp</td>
<td>pcie_behav</td>
<td>0.086</td>
<td>4.3e-009</td>
<td>0.72e-012</td>
</tr>
<tr>
<td>B1</td>
<td>txoutn</td>
<td>pcie_behav</td>
<td>0.086</td>
<td>4.3e-009</td>
<td>0.72e-012</td>
</tr>
<tr>
<td>Base</td>
<td>test_single</td>
<td>behav_base</td>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>

[Diff PIN] inv_pin vdiff tdelay_typ tdelay_min tdelay_max
| A1 | B1 | 200Cmv | 0    | 0    | 0      |

[Model] pcie_behav
| need to use *.diff for ture differential pair models
Model_type Output_diff

Pref Diff = 100
```
Wrap into IBIS 4.2

---

```plaintext
[Model] pole_behavior

  need to use * diff for true differential pair models
Model_type Output_diff

# Ref_diff = 100

# Other model subparameters are optional
[Typ]
  typ min max
  Voltage Range 1.5 1.5 1.5

# Ramp
SV/Drift 300mV/95ps 240mV/80ps 360mV/110ps
SV/Drift 300mV/95ps 240mV/80ps 360mV/110ps

[External Model]

  Assign SPICE

  Corner corner_name file_name circuit_name .subckt_name
  Specify the corners
  Corner Typ pole.spc pole_behavior
  Corner Min pole.spc pole_behavior
  Corner Max pole.spc pole_behavior

  # Parameter definitions
  # prefix BUFF will be treated as buffer model setting.
  Parameters BUFF_behavior_base
  # all regular parameters are here. Change them for different settings
  Parameters tr=40
  Parameters tr=1.60
  Parameters tr=50
  Parameters tr=50
  Parameters hida=0

  # Ports List of port names (in same order as in SPICE)
  Ports A_poref A_sgnal pos A_poref my_drive
  Ports A_poref A_sgnal neg A_sgnal_neg

  D_to_A D_port port1 port2 vlow which trisf trisf corner_name
  D_to_A D_drive my_drive A_poref 0.0 1.0 95p 95p typ
  D_to_A D_drive my_drive A_poref 0.0 1.0 80p 80p Min
  D_to_A D_drive my_drive A_poref 0.0 1.0 110p 110p Max
  D_to_A will be used as enable my_drives
  # vlow and trisf will be the ramping data
  
  no A_to_D required

[End External Model]
```
Outline

- PCI Express Serial Link
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Validations and Optimizations
- $\text{DEq} = 0$, $\text{DTx} = 0$, $\text{HiLoDrv} = 0$

- Use combined die capacitor instead of $C_{\text{comp}}$ in IBIS model
- Use combined on-die terminator instead of clamps
- Adjust DEq and DTx initial levels
Macromodeling Steps
- Understanding Structures

On-die terminators & Capacitance

Tx=IBIS Buffer Model w/o Clamps
Validations and Optimizations
- DEq = 8, DTx = 0, HiLoDrv = 0

- Added one more series_switch on parallel
- Added Miller Capacitances
Macromodeling Steps
- Understanding Structures

- Tx = IBIS Buffer Model w/o Clamps
- Main Driver
- EQ Driver
- Delay = Bitp
- InP
- InN
- DEq, DTx, HiLoDrv
- Serial Currents x2
- Double Series currents
- Miller Capacitances

Tx=IBIS Buffer Model w/o Clamps
Simulation Results 30” Backplane

Simulation Time
(WinXp, 2.1GHz CPU, 2GB RAM)

<table>
<thead>
<tr>
<th>IBIS Macromodels</th>
<th>Transistor Models</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB SI (3000 bits)</td>
<td>HSpice (2000 bits)</td>
</tr>
<tr>
<td>12mins.</td>
<td>7mins.</td>
</tr>
</tbody>
</table>
Outline

• PCI Express 3.125 Gbps Serial Link
• Macromodeling Steps
• IBIS 4.2 Spice Macromodeling
• Validations and Optimizations

Conclusions
Conclusions

- Spice Macromodeling using IBIS 4.2 [External Model] is accurate and much faster than transistor-level models
- Spice Macromodeling is durable and can work on existing Spice simulators
  - Understanding the structure is the key
- IBIS future enhancement requests
  - Open IBIS for other commercial Spice simulators
  - Spice [External Model] needs to pass Parameters too
  - “Self-containing” IBIS Buffer from [External Model] is required for Spice Macromodeling. (Some commercial Spice simulators have this capability already)
Thank You!

- Acknowledgements / References
  - CDNLive Silicon Valley Paper from Nirmal Jain @Rambus
  - IBIS Summit 2003, True Diffpair Modeling, Arpad Muranyi @Intel
  - IBIS Cookbook