IBIS Model Engineering for SI Simulation
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IBIS Model
As time goes by

Number of IBIS Model User

Usefulness

Increase

As time goes by
IBIS model goes mainstream

Time/Cost

all-at-once-ness

- Preparation
- Inspection
- Education
- Verification
Challenge to the SI simulation Engineering of PCB Design

**Post Layout Simulation**

- **Primary 1980s~**
  - Layout Design
  - SIM
  - ECO
  - Trial production
  - (Reduce the repeat count of trial production)
  - then
  - Sift
  - Reduce

- **Secondly 1990s~**
  - SIM
  - Layout Design
  - ECO
  - Trial production
  - (Reduce the time of ECO)

**Front loaded SI Engineering**

**Pre Layout Simulation**
SI Simulation

Modeling → Simulation → Correction

SI Management

Sim Result

Error has occurred
SI Simulation

- **Front loaded IBIS Engineering**
- **Modeling** → **Simulation** → **Sim Result**
- **Find Error** → **Correction** → **No backslide**
- **SI Management**
IBIS model Engineering as Front loaded SI Engineering
To minimized the time of SI simulation

- Incoming inspection for IBIS Model
  - Check IBIS Model
  - Verification IBIS Model
  - Correction IBIS Model
- Prepare IBIS Model
- Tune IBIS Model

Make decisions on SI view
Incoming inspection for IBIS Model

• Syntax Check

• I/O Cell Verification

Example:
Verification IBIS Model

Test circuit for IBIS Verification

Example:
• Correction IBIS Model

Example:

Erase and data interpolation

Shift
• Prepare IBIS Model

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<th>Signal</th>
<th>Model</th>
<th>R_pin</th>
<th>L_pin</th>
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Spiral pin number location

BGA
• Tune IBIS Model

More I-O H/L

Less I-O H/L

Detail Edit

Comparison-data for the best result

Real and Virtual Wave
What the SI Electronics whiz dose for IBIS?

Schematic

IBIS Model looks good. Need series termination. Topology should be Daisy

Simulation with leading hypothesis

Engineering instruction to Layout designer

Keep the space of place for series resistor in advance
What the Non SI Electronics whiz may do?

Schematic
IBIS Model
IBIS Model
IBIS Model
Simulations with
groundless suspicion

No SI view
Try & error
NG

Engineering instruction to Layout designer

Keep the space of place for series resistor if it’s possible

PCB under suspicion

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IBIS model Engineering as Front loaded SI Engineering

IBIS Model

|****************************************************
[Model] A  
Model_type  I/O  
Polarity    Non-Inverting  
Enable      Active-Low  
Vinl = 0.66V  
Vinh = 2.00V  
C_comp 2.55pF 1.18pF 3.91pF  
[Voltage Range] 3.3V 3.0V 3.6V  
[Power Clamp Reference] 3.3V 3.0V 3.6V  
[GND Clamp Reference] 0.0V 0.0V 0.0V  
[Pullup Reference] 3.3V 3.0V 3.6V  
[Pulldown Reference] 0.0V 0.0V 0.0V  
[Temperature Range] 49.0 125.0 -20.0 |
|****************************************************

Predict Signal Wave from IBIS Model
IBIS model Engineering as Front loaded SI Engineering

- Take a look (evaluate a symptom) of Output Current
- Take a look (evaluate a symptom) of Rise/Fall Speed
- Take a look (evaluate a symptom) of Signal amplitude

- Trend prediction for Routing Topology, Cross Talk, etc

<table>
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<th>Procurement IBIS model</th>
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To minimized the time of SI simulation

Pre Layout Simulation

Secondly 1990s~

Prevention of the backslide

NEXT 2000s~

Front loaded SI Engineering

(Reduce the time of SIM)

As far in advance as possible
Usefulness & Comfortable

Creative Engineering imagination comes into practical use

IBIS model goes mainstream
Make IBIS more comfortable
もっとIBISを快適に

Tune
Indicate & Designation
Verify

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