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Enhanced Macromodels for I/O Buffers

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Agenda

1. Macromodels for SI&PI: Requirements
2. Two-piece Macromodels: overview and general model structure
3. Validation tests – Single-ended and Differential Drivers
4. Conclusions and Future Development
Macromodels for SI/PI: Requirements

**General macromodel structure**

\[ i_{\text{out}}(t) = F(IN, v_{\text{out}}(t), v_{dd}(t)) \]
\[ i_{dd}(t) = G(IN, v_{\text{out}}(t), v_{dd}(t)) \]

**Requirements for SI/PI Co-Simulation:**

- Accuracy of currents and voltages at output and supply ports
- \( i_{dd}(t) \) & \( v_{dd}(t) \) & \( v_{\text{out}}(t) \) mutual effects (distortions & timing)
- Speed-up factors, compatibility with SPICE solver, ...
Two-Piece Macromodels

\[ i_{out} = F(IN, v_{out}, v_{dd}) \]
\[ i_{dd} = G(IN, v_{out}, v_{dd}) \]

\[ i_{out} = w_H i_H + w_L i_L \]
\[ i_{dd} = w_H i_{dH} + w_L i_{dL} + \delta_i \]

Most state-of-the-art macromodels adopt a “two-piece” structure.
Key differences are:
- \( w_{H/L}(t) \) vs \( w_{H/L}(t, v_{dd}(t)) \)
- Approximations on \( i_{H/L} \) (static & dynamic)
- Estimation of \( \delta_i \)
- ...
Static & Dynamic Characteristics: IBIS

For a given input-state (H,L):

- output static characteristics are extracted with a .DC sweep. Results stored in I-V tables (PU/PD)
- output dynamic characteristic corresponds to the \( i-v \) behavior of a capacitor \( C_{COMP} \)

\[
I_{out,static} + i_{out,dynamic} = i_{out}
\]
Weighting Functions: IBIS

(At least) two .TRAN simulations are needed to characterize the rising and falling switching behaviour of the output port. Output voltages are stored in V-t tables.

The SPICE solver uses the tables to solve a 2EQ/2UK problem, and extracts $K_U(t)$ and $K_D(t)$.

$$\forall t: \begin{cases} i_{out,1} = k_U (I_{H1} + i_{H1}) + k_D (I_{L1} + i_{L1}) \\ i_{out,2} = k_U (I_{H2} + i_{H2}) + k_D (I_{L2} + i_{L2}) \end{cases}$$

$$[k_U] = \begin{bmatrix} (I_{H1} + i_{H1}) & (I_{L1} + i_{L1}) \\ (I_{H2} + i_{H2}) & (I_{L2} + i_{L2}) \end{bmatrix}^{-1} [i_{out,1}]$$

Weighting Functions

$k_U = 1$

$k_D = 1$

$k_D = 0$

$k_U = 0$
Supply Current: IBIS

From IBIS v5.0 onwards, IBIS model structure has been extended in order to **model supply-current profiles**.

Using the **same .TRAN simulations**, supply-current profile \( i_{COMP1,2} \) is stored in \( I_{COMP} - t \) tables.

From \( I_{COMP} - t \) **tables**, Pre-Driver/Crowbar current can be computed as

\[
i_{PRE} = i_{COMP} - i_{out}
\]
Supply-Dependency: IBIS

\[ V_{DD} \text{ (nominal)} \]

\[ i_{SSO\_PU} \]

\[ V_{DD} \text{ (nominal)} \]

\[ i_{SSO\_PD} \]

SSO\_PU(PD) tables obtained from .DC sweeps:
- VDD(VSS) changes
- output node is tied to GND(VDD)

\[
K_{sso\_pd}(Vtable\_pd) = \frac{I_{sso\_pd}(Vtable\_pd)}{I_{sso\_pd}(0)}
K_{sso\_pu}(Vtable\_pu) = \frac{I_{sso\_pu}(Vtable\_pu)}{I_{sso\_pu}(0)}
\]

\[ IBIS\ v6.0,\ pg.60 \]

\[ K_{pu}(t)I_{pu}(Vcc-Vout(t)) \]

\[ K_{pd}(t)I_{pd}(Vout(t)) \]

KSSO\_PU/PD modulate the output static characteristics to reproduce supply-variations effects

The approximation deviates from DUM’s 3D static char

Same issue affects also standard MPILOG models!
Proposed Enhancements: Static Characteristics

The static characteristics are now extracted with **nested .DC sweeps** at **output and supply** ports.

1 output, 1 supply, 1 current: 3D-surface

\[ I_S = F(V_{out}, V_{dd}) \]

Such 3D surfaces are calculated for:

\[ I_{SH}(V_{out}, V_{dd}) \]
\[ I_{SL}(V_{out}, V_{dd}) \]
\[ I_{dd,SH}(V_{out}, V_{dd}) \]
\[ I_{dd,SL}(V_{out}, V_{dd}) \]
SVD Approximation of 3D Surfaces

\[ Y, \text{ samples @ } V_{out}, V_{dd} \text{ from SPICE and .dc sweeps} \]

\[ y \approx F(V_{out}, V_{dd}) = \sum_{k=1}^{N} \sigma_k \varphi_{1,k}(V_{out}) \varphi_{2,k}(V_{dd}) \]

SVD-approximation can be written as:

- SPICE Netlist (VCVS, CCCS, ...)
- Verilog-A Code

**Truncation Process:**
Maximum compactness meeting target accuracy
Proposed Enhancements: Dynamic Characteristics

Dynamic characteristics are reproduced by rational approximations obtained post-processing the simulation results using Time-Domain Vector-Fitting (TD-VF) algorithms. These models are computed for:

\[ i_{out,H}(v_{out}, v_{dd}) \]
\[ i_{out,L}(v_{out}, v_{dd}) \]
\[ i_{dd,H}(v_{out}, v_{dd}) \]
\[ i_{dd,L}(v_{out}, v_{dd}) \]

and implemented as:
- SPICE Netlist
- Verilog-A models
Proposed Enhancements: Weighting Functions

\( V_{dd} \in [80\%, \ldots, 100\%, \ldots, 120\%] \times V_{DD} \) (nominal)

Weighting functions \( w_H \) and \( w_L \) are calculated for several \( V_{dd} \) values.

This allows the creation of 3D-surfaces \( w_H(t, v_{dd}) \) and \( w_L(t, v_{dd}) \) reproducing the complex dependency of the switching events on VDD.
## Comparative Summary

<table>
<thead>
<tr>
<th></th>
<th>IBIS v5.1</th>
<th>PROPOSED</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Output Static</strong></td>
<td>2D I-V Tables</td>
<td>3D Surfaces $F_x(V_{out}, V_{dd})$</td>
</tr>
<tr>
<td><strong>Output Dynamic</strong></td>
<td>Capacitive $C_{COMP}$</td>
<td>State-space models $f_x(v_{out}, v_{dd})$</td>
</tr>
<tr>
<td><strong>Weighting Functions</strong></td>
<td>2EQ/2UK @VDD$_{NOM}$ $k_U(t)$</td>
<td>3D Surfaces $w_{L2H}(t, v_{dd})$ and $w_{H2L}(t, v_{dd})$</td>
</tr>
<tr>
<td></td>
<td>and $k_D(t)$</td>
<td></td>
</tr>
<tr>
<td><strong>Supply Current</strong></td>
<td>$I_{COMP} - t$ Table</td>
<td>3D Surface $\delta_i(t, v_{dd})$</td>
</tr>
<tr>
<td><strong>Supply Effects</strong></td>
<td>Static Modulation $K_{SSO_PU(PD)}$</td>
<td>3D surfaces &amp; MISO models Static/Dyn/Timing Effects</td>
</tr>
</tbody>
</table>
**MPILOG Model Implementation**

Mpiolog models can be synthesized as:

- **SPICE Netlists**
- **Verilog-A Modules**
- **IBIS (v5.1/6.0)**
- **IBIS** using [External Model]

```vss
IN
VDD
OUT
VSS
```

```launch
// Output + supply ports driver macromodel
// VERILOG-A implementation autogenerated by Mpiolog

'include "constants.vams"
'include "disciplines.vams"

// COMPLETE MACROMODEL
module mpiolog_model (v_in, v_io, vdd_io, ref_io, v_oe);

// ELECTRICAL VARIABLES
electrical v_in, v_io, vdd_io, ref_io, v_oe;
electrical w1, w2, f1, f2, fs1, fs2, f7, f57;
electrical f3, f4, fs3, fs4, d1, f8, fs8;
electrical u1, u2;

// PARAMETERS
parameter real PVDDcore=1; // logic core nominal voltage
parameter real PVDD=1.2; // output power-supply nominal voltage

analog begin
  // MODEL STRUCTURE...
```

```
[External Model]
Language Verilog-A(PS)

<table>
<thead>
<tr>
<th>Corner name</th>
<th>file name</th>
<th>circuit name (module)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Corner Typ</td>
<td>mpiolog.va mpiolog_model</td>
<td></td>
</tr>
<tr>
<td>Corner Min</td>
<td>NA NA</td>
<td></td>
</tr>
<tr>
<td>Corner Max</td>
<td>NA NA</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Ports List of port names (In same order as in Verilog-A(PS))</th>
</tr>
</thead>
<tbody>
<tr>
<td>v_in v_out vdd_io ref_io v_oe Ports my_drive A_signal_pos A_puref A_pdriver my_enable</td>
</tr>
</tbody>
</table>

[End External Model]
```
Validations: Ideal Supply

Good agreement! (output 😊, timing 😊, IBIS supply 😊)

Speed-up:
MPILOG x350+
IBIS x1500+

IBIS: timing 😌, output/supply 😌 -- MPILOG: timing/output/supply 😊😊
Validations: Non-Ideal PDN

IBIS: timing 😐, output/supply 😊
MPILOG: timing/output/supply 😊😊
Validations: LPDDR3 SI/PI Co-Simulation

Inaccurate predictions of supply-noise induced jitter can lead to wrong/dangerous estimations on system functionality/margins (e.g., $t_{SU}$, $t_H$, $t_{CK}$ in (LP-)DDR)

IBIS 😞 MPILOG 😊
Macromodeling of Differential I/O-Buffers

\[ \begin{align*}
    i_1 &= w_{H1}(t, v_{dd}) \cdot i_{H1}(\bar{v}) + w_{L1}(t, v_{dd}) \cdot i_{L1}(\bar{v}) \\
    i_2 &= w_{H2}(t, v_{dd}) \cdot i_{H2}(\bar{v}) + w_{L2}(t, v_{dd}) \cdot i_{L2}(\bar{v}) \\
    i_3 &= w_{H3}(t, v_{dd}) \cdot i_{H3}(\bar{v}) + w_{L3}(t, v_{dd}) \cdot i_{L3}(\bar{v})
\end{align*} \]

where \( \bar{v} = (v_{OUTP}, v_{OUTN}, v_{dd}) \)

- Multi-dimensional Static Surfaces
- MIMO TDVF Dynamic Models
- 3D Weighting Functions (e.g., \( w_{H1}(t, v_{dd}) \))

This model structure (SPICE/Verilog-A) can be embedded in an IBIS file as an [External Model]
Low-Power Voltage-Mode Drivers

Output Swing and Common-Mode can be configured tuning an internal VREG

Reduced Swing to minimize power consumption

Impact of LDO performance on output signals

Perturbations $\partial_i(t)$ across $i_{NOM}$ introduce voltage bounce $\Delta V_{LDO}(t)$ (depending on LDO dynamics)

• Distortions on output signals
**Validation Test**

**PROPOSED** model structure:
\( V_{\text{REG}} \)-induced effects are correctly captured
*(Signal distortion, common-mode noise, ...)*

**IBIS** model-structure cannot reproduce
the effects introduced by the internal \( V_{\text{REG}} \).
*(\( V-t \) vs "long" \( V_{\text{REG}} \) regulation transient)*
*(\( I-V & C_{\text{COMP}} \) vs complex \( Z_{\text{LDO}}(f) \))*)
Conclusions and Future Enhancements

**Enhanced** two-piece model structure (to accurately reproduce output and supply ports):
- **SVD + truncation-process** for (multi-dimensional) Static Char.
- Multiple-Input **TDVF** for Dynamic Characteristic
- 3D switching characteristics \( w(t, V_{DD}) \)

**Flexible and modular** modelling solution
Model implementation in **SPICE/Verilog-A**

**IBIS compliant** (v5.1/6.0) via [External Model] keyword

**Validation tests** highlight **good speed-up** factors (x350 +) and **excellent accuracy** in **SI/PI co-simulations**

**What’s next?**
- Pre/De-Emphasis stages in high-speed transmitters
- Continuous-time linear equalizers in high-speed receivers
Thank you for the attention!