IBIS-AMI Modelling of High-Speed Memory Interfaces

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Motivation

• Memory interfaces are becoming harder to simultaneously meet high capacity requirements while maintaining high bandwidths

• To combat the signal degradations, equalization approaches are utilized (Tx de/preemphasis and Rx AFE & DFE) in conjunction with the traditional selection of on-die termination (ODT) and transmit driver impedance settings

• Leverage IBIS-AMI standards to model high-speed memory interfaces to provide system vendors information

• Present simulation results for 2.4 Gbps and 6.4 Gbps data transmission over the same channel with different equalization features

• Conclusion
Current DDR Signaling Trend for Datacenter and Enterprise Server Environments

Multi-drop topology of DDR bus causes channel loss, limits speed

Fundamental Challenge:
- Higher speed → less capacity per channel
- Requires more channels to maintain capacity
- Expensive, pkg/costs hard to scale

Overview of IBIS-AMI modelling of high-speed memory interfaces

- With shrinking voltage supplies and demand for mainstream memory data rates increasing, equalization approaches are necessary to combat noise.
- System vendors need models for these interfaces.
- IBIS-AMI is an excellent platform for semiconductor/IP vendors and system vendors to exchange information.
- Use IBIS-AMI standards with electrical response captured by .ibs and the behavioral response captured by .ami (& .dll / .so).
Encapsulating Multi-drop Passive Memory Channel

- AMI is really developed for point-to-point transmission (SerDes links)
- To enable the modelling of multi-drop, passive memory channels, the channel now includes the ODT of the peripheral channel
- Macromodel/S-parameter is then incorporated into the link simulation
System Identification of Analog Front End

- Used system identification to extract the poles and zeros of the transfer function from the AFE from SPICE simulations
- $H(s) \rightarrow H(z)$ through bilinear transform to discretize the transfer function which is subsequently integrated into the .ami portion of the receiver

$$z = e^{s \cdot T_s} = e^{\frac{2\pi \cdot f (UI/OSR)}{}}$$
Example of IBIS-AMI file format

- Here shows a typical format of the .ibs file which acts as the wrapper to call the .ami file along with the .so / .dll file
- .ibs wrapper are the electrical LUTs which define the nonlinearities of the electrical Tx and Rx impedance
- package model is typically extracted through electromagnetic simulations and will have an RLC or S-parameter format
- temperature and voltage ranges along with the input capacitance (C_comp) are defined
- .ami contains the variables which pass to the .dll or .so file along with the value range.
- Matlab/Simulink was used to model and encode the AMI portion of the macromodel along with Microsoft’s Visual Studio for C++ code development and GNU Compiler Collection (GCC)
Example of Tx and Rx modelled with IBIS-AMI operating at 2.4 Gbps

For 2.4 Gbps operation, only the Rx has CTE equalization with the transmit eye diagram plotted with two different ODT\textsubscript{1,2} settings as shown in (a-b) before the CTE without crosstalk whose reference voltage is adjusted to conform with single-ended (SE) pseudo-open drain logic (PODL) signaling typical of DDR4

(c-d) shows the eye diagram after the CTE where the SE signal is converted to a differential signal resulting with a reference voltage of 0 V with and without crosstalk, respectively

(e-f) show eye diagram with the inclusion of the random noise (RJ) and RJ plus voltage noise at the Rx, respectively

A comparison of the simulation time and EH / EW is shown in the below table indicating that IBIS-AMI models fairly represent the results of full-transistor models with a simulation time improvement of over 1000x the CPU time speed.

<table>
<thead>
<tr>
<th></th>
<th>Full-Transistor</th>
<th>IBIS-AMI</th>
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</thead>
<tbody>
<tr>
<td>Simulation Time</td>
<td>191.6 min</td>
<td>0.148 min</td>
</tr>
<tr>
<td>Accuracy</td>
<td>High</td>
<td>Med</td>
</tr>
<tr>
<td>At pad w/ ODT\textsubscript{2}</td>
<td>EW = 387 ps, EH = 290 mV</td>
<td>EW = 375 ps, EH = 295 mV</td>
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<tr>
<td>w/o xtalk after CTE</td>
<td>EW = 383 ps, EH = 581 mV</td>
<td>EW = 360 ps, EH = 580 mV</td>
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<tr>
<td>w/ xtalk after CTE</td>
<td>EW = 341 ps, EH = 454 mV</td>
<td>EW = 338 ps, EH = 480 mV</td>
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</table>
Example of Tx and Rx modelled with IBIS-AMI operating at 6.4 Gbps

- For advanced memory interfaces operating beyond DDR4, a DFE may be necessary to overcome post-cursor distortion associated with multi-drop topologies typical of high capacity, memory channels for server applications.
- As a demonstration of equalization effects, a two-tap DFE is used to open the eye at 6.4 Gbps using single-ended PODL signaling.
Conclusion

• As demand for main stream memory data rates increase, equalization approaches are necessary with shrinking voltage supplies and stagnant channel performance
• System vendors need models for these interfaces
• IBIS-AMI is an excellent platform for semiconductor/IP vendors and system vendors to exchange information
  ◦ Expand application of IBIS-AMI standard for high-speed memory interfaces
  ◦ Challenges include enabling IBIS-AMI for single-ended transmit/receiver and the accurate calculation of the DC value

• References: