IBIS Update

Mike LaBonte
SiSoft
Chair, IBIS Open Forum

EPEPS 2017 IBIS Summit
San Jose, CA
October 18, 2017

http://www.ibis.org/
26 IBIS Members

Number of Members by Year

IBIS Update
IBIS Officers 2017-2018

Chair:    Mike LaBonte, SiSoft
Vice-Chair: Lance Wang, IO Methodology Inc.
Secretary: Randy Wolff, Micron Technology
Treasurer: Bob Ross, Teraspeed Labs
Librarian: Anders Ekholm, Ericsson
Postmaster: Curtis Clark, ANSYS
Webmaster: Mike LaBonte, SiSoft

2018 Officer Election nominations open May 17
IBIS Meetings

• Weekly teleconferences
  – Quality Task Group (Tuesdays)
  – Advanced Technology Modeling Task Group (Tuesdays)
  – Interconnect Task Group (Wednesdays)
  – Editorial Task Group (some Fridays)

• IBIS Open Forum teleconference every 3 weeks
  – 486 meetings so far

• IBIS Summit meetings: DesignCon, IEEE SPI, EDICON USA, EPEPS, Shanghai, Taipei, Tokyo
SAE ITC

- SAE Industry Technologies Consortia is the parent organization of the IBIS Open Forum
- IBIS is assisted by SAE employees Thomas Munns, Phyllis Gross, Dorothy Lloyd
- SAE ITC provides financial, legal, and other services

http://itc.sae.org/
Task Groups

• Interconnect Task Group
  – Chair: Michael Mirmak
  – http://ibis.org/interconn_wip/
  – Develop on-die/package/module/connector interconnect modeling BIRDs

• Advanced Technology Modeling Task Group
  – Chair: Arpad Muranyi
  – http://ibis.org/atm_wip/
  – Develop most other technical BIRDs

• Quality Task Group
  – Chair: Mike LaBonte
  – http://ibis.org/quality_wip/
  – Oversee IBISCHK parser testing and development

• Editorial Task Group
  – Chair: Michael Mirmak
  – http://ibis.org/editorial_wip/
  – Produce IBIS Specification documents
IBIS Milestones

I/O Buffer Information Specification

• 1993-1994 **IBIS 1.0-2.1:**
  – Behavioral buffer model (fast simulation)
  – Component pin map (easy EDA import)

• 1997-1999 **IBIS 3.0-3.2:**
  – Package models
  – Electrical Board Description (EBD)
  – Dynamic buffers

• 2002-2006 **IBIS 4.0-4.2:**
  – Receiver models
  – AMS languages

• 2007-2012 **IBIS 5.0-5.1:**
  – IBIS-AMI SerDes models
  – Power aware

• 2013-2015 **IBIS 6.0-6.1:**
  – PAM4 multi-level signaling
  – Power delivery package models

• 2018? **IBIS 7.0**

Current development

Other Work

• 1995: **ANSI/EIA-656**
  – IBIS 2.1

• 1999: **ANSI/EIA-656-A**
  – IBIS 3.2

• 2001: **IEC 62014-1**
  – IBIS 3.2

• 2003: **ICM 1.0**
  – Interconnect Model Specification

• 2006: **ANSI/EIA-656-B**
  – IBIS 4.2

• 2009: **Touchstone 2.0**

• 2011: **IBIS-ISS 1.0**
  – Interconnect SPICE Subcircuit specification
IBIS Version Development

As of 18-Oct-2017
# Possible IBIS 7.0 Timeline

<table>
<thead>
<tr>
<th>Meeting Date</th>
<th>Milestone</th>
</tr>
</thead>
<tbody>
<tr>
<td>4/21/2017</td>
<td>Vote to establish 7.0 as the next IBIS version passes</td>
</tr>
<tr>
<td>5/12/2017</td>
<td>BIRD review and acceptance (6 meetings)</td>
</tr>
<tr>
<td>9/15/2017</td>
<td>BIRD review and acceptance (4 meetings)</td>
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<tr>
<td>12/8/2017</td>
<td>Vote to approve 7.0 BIRD set is scheduled for next meeting</td>
</tr>
<tr>
<td>1/5/2018</td>
<td>7.0 BIRD set accepted. Editorial work begins</td>
</tr>
<tr>
<td>1/26/2018</td>
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<tr>
<td>2/16/2018</td>
<td></td>
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<tr>
<td>3/9/2018</td>
<td>Editorial announces 7.0 ready. Review period begins</td>
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<tr>
<td>3/30/2018</td>
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<tr>
<td>4/20/2018</td>
<td>Vote to ratify 7.0 scheduled for next meeting</td>
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<tr>
<td>5/11/2018</td>
<td>7.0 ratified</td>
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</table>

BIRD = Buffer Issue Resolution Document
<table>
<thead>
<tr>
<th>BIRD</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>147.6</td>
<td>Back-channel Support</td>
</tr>
<tr>
<td>158.5</td>
<td>AMI Ts4file Analog Buffer Models</td>
</tr>
<tr>
<td>179</td>
<td>New IBIS-AMI Reserved Parameter Special_Param_Names</td>
</tr>
<tr>
<td>180</td>
<td>Require Unique Pin Names in [Pin]</td>
</tr>
<tr>
<td>182</td>
<td>POWER and GND [Pin] signal_name as [Pin Mapping] bus_label</td>
</tr>
<tr>
<td>183</td>
<td>[Model Data] Matrix Subparameter Terminology Correction</td>
</tr>
<tr>
<td>184.2</td>
<td>Model_name and Signal_name Restriction for POWER and GND Pins</td>
</tr>
<tr>
<td>185.2</td>
<td>Section 3 Reserved Word Guideline Update</td>
</tr>
<tr>
<td>186.4</td>
<td>File Naming Rules</td>
</tr>
<tr>
<td>187.3</td>
<td>Format and Usage Out Clarifications</td>
</tr>
<tr>
<td>188.1</td>
<td>Expanded Rx Noise Support for AMI</td>
</tr>
<tr>
<td>189.4</td>
<td>Interconnect Modeling Using IBIS-ISS and Touchstone</td>
</tr>
<tr>
<td>191.2</td>
<td>Clarifying Locations for Si_location and Timing_location</td>
</tr>
<tr>
<td>192.1</td>
<td>Clarification of List Default Rules</td>
</tr>
</tbody>
</table>

Green = currently accepted BIRD
## BIRDs Possibly Excluded from IBIS 7.0

<table>
<thead>
<tr>
<th>BIRD</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>125.1</td>
<td>Make IBIS-ISS Available for IBIS Package Modeling</td>
</tr>
<tr>
<td>145.3</td>
<td>Cascading IBIS I/O buffers with [External Circuit]s using the [Model Call] keyword</td>
</tr>
<tr>
<td>161.1</td>
<td>Supporting Incomplete and Buffer-only [Component] Descriptions</td>
</tr>
<tr>
<td>166.2</td>
<td>Resolving problems with Redriver Init Flow</td>
</tr>
<tr>
<td>163</td>
<td>Instantiating and Connecting [External Circuit] Package Models with [Circuit Call]</td>
</tr>
<tr>
<td>164</td>
<td>Allowing Package Models to be defined in [External Circuit]</td>
</tr>
<tr>
<td>165</td>
<td>Parameter Passing Improvements for [External Circuit]s</td>
</tr>
<tr>
<td>181.1</td>
<td>I-V Table Clarifications</td>
</tr>
<tr>
<td>190</td>
<td>Clarification for Redriver Flow</td>
</tr>
</tbody>
</table>

White = currently not an accepted BIRD
**BIRD 147.6, Back-channel Support**

- Enable back-channel link training messages between the Tx and Rx executable models to enable link training to optimize equalization settings during time domain (AMI_GetWave) simulations.

- New AMI Parameters:
  - BCI_Protocol, BCI_State, BCI_ID, BCI_Message_Interval_UI, BCI_Training_UI
**IBIS Update**

**Link Training Back-channel**

- **Stimulus**
- **Tx**
  - Init
  - GetWave
- **Channel**
- **Rx**
  - GetWave
  - Init

- **BCI_State**
  - BCI_State = “Training”
  - BCI_State = “Done”

- **Back-channel File**
  - <BCI_ID>_PCIe3g.dat

- **Initial Tx Settings**
- **Initial Rx Settings**

- **Training Start**
- **Training Stop**

- **EDA Tool**
- **AMI Models**
- **Protocol-specific message file**

- **BCI_Protocol** = “PCIe3g”
  -Tx AMI Parameters
  -Rx AMI Parameters
BIRD 158.5, AMI Ts4file Analog Buffer Models

- Touchstone on-die analog models for IBIS-AMI models directly included from the AMI file, bypassing the analog model in the IBIS file.
- Same as “TStoneFile” models, now “Ts4file”.

Specification Development
BIRD 188.1, Expanded Rx Noise Support for AMI

• Bounded (uniform) Rx Noise must be supported by IBIS-AMI, separately from the existing Gaussian random Rx Noise parameter.

| Parameter: | Rx_Noise, Rx_GaussianNoise |
| Required: | No, and Rx_Noise is illegal before AMI_Version 6.0; No, and Rx_GaussianNoise is illegal before AMI_Version 7.0 |

| Parameter: | Rx_UniformNoise |
| Required: | No, and illegal before AMI_Version 7.0 |
**BIRD 189.4, Interconnect Modeling Using IBIS-ISS and Touchstone**

<table>
<thead>
<tr>
<th>Interconnect Model</th>
<th>Full_ISS_pad_pin_IO</th>
</tr>
</thead>
<tbody>
<tr>
<td>File_IBIS-ISS</td>
<td>full_pad_pin_io.iss</td>
</tr>
<tr>
<td>Number_of_terminals</td>
<td>8</td>
</tr>
</tbody>
</table>

1. Pin_Rail pin_name 1 | VCC_5.0 POWER
2. Pin_Rail pin_name 2 | VCC_3.3 POWER
3. Pin_I/O pin_name 3 | DATA1 DATA_MODEL
4. Pin_Rail pin_name 4 | VSS GND
5. Pad_Rail pad_name VCC1 | VCC_5.0 POWER
6. Pad_Rail pad_name VCC2 | VCC_3.3 POWER
7. Pad_I/O pin_name 3 | DATA1 DATA_MODEL
8. Pad_Rail pad_name VSS1 | VSS GND

[End Interconnect Model]

<table>
<thead>
<tr>
<th>Interconnect Model</th>
<th>Full_ISS_buf_pad_IO</th>
</tr>
</thead>
<tbody>
<tr>
<td>File_TS</td>
<td>full_buf_pad_io.s8p</td>
</tr>
<tr>
<td>Number_of_terminals</td>
<td>8</td>
</tr>
</tbody>
</table>

1. Pad_Rail pad_name VCC1 | VCC_5.0 POWER
2. Pad_Rail pad_name VCC2 | VCC_3.3 POWER
3. Pad_I/O pin_name 3 | DATA1 DATA_MODEL
4. Pad_Rail pad_name VSS1 | VSS GND
5. Buffer_Rail pin_name 1 | VCC_5.0 POWER
6. Buffer_Rail pin_name 2 | VCC_3.3 POWER
7. Buffer_I/O pin_name 3 | DATA1 DATA_MODEL
8. Buffer_Rail pin_name 4 | VSS GND

[End Interconnect Model Set]
[Thank You]

IBIS Open Forum:
Web: http://www.ibis.org
Email: ibis-info@freelists.org

We welcome participation by all IBIS model makers, EDA tool vendors, IBIS model users, and interested parties.