# Asian IBIS Summit – JAPAN,2024

## The Perspective of an IBIS User


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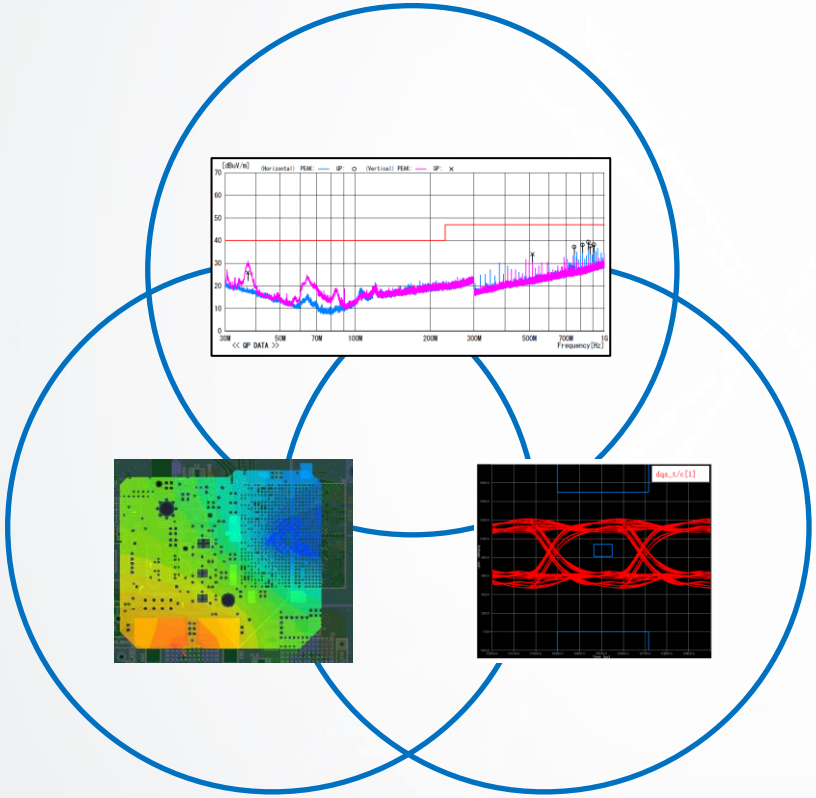
**ASTRODESIGN, Inc.**

# Agenda

- Review: Electrical Quality
- Serial and Parallel Data Transmission
- Serial Data Transmission’s Case
- Parallel Data Transmission’s Case
- Conclusion

# Review: Electrical Quality

> Electro-Magnetic Compatibility

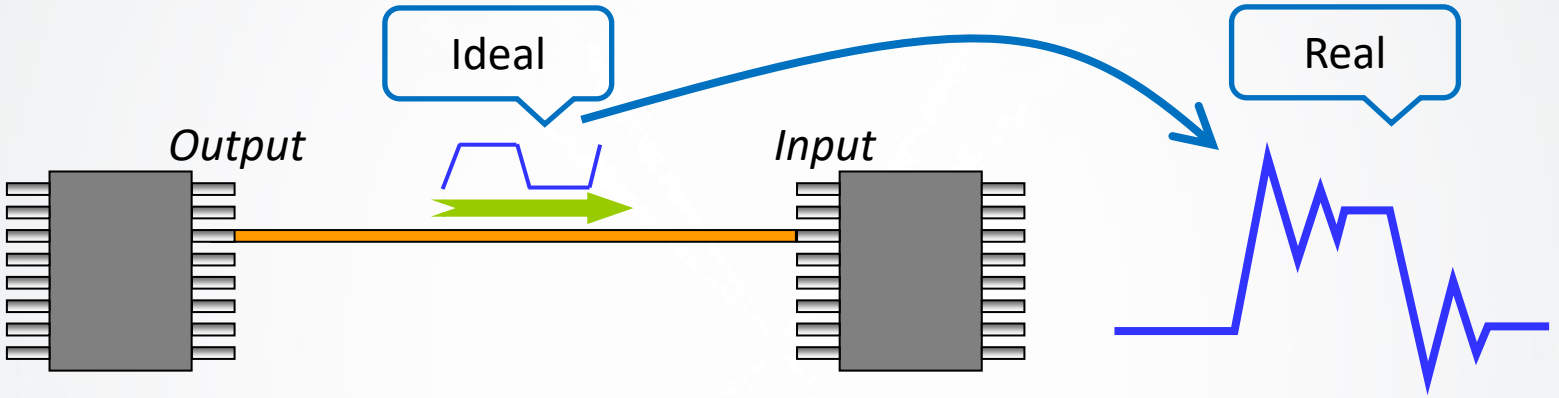


Today’s topic is
Signal Integrity with IBIS.

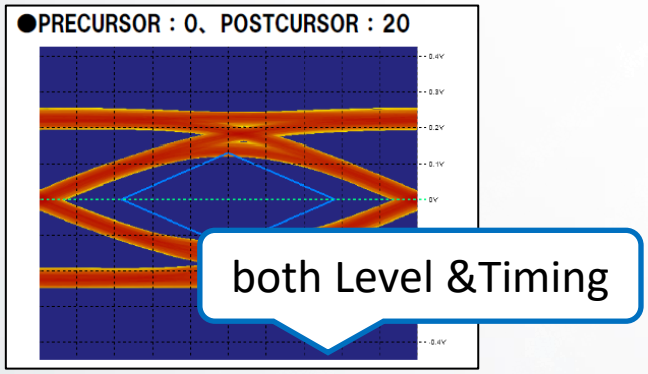
> Power Integrity  > Signal Integrity

# Review: Electrical Quality

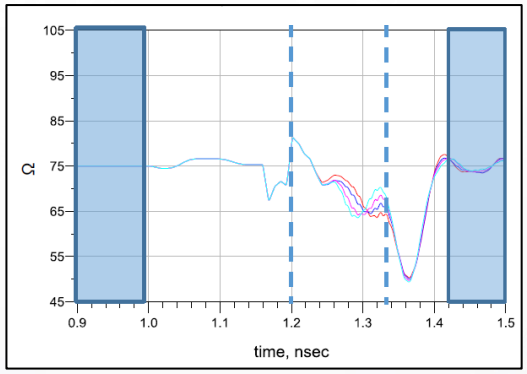
Signal Integrity: Being able to transmit and receive digital signals.



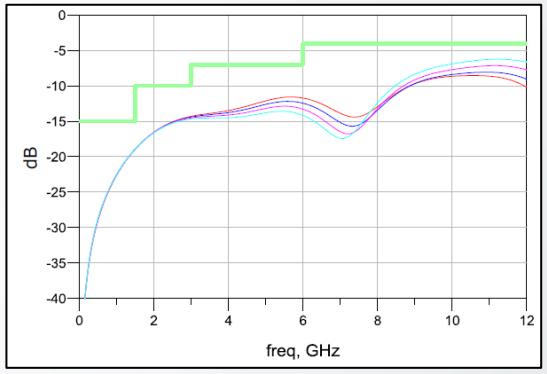

Some Simulations:




Eye pattern



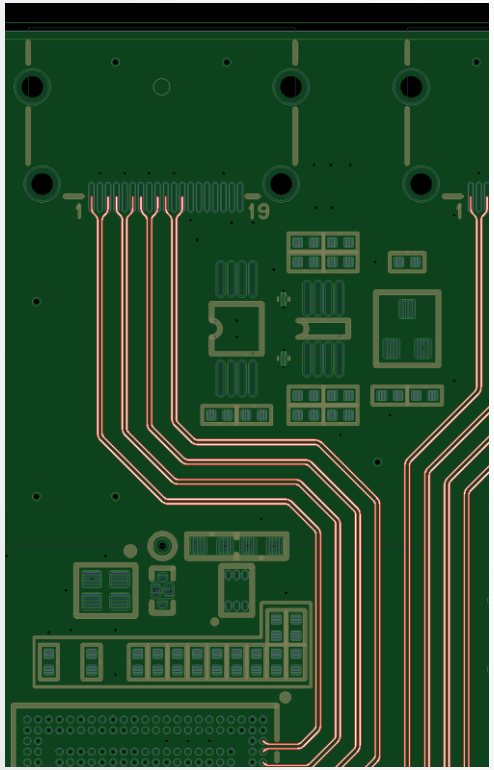

Time Domain Reflection




Return Loss

# Serial and Parallel Data Transmission

> Serial Data Transmission



PCIe gen5:
16GHz

QSFP28:
12.5GHz

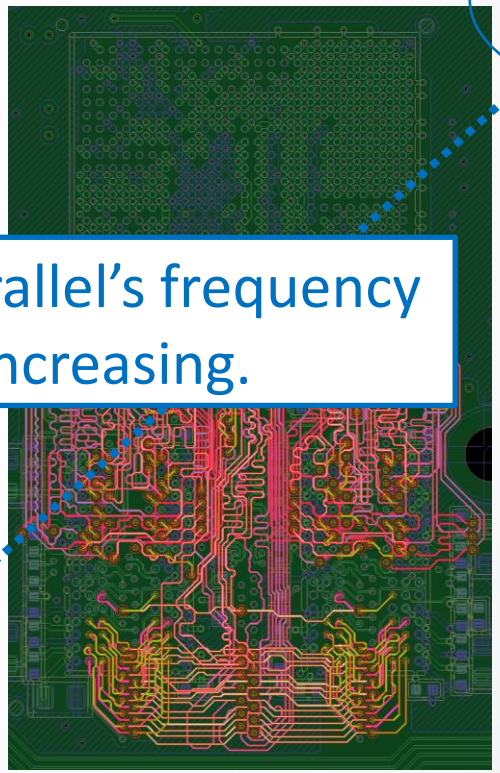
HDMI2.1:
6GHz

USB3.2 gen2:
5GHz

(3.2GHz)

/1lane

> Parallel Data Transmission



DDR5-6400:
3200MHz

DDR4-3200:
1600MHz

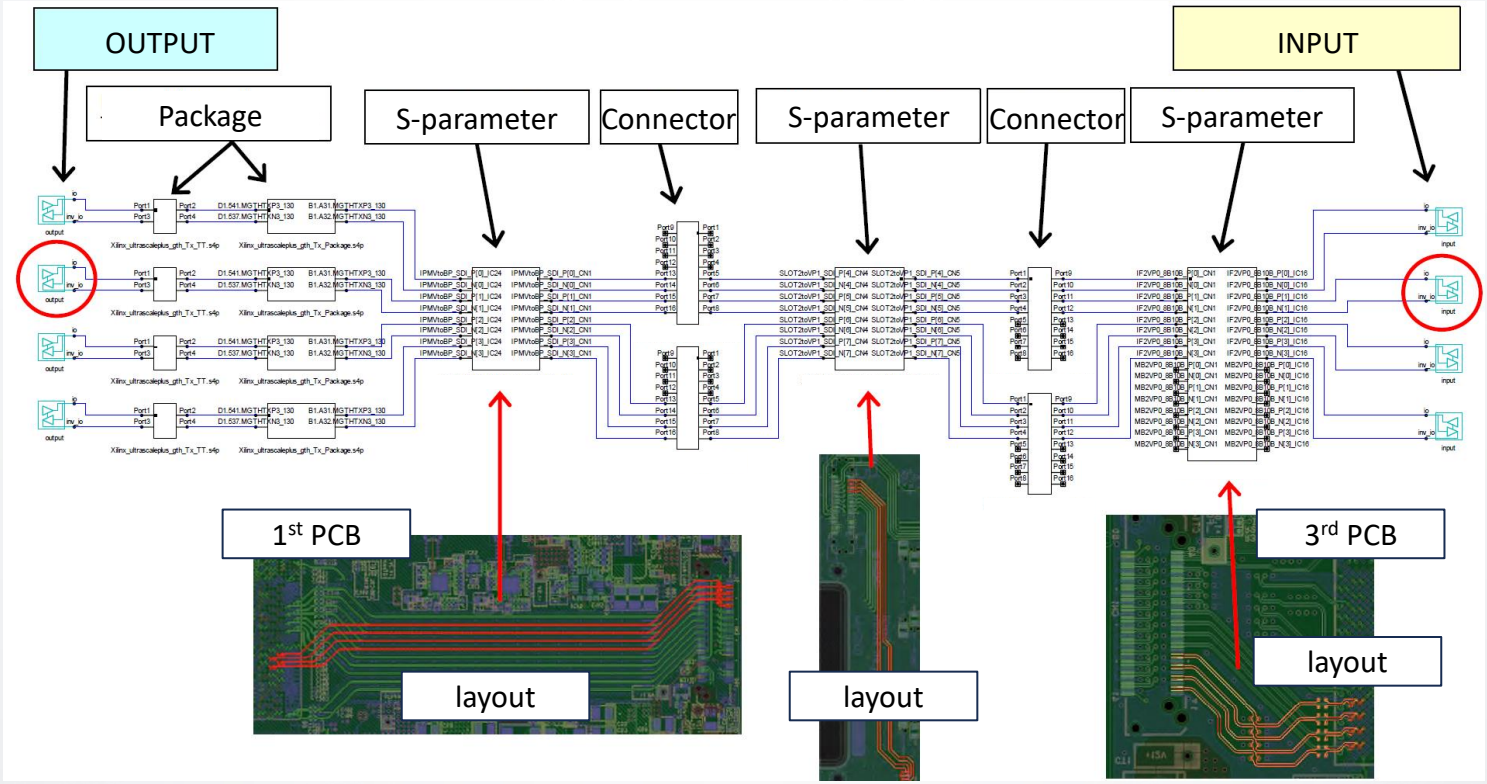
DDR3-1866:
933MHz

/Speed

Parallel's frequency is increasing.

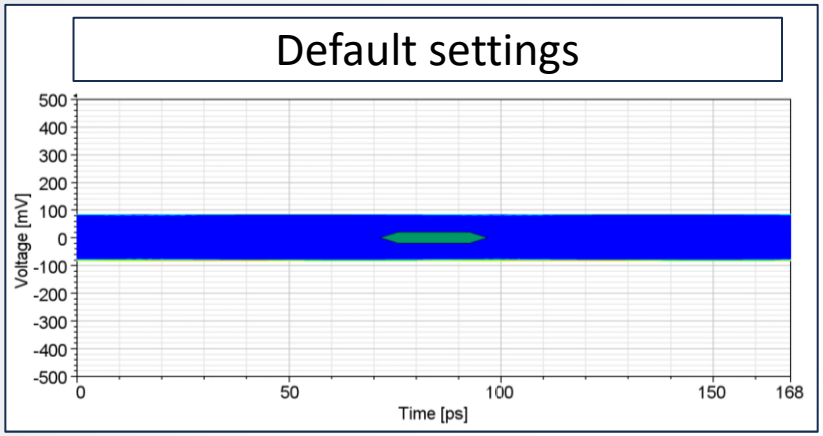
# Serial Data Transmission's Case

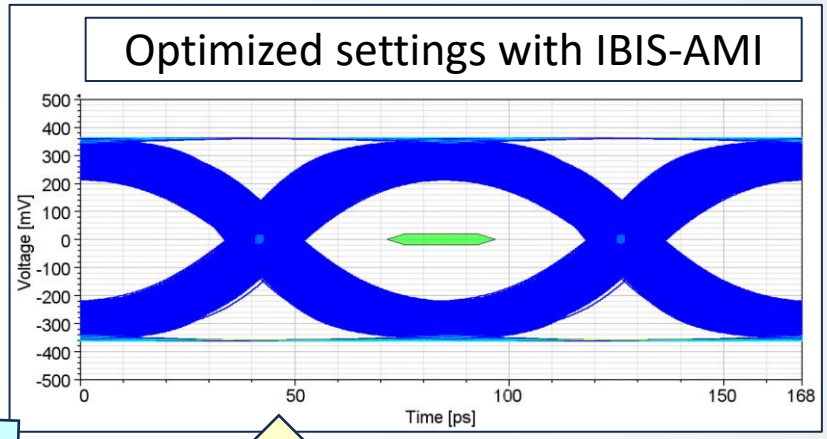
12G-SDI is necessary in the broadcasting. Inside the board, the signal's frequency is 6GHz at the differential pair.
<u>There is an impact of transmission loss.</u>




SDI: Serial Digital Interface

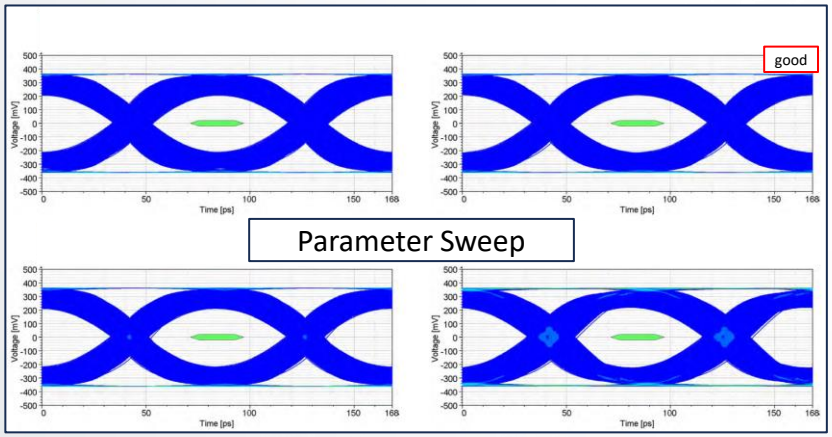
# Serial Data Transmission's Case

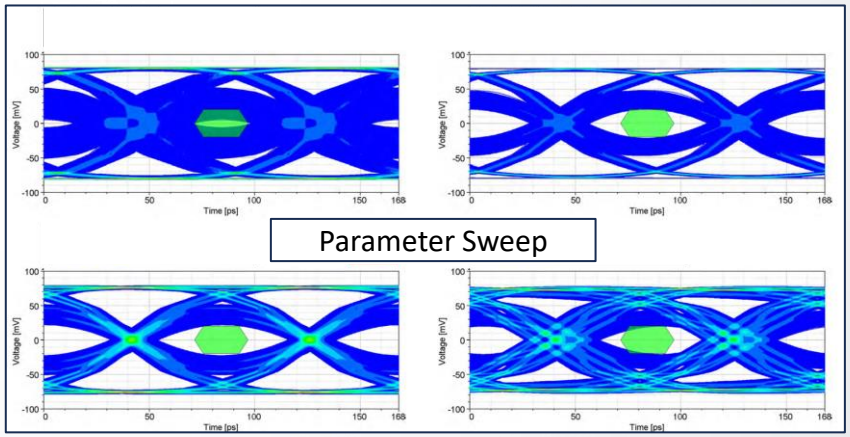



TXDIFFCTRL,TXPRE,TXPOST

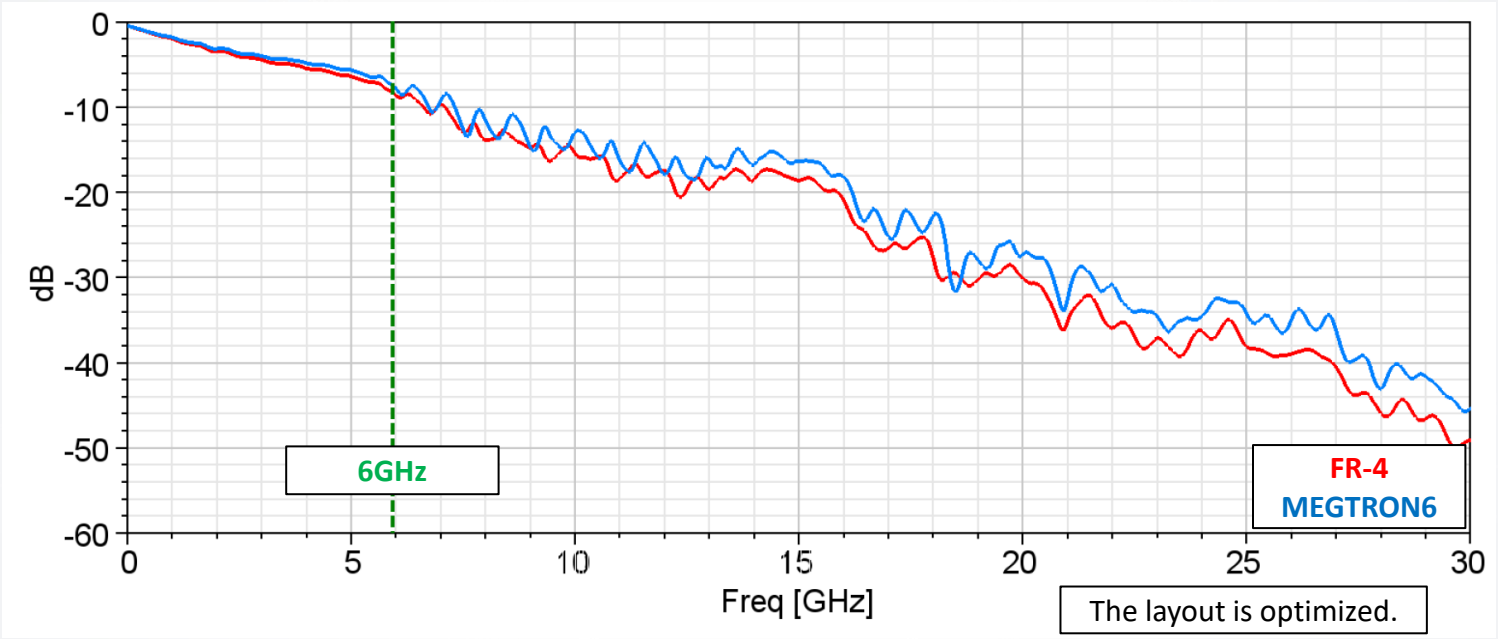
CTLE,DFE



# Serial Data Transmission's Case

FR-4 vs MEGTRON6 at SDD21




This graph shows the insertion loss of the transmission line by simulation. If it is known before manufacturing that transmission is possible using FR-4, costs can be reduced.

It's possible to simulate finding the best design.

# Parallel Data Transmission's Case

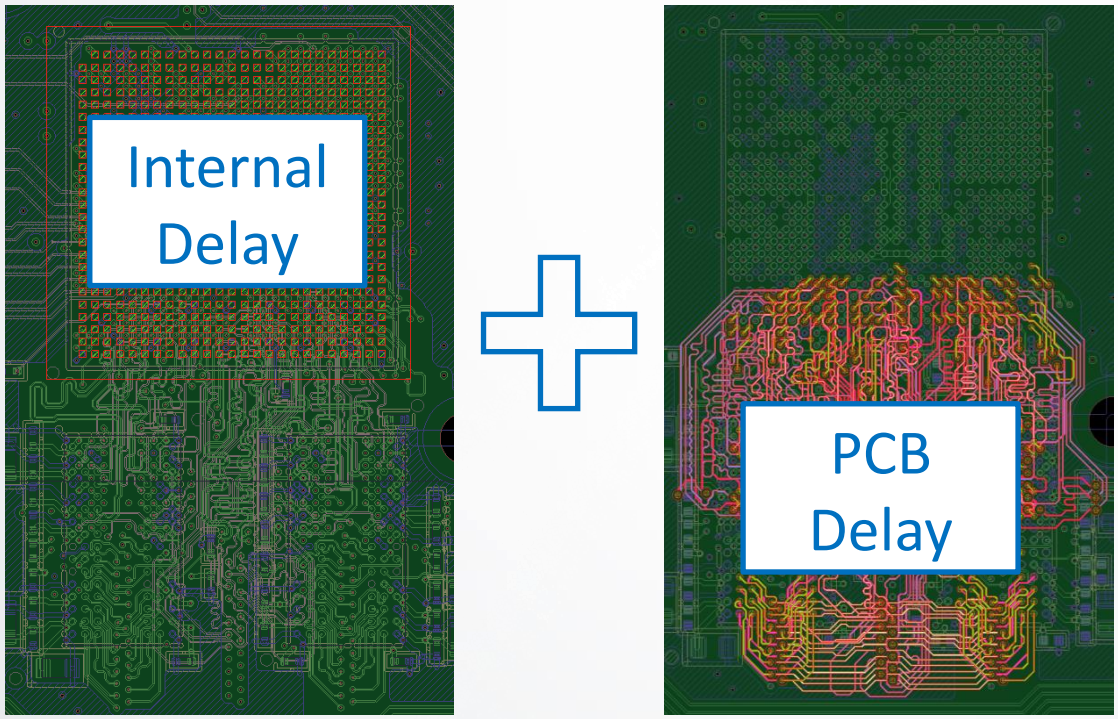
To design Parallel Data Transmission, It's important to match skew including the internal delay.

DDR4's Requirement

Total Length in Time

-3.5ps < DQ-DQS < 3.5ps

-20ps < CLK-ADDR < 20ps




PCB Delay = Via + Trace

Calculating the delay per unit length every layer and adjust the wiring length.
3.5ps is equivalent to 0.5mm.

# Parallel Data Transmission's Case

The table shows internal delays exported from FPGA Design Tool.
Based on this delay time, adjusting the PCB delay for matching skew.

e.g. DQ-DQS

| Signal Name | Pin Number | Internal Delay (ps) |
|---|---|---|
| DDR4_dqs_t[0] | AD11 | 136.555 |
| DDR4_dqs_c[0] | AD10 | 136.181 |
| DDR4_dq[7] | AA10 | 128.671 |
| DDR4_dq[6] | Y10 | 129.431 |
| DDR4_dq[5] | AB9 | 122.995 |
| DDR4_dq[4] | AB10 | 120.185 |
| DDR4_dq[3] | AC11 | 125.845 |
| DDR4_dq[2] | AB11 | 122.032 |
| DDR4_dq[1] | AA11 | 118.821 |
| DDR4_dq[0] | AA12 | 118.851 |

max(DQ) - DQS= -6.75ps
DQS - min(DQ) = 17.73ps

e.g. CLK-ADDR

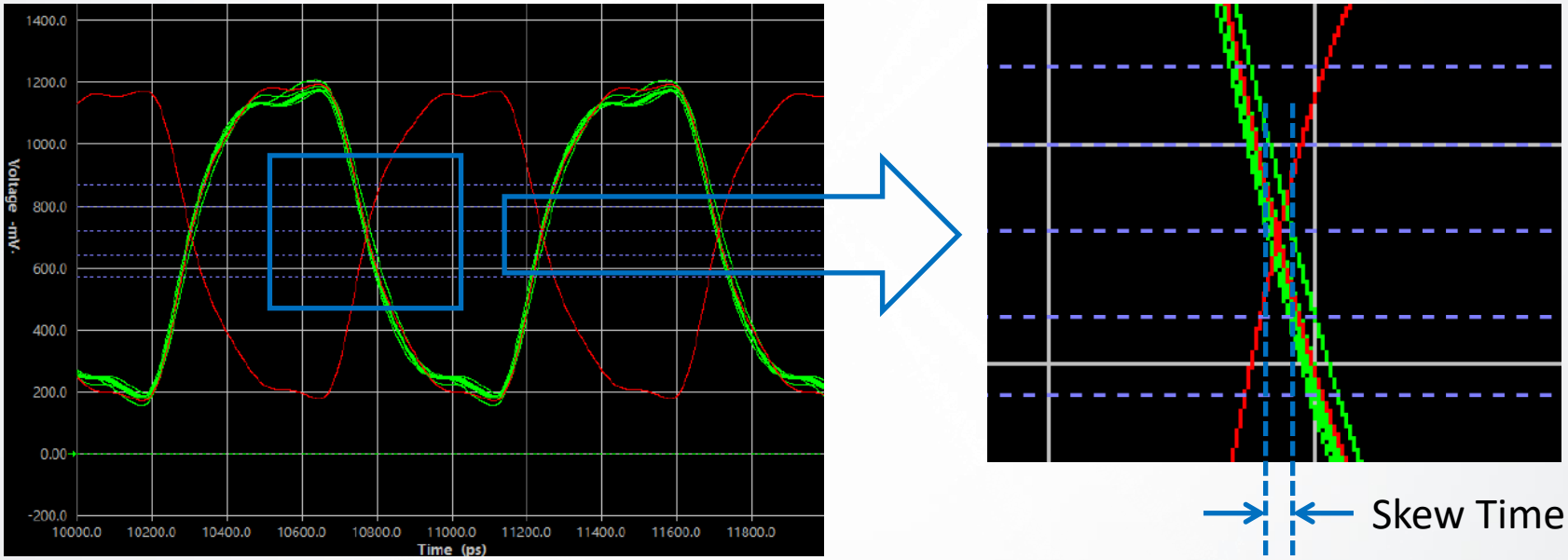
| Signal Name | Pin Number | Internal Delay (ps) |
|---|---|---|
| DDR4_ck_t[0] | AA3 | 182.941 |
| DDR4_ck_c[0] | AB3 | 183.515 |
| DDR4_adr[16] | AB4 | 162.598 |
| DDR4_adr[15] | AE4 | 185.645 |
| DDR4_adr[14] | AD4 | 185.922 |
| DDR4_adr[13] | AE5 | 171.412 |
| DDR4_adr[12] | AD5 | 167.074 |
| DDR4_adr[11] | AB5 | 162.556 |
| DDR4_adr[10] | AB6 | 162.691 |
| DDR4_adr[9] | AA1 | 191.654 |
| DDR4_adr[8] | AA2 | 187.748 |
| DDR4_adr[7] | AC1 | 191.921 |
| DDR4_adr[6] | AB1 | 187.316 |
| DDR4_adr[5] | AC2 | 184.296 |
| DDR4_adr[4] | AC3 | 181.334 |
| DDR4_adr[3] | AE1 | 205.786 |
| DDR4_adr[2] | AD1 | 199.816 |
| DDR4_adr[1] | AE2 | 188.745 |
| DDR4_adr[0] | AD2 | 188.023 |

max(ADDR) - CLK= 22.85ps
CLK - min(ADDR) = 20.96ps

# Parallel Data Transmission's Case

In simulation, the skew is measured from the waveform.
And internal delays contribute to this skew.

e.g. DQ-DQS




In this simulation case, internal delays are simulated using FPGA's [Define Package Model].

# Parallel Data Transmission's Case

Internal delays from the tool:

| Signal Name | Pin Number | Internal Delay (ps) |
|---|---|---|
| DDR4_dqs_t[0] | AD11 | 136.555 |
| DDR4_dqs_c[0] | AD10 | 136.181 |
| DDR4_dq[7] | AA10 | 128.671 |
| DDR4_dq[6] | Y10 | 129.431 |
| DDR4_dq[5] | AB9 | 122.995 |
| DDR4_dq[4] | AB10 | 120.185 |
| DDR4_dq[3] | AC11 | 125.845 |
| DDR4_dq[2] | AB11 | 122.032 |
| DDR4_dq[1] | AA11 | 118.821 |
| DDR4_dq[0] | AA12 | 118.851 |

Inductance and capacitance from IBIS's PKG:

[Inductance Matrix]
[Row] Y10
Y10 5.74183e-009

[Capacitance Matrix]
[Row] Y10
Y10 2.80919e-012

[Inductance Matrix]
[Row] AA11
AA11 5.27346e-009

[Capacitance Matrix]
[Row] AA11
AA11 2.66373e-012

$$Td = \sqrt{LC}\,[s]$$

127.004ps

118.520ps

Difference:
DQ[6] 2.427ps
DQ[1] 0.301ps

The values are similar but not exactly same.
It's expected this difference has an impact for the transmission when the frequency increases.

# Parallel Data Transmission's Case

Excerpt from the specification of package modeling:

- [Define Package Model]
  - [Manufacturer]
  - [OEM]
  - [Description]
  - [Number Of Sections]
  - [Number Of Pins]
  - [Pin Numbers]
  - [Merged Pins]
  - [Model Data]
    - [Resistance Matrix]
      - [Bandwidth]
      - [Row]
    - [Inductance Matrix]
      - [Bandwidth]
      - [Row]
    - [Capacitance Matrix]
      - [Bandwidth]
      - [Row]
    - [End Model Data]
  - [End Package Model]

## 7 PACKAGE MODELING

### 7.1 INTRODUCTION

Several package modeling formats are available in IBIS. These include:

1. Lumped [Component]-level models for the entire [Component], using the [Package] keyword.
2. Lumped [Component]-level modeling per-pin, using the [Pin] keyword.
3. [Package Model] (including [Alternate Package Models] and [Define Package Model]).
4. [Interconnect Model Group] and the keywords associated with it.

The lumped formats are described in the [Package] and [Pin] keyword definitions in Section 5. Keywords for use with the [Package Model] format are described in this section, while keywords for use with [Interconnect Model Group] are described in Section 12.

Specifying a Len or L/R/C value of zero is allowed. If Len = 0 is specified, then the L/R/C values are the total for that section. If a non-zero length is specified, then the total L/R/C for a section is calculated by multiplying the value of the Len subparameter by the value of the L, R, or C subparameter. However, if a non-zero length section is specified, the L and C for that section should be treated as distributed elements.

I think IBIS-ISS(Interconnect SPICE Subcircuit) is better for considering the internal delays, But whether FPGA Design Tool can export.

# Parallel Data Transmission's Case

If we assume the simulation results is correct, the internal delays exported  from FPGA Design Tool might be slightly different.

This means the PCB delay adjusted also might be slightly different.

I think we should discuss ways to eliminate this difference.

One way, how about allowing IBIS to take into the internal delays output by FPGA Design Tool?
In the case, L/C should be only used to calculate the impedance.

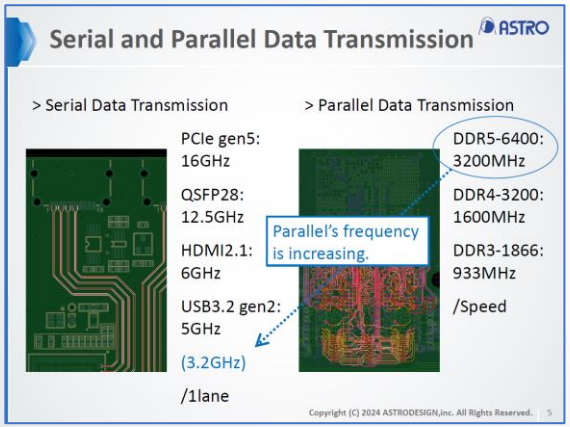
Whatever, it would be helpful if the simulator could suggest the meander length, not time.

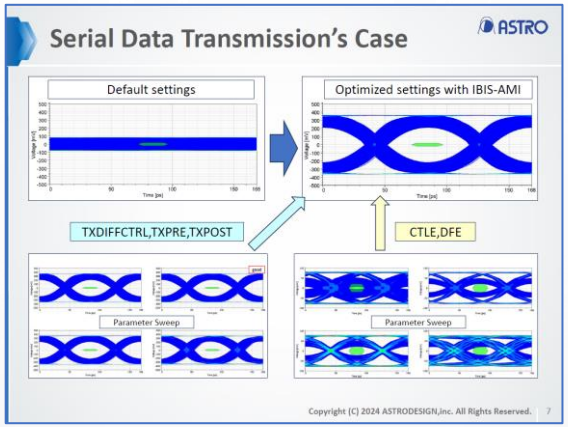
# Conclusion

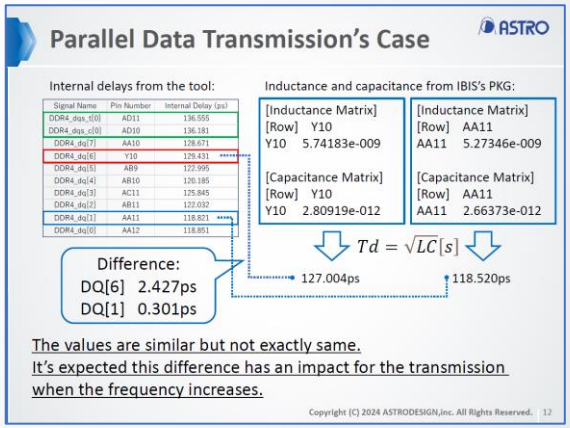
Both IBIS and IBIS-AMI is useful for the development.

Parallel data transmission's frequency is increasing.
So, it becomes difficult to design parallel data transmission more than serial data transmission.
Then, I suggested the need for discussion about FPGA's internal delays.

* Special thanks to KYODEN for their technical assistance.
https://www.kyoden.co.jp/



# Thank you &
# Any questions?


https://www.astrodesign.co.jp/