Challenges and Proposals in developing Models for High-Speed Memory Interface

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Agenda

1. Challenges of IBIS models
   due to High-Speed Memory Interface
2. Package Model Challenges
3. Equalizer Model Challenges
4. Summary

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1. Challenges of IBIS models due to High-Speed Memory Interface

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1. Challenges of IBIS models due to High-Speed Memory Interface

■Background

- Recently, memory interfaces need to support data rate above Gbps
- This has led to some challenges with IBIS model

■Challenges of IBIS Model

Package Model Challenges

- The frequency response of the package needs to be considered

  Current models that support Touchstone are not the best options

Equalizer Model Challenges

- Equalizer(DFE) is driven by an external clock(DQS)

  DQS timing must be adjusted for data transfer

- New DFE support

  Difficult to model DFE based on *DTSA. (*DTSA：Double-Tail Latch-type Voltage Sense Amplifier)

The details of these challenges will be explained on the following pages

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2.Package Model Challenges

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2.Package Model Challenges

■ Current models that support Touchstone：”Interconnect Model” and “EMD”

	Interconnect Model	EMD
Multiple connections	・Can be expressed by an ingenious method (cons)	・Can be expressed normally (pros)
EDA tool & Display Implementation	・Already in widespread use ・Displayed as package (pros)	・Not widespread as a model ・Package is often displayed with the inside expanded (cons)
File path specification	Unclear how to set description (cons)	
File Size	Increase due to high frequencies and parallel transfers (cons)	

Because of the challenges of both models, there is no optimal choice

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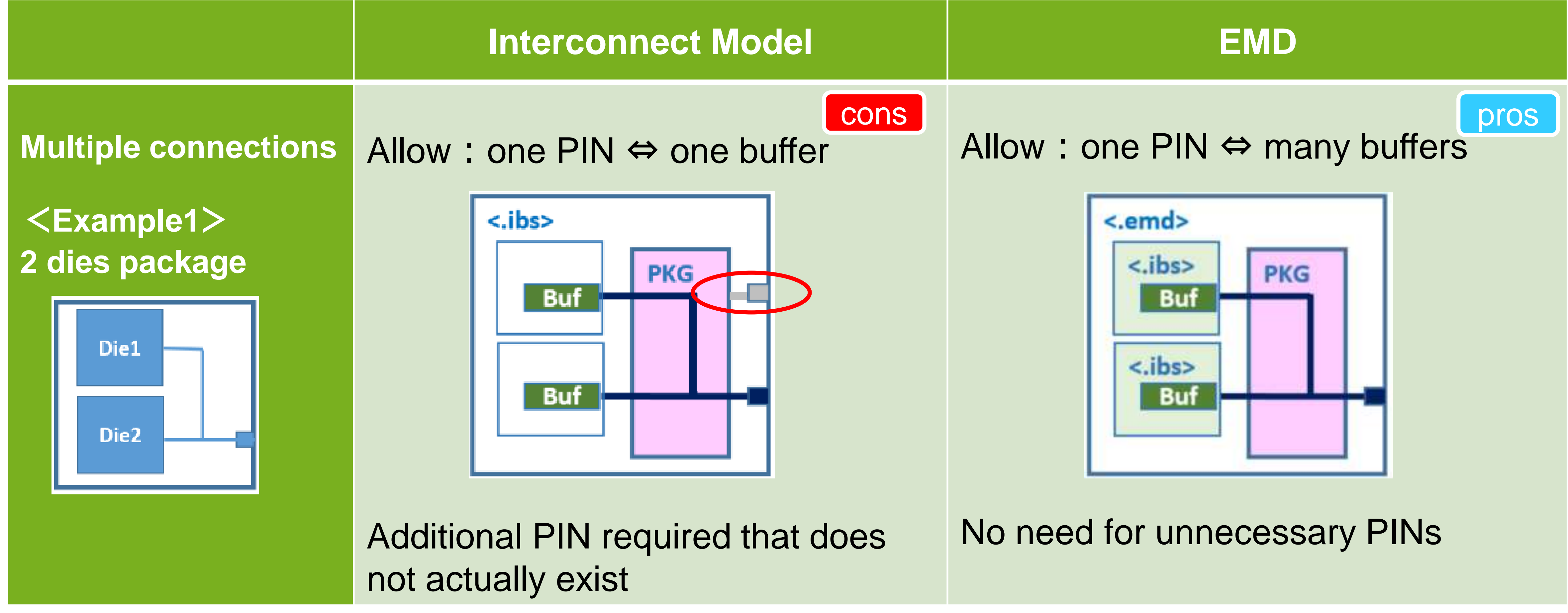
2.Package Model Challenges：Multiple connections support



Interconnect Model is insufficient for multiple connections

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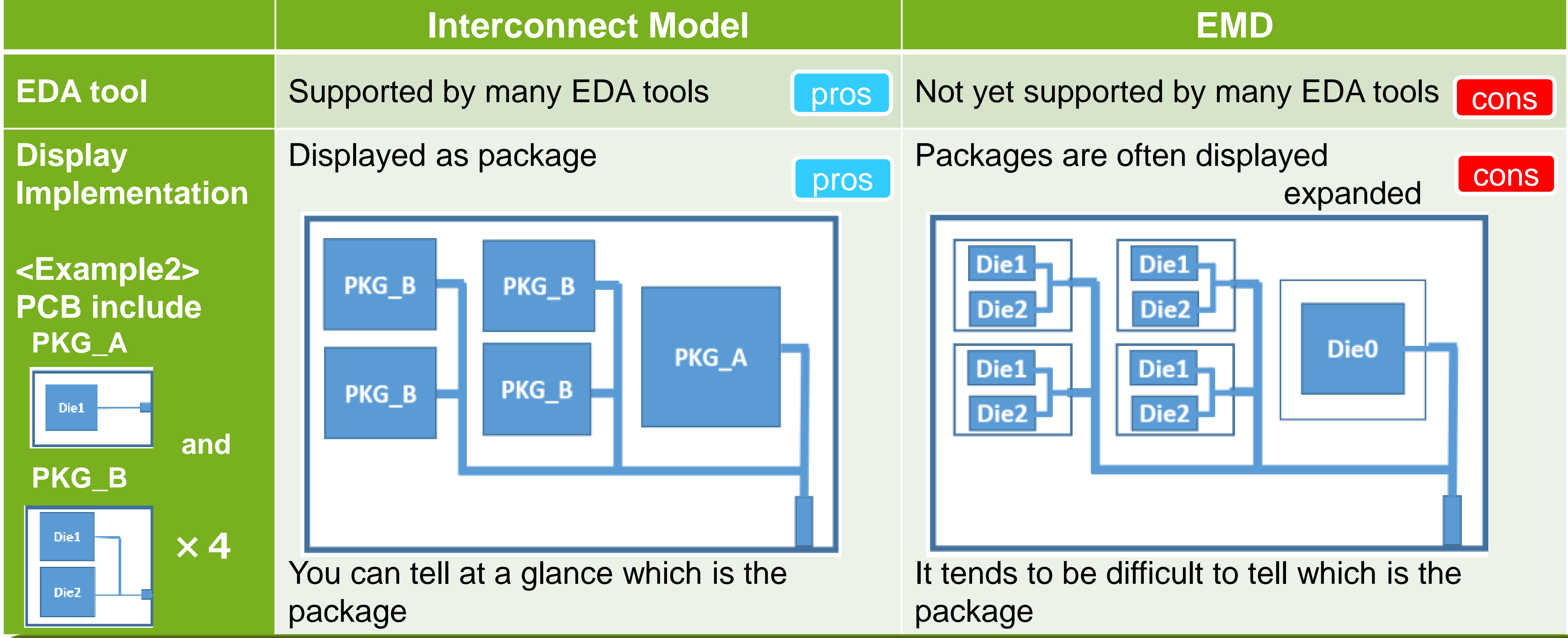
2.Package Model Challenges ：EDA tool / Display Implementation Support



Many EDA tools does not support the EMD model at this time
In EMD (similar to EBD) is difficult to distinguish between the package and the PCB

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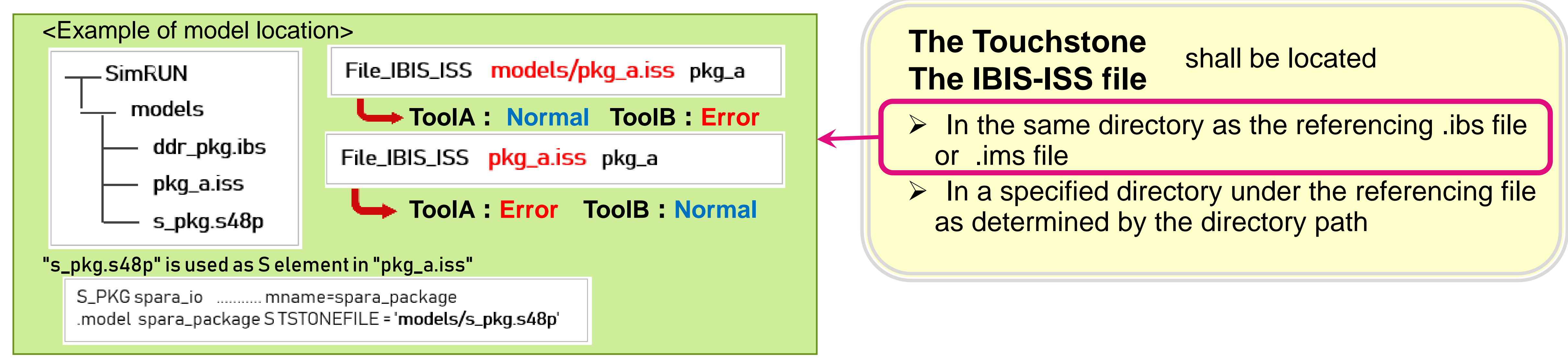
2.Package Model Challenges ：File path specification

■Touchstone/IBIS-ISS Setup

- The rules for the location are written in IBIS specification, but there is no clear description for the path setting
- Depending on the EDA tool, there are different ways of describing the path specification in the IBIS model



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2.Package Model Challenges ：Increase of file size

■File Size（S-parameter）

- Faster data rates expand the required frequency area
- Since the Memory is a parallel interface, more terminals are extracted at once
- As a result, file size of the extracted S-parameter is increasing more
- We need to be careful when using this model

  （ For example, disk usage, analysis time, etc. ）
- There is a trade-off between model accuracy and file size

More attention may be needed

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2.Package Model Challenges : Summary

■ Challenges

- Multiple connections・・・ Interconnect Model is insufficient
- EDA tool/Display Implementation・・・EMD model is not supported by many EDA tools, and in EMD is difficult to distinguish between the package and the PCB
- File path・・・There is no clear description for the path setting
- File Size・・・Increasing

We don’t have the best option as a package model.

■ Proposals

- Make Interconnect Model support Multiple connection as well as EMD
- Clear guidelines of the package model and promote the model to make it more popular
- Clear description and unified specification of the file path

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3. Equalizer Model Challenges

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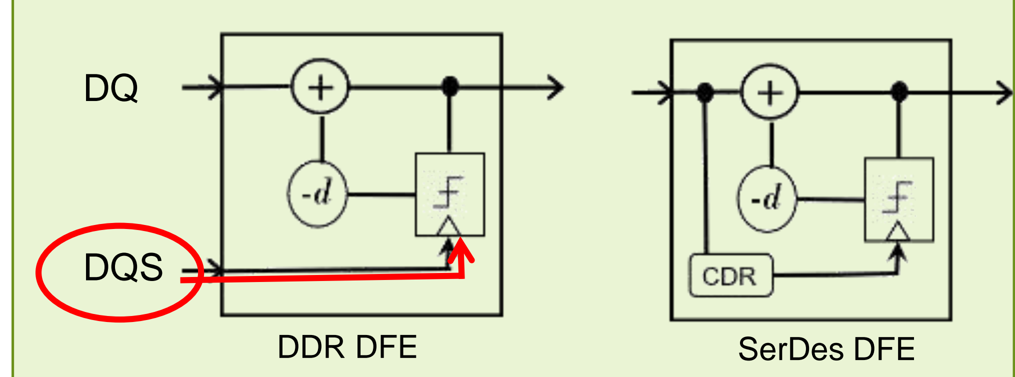
3. Equalizer Model Challenges： DFE is driven by an external clock(DQS).

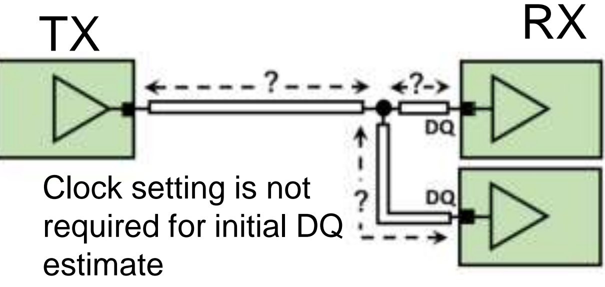
■Equalizer added to DDR specification due to higher Interface speeds

- DFE is clocked by an external clock(DQS)
（In SerDes systems, DFE is clocked by a CDR）
- IBIS-AMI also updated to work with external clocks
（added ”Rx_Use_Clock_Input”）



- Even when analyzing DQ signal with fixed DQS, DQS setting is required

(When considering Substrate Material, initial study of circuit topology, etc.)



New IBIS-AMI model applications have limitations.

■**Can we improve the specifications of the IBIS model?**

・For example, use a model with built-in CDR to match the timing after clock adjustment

Added the ability to switch DQS settings in IBIS specifications

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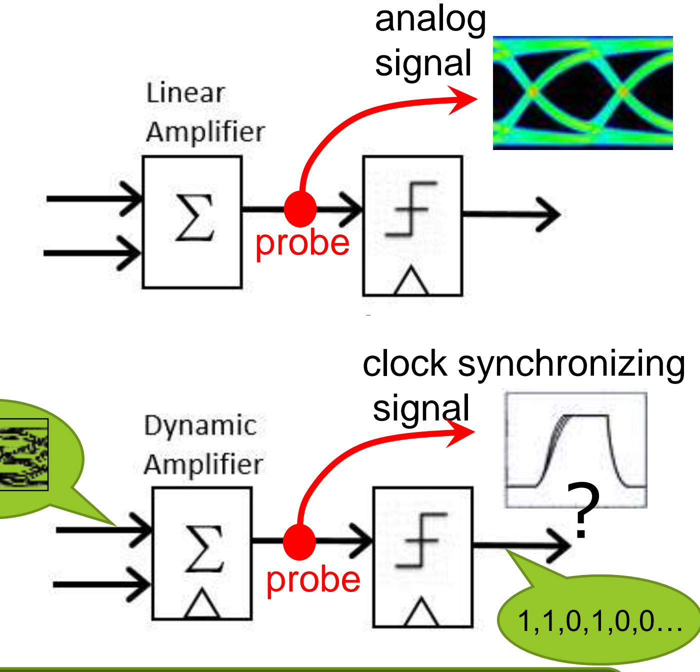
3. Equalizer Model Challenges ： DFE based on DTSA

■DFE based on DTSA are now seen

- DTSA use Dynamic Amplifier as Adder, which are different from usual Linear Amplifier
- The output of an Adder using a Linear Amplifier is a probe point normally, but the output of an Adder using a Dynamic amplifier results in a waveform unsuitable for a probe point
  Because that output isn't analog signal
- Then the only way is to probe the input signal of the DFE before equalizer processing or the digital signal output of the Slicer



How do we model IBIS-AMI of this DFE? How do we analyzed this DFE?

■We would like to hear the IBIS Open Forum's opinion on what should be done with this DFE in the future

- Maybe we should consider how to do SI analysis using EYE waveforms instead of considering them in the model in the first place
- Is it possible to incorporate a Pass/Fail determination method with digital signals?

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4.Summary

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4.Summary

■Discussed challenges and proposals for package and equalizer models of high-speed memory interfaces.

Challenge	Proposal
We don’t have the best option as a package model	✓ Make Interconnect Model support Multiple connection ✓ Clear guidelines of the package model and promote the model to make it more popular
Unclear how to set description of file path	✓ Clear description and unified specification of the file path
File size of S-parameter is increasing	✓ More attention may be needed
New IBIS-AMI model applications have limitations	✓ We would like to discuss it
Modeling DFE based on DTSA	✓ We would like to hear the IBIS Open Forum‘s opinion and discuss modeling New DFE

It is time to resolve the above challenges in Memory Interface
We would also like to discuss IBIS model development with the IBIS Open Forum and EDA Model Specialty Committee

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